Process Change Notification

PCN Number: PCN-2018-107 **PCN Notification Date:** 11/26/2018

Informational PCN

Data Sheet Update:

WM8231 version 4.8

Dear Customer,

This notification is to advise you of the following change.

With immediate effect, the data sheet for WM8231 has been updated to reflect a change of supported operating frequencies (MCLK, Sample Rates).

Special Note:
This document supersedes any prior communication regarding WM8231 version 4.8.

If you have any questions, please contact your Sales Representative.

Sincerely,

Quality Systems Administrator
Cirrus Logic Corporate Quality
Phone: +1(512) 851-4000

Process Change Notification

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Products Affected:

The devices listed on this page are the complete list of affected devices. According to our records, these are the devices that you have purchased within the past twenty-four (24) months. The corresponding customer part number is also listed, if available.

Technical details of this Process / Product Change follow on the next page(s).

Title:	Data Sheet Update: WM8231version 4.8					
Customer Contact:	Local Field Sales Representative		**Phone:** (512) 851-4000		**Dept:**	Corporate Quality
Proposed 1st Ship Date:		NA	**Estimated Sample Availability Date:**			NA
Change Type:						
	Assembly Site		Assembly Process		Assembly Materials	
	Wafer Fab Site		Wafer Fab Process		Wafer Fab Materials	
	Wafer Bump Site		Wafer Bump Process		Wafer Bump Material	
	Test Site		Test Process		Design	
	Electrical Specification		Mechanical Specification		Part Number	
	Packing/Shipping/Labeling	X	Other			
Comments:	Data Sheet Update					

PCN Details

Description of Change:

The supported operating frequencies (MCLK, Sample Rates) updated.

Data Sheet Reference:

WM8231: https://www.cirrus.com/products/wm8231/

WM8231 from version 4.7 to version 4.8

	Before	After
Feature (page 1)	1. LVDS/CMOS output option – LVDS 5pair 490 MHz 35-bit data – CMOS 90 MHz output maximum	1. LVDS/CMOS output option – LVDS 5-pair 315 MHz 35-bit data – CMOS 90 MHz output maximum
OUTPUT DATA TIMING (CMOS OUTPUT) (page 16)	Test condition with: AVDD = LDOVDD = DBVDD = 3.3V, AGND = LDOGND = DBGND= 0V, T_A = 25ºC, MCLK= 35MHz unless otherwise stated.	Test condition with: AVDD = LDOVDD = DBVDD = 3.3V, AGND = LDOGND = DBGND= 0V, T_A = 25ºC, MCLK= 30MHz unless otherwise stated.

Register PLL DLL SETUP (page 23)

Before

PLL DLL SETUP

WM8231 is supporting wide range of input frequency. PLL_EXDIV_SEL[2:0], LVDLGAIN[1:0] and DLGAIN[1:0] must be configured by MCLK clock rate and data output format.

Note that after PLL and DLL configuration, the device must be reset as the following step.

- R03[1:0]=11 (PDMD=1, PD=1)
- Delay 1ms
- R03[1:0]=00 (Normal operation)

Also, several LVDS operation mode is required to change internal LDO configuration to perform LVDS clocking properly. The following register need to set to change the LDO configuration.

- R1B0h=1
- R1B4h=12h

	Max sample rate	MCLK Clock rate [MHz]	30.1 ~ 35.0	30	25.0 ~ 29.9	15.0 ~ 23.3	12.5 ~ 14.99	10.0 ~ 12.49	8.33 ~ 9.99	7.5 ~ 8.32	5.0 ~ 7.49
CMOS 10 bit	30MHz	PLL_EXDIV_SEL[2:0]		000	000	001	001	001	001	010	010
		LVDLGAIN[1:0]									
		DLGAIN[1:0]		01	01	01	10	10	10	10	10
		LDO setting									
LVDS 5pair 10bit	35MHz	PLL_EXDIV_SEL[2:0]	001	001	001	010	010	011	011	011	100
		LVDLGAIN[1:0]	01	01	01	01	10	10	10	10	10
		DLGAIN[1:0]	01	01	01	01	10	10	10	10	10
		LDO setting									
LVDS 5pair 16bit LVDS 4pair 12bit LVDS 3pair 10bit	35MHz	PLL_EXDIV_SEL[2:0]	000	000	000	001	001	001	001	010	010
		LVDLGAIN[1:0]	00	00	01	01	01	01	10	10	10
		DLGAIN[1:0]	01	01	01	01	10	10	10	10	10
		LDO setting	12h	12h							
LVDS 3pair 16bit	23.3MHz	PLL_EXDIV_SEL[2:0]				001	001	001	001	010	010
		LVDLGAIN[1:0]				00	01	01	01	01	01
		DLGAIN[1:0]				01	10	10	10	10	10
		LDO setting				12h					

Table 4 PLL and DLL Setting

Register PLL DLL SETUP (page 23) - Continued

After

PLL DLL SETUP

The WM8231 supports a wide range of MCLK input frequencies. The PLL_EXDIV_SEL[2:0], LVDLGAIN[1:0] and DLGAIN[1:0] fields must be configured according to the MCLK frequency and the applicable data-output format – see Table 4. Note the LVDLGAIN field is not used in CMOS mode.

Note that after PLL and DLL configuration, the device must be reset as follows:

- R03[1:0]=11 (PDMD=1, PD=1)
- Delay 1 ms
- R03[1:0]=00 (Normal operation)

Under default conditions, the LDO2 voltage is 1.8V. To select 2.0V output as noted in Table 4, the following control sequence is required:

- R1B0h[0]=1
- R1B4h=12h

Data Format	Max sample rate	MCLK frequency (MHz)	30.1 ~ 35.0	30.0	25.0 ~ 29.9	15.1 ~ 23.3	15.0	12.5 ~ 14.99	10.0 ~ 12.49	8.33 ~ 9.99	7.5 ~ 8.32	5.0 ~ 7.49
CMOS 10-bit	30 MHz	PLL_EXDIV_SEL[2:0]	–	000	000	001	001	001	001	001	010	010
		DLGAIN[1:0]	–	01	01	01	01	10	10	10	10	10
		LDO2 voltage	–	1.8V	1.8V	1.8V	1.8V	1.8V	1.8V	1.8V	1.8V	1.8V
LVDS 10-bit 5-pair	35 MHz	PLL_EXDIV_SEL[2:0]	001	001	001	010	010	010	011	011	011	100
		LVDLGAIN[1:0]	01	01	01	01	01	10	10	10	10	10
		DLGAIN[1:0]	01	01	01	01	01	10	10	10	10	10
		LDO2 voltage	1.8V	1.8V	1.8V	1.8V	1.8V	1.8V	1.8V	1.8V	1.8V	1.8V
LVDS 16-bit 5-pair LVDS 10-bit 3-pair LVDS 12-bit 4-pair	30 MHz	PLL_EXDIV_SEL[2:0]	–	000	000	001	001	001	001	001	010	010
		LVDLGAIN[1:0]	–	00	01	01	01	01	01	10	10	10
		DLGAIN[1:0]	–	01	01	01	01	10	10	10	10	10
		LDO2 voltage	–	2.0V	1.8V	1.8V	1.8V	1.8V	1.8V	1.8V	1.8V	1.8V
LVDS 16-bit 3-pair	15 MHz	PLL_EXDIV_SEL[2:0]	–	–	–	–	001	001	001	001	010	010
		LVDLGAIN[1:0]	–	–	–	–	00	01	01	01	01	01
		DLGAIN[1:0]	–	–	–	–	01	10	10	10	10	10
		LDO2 voltage	–	–	–	–	2.0V	1.8V	1.8V	1.8V	1.8V	1.8V

Table 4 PLL and DLL Setting

OUTPUT DATA FORMAT (page 25)

Before

MODES	DESCRIPTION	OUTPUT DATA RATE	MAXIMUM MCLK RATE
1	LVDS 10-bit 5pair	MCLK x7	35MHz
2	LVDS 16-bit 5pair	MCLK x10.5	35MHz
3	LVDS 10-bit 3pair	MCLK x10.5	35MSPS
4	LVDS 16-bit 3pair	MCLK x21	21MSPS
5	LVDS 12-bit 4pair	MCLK x10.5	35MSPS
6	CMOS 10-bit	MCLK x3	30MHz

Table 5 Output Format and Data Rate

After

MODES	DESCRIPTION	OUTPUT DATA RATE	MAXIMUM MCLK RATE
1	LVDS 10-bit 5-pair	MCLK x 7	35 MHz
2	LVDS 16-bit 5-pair	MCLK x 10.5	30 MHz
3	LVDS 10-bit 3-pair	MCLK x 10.5	30 MHz
4	LVDS 16-bit 3-pair	MCLK x 21	15 MHz
5	LVDS 12-bit 4-pair	MCLK x 10.5	30 MHz
6	CMOS 10-bit	MCLK x 3	30 MHz

Table 5 Output Format and Data Rate

Process Change Notification

PCN Number: PCN-2018-107 **PCN Notification Date:** 11/26/2018

Reason for Change:

When operating some AFE devices at higher output data rate configurations, some devices operating in these conditions are not operating as expected and therefore more headroom in the clock generation block is required to ensure correct operation of all devices.

Therefore, a restriction has been applied to the maximum sample rate in various LVDS output configurations.

Anticipated Impact on Form, Fit, Function, Quality or Reliability:

No impact to form, fit, quality or reliability.
Impact to function as per the details above.

Anticipated Impact on Material Declaration:

☒ No Impact to the Material Declaration

☐ Material Declarations or Product Content reports are driven from production data and will be available following the production release.

Product Affected:

Device	Cirrus Logic Part Number
WM8231	WM8231GEFL/RV

Changes To Product Identification Resulting From This PCN:

No marking changes, this is a datasheet only change and the data sheet will be revised accordingly