DATASHEET

4G bits DDR4 SDRAM

D2516AN9EXGXN-TU (256M words x 16 bits)

•Specifications

•Density: 4G bits
•Organization
-32M words x 16 bits x 8 banks
•Package
-96-ball FBGA
- Lead-free
- Halogen-free
•Power supply (JEDEC standard 1.2V)
- VDD = 1.2V ± 0.06V
- VPP = 2.5V +0.25V / -0.125V
•Data rate
- 3200 Mbps max. Backward compatible
•8 internal banks
- 8 banks (4 banks x 2 bank groups) for x16 product
•Interface: Pseudo Open Drain (POD)
•Burst Length (BL): 8 and 4 with Burst Chop (BC)
•CAS Latency (CL):
10,11,12,13,14,15,16,17,18,19,20,21,22,24
•CAS Write Latency (CWL): 9,10,11,12,14,16,18,20
•Precharge: auto precharge option for each burst access
•Refresh: auto-refresh, self-refresh
•Refresh cycles
Average refresh period
7.8µs at 0°C ≤ TC ≤ +85°C
3.9µs at +85°C < TC ≤ +95°C
•Operating case temperature range
- 0°C to +95°C

•Features

- Double-data-rate architecture: two data transfers per clock cycle.
- The high-speed data transfer is realized by the 8 bits prefetch pipelined architecture.
- Bi-directional differential data strobe (DQS and /DQS) is transmitted/received with data for capturing data at the receiver.
- DQS is edge-aligned with data for READs; center- aligned with data for WRITEs.
- Differential clock inputs (CK_t and CK_c).
- DLL aligns DQ and DQS transitions with CK transitions.
- Data mask (DM) write data-in at the both rising and falling edges of the data strobe.
- Write Cycle Redundancy Code (CRC) is supported.
- Programmable preamble for read and write is supported.
- Programmable burst length 4/8 with both nibble sequential and interleave mode.
- BL switch on the fly.
- Driver strength selected by MRS.
- Dynamic On Die Termination supported.
- Two Termination States such as RTT_PARK and RTT_NOM switchable by ODT pin.
- Asynchronous RESET pin supported.
- ZQ calibration supported.
- Write Levelization supported.
- This product in compliance with the RoHS directive.
- Internal Vref DQ level generation is available.
- TCAR(Temperature Controlled Auto Refresh) mode is supported.
- LP ASR(Low Power Auto Self Refresh) mode is supported.
- Command Address (CA) Parity (command/address) mode is supported.
- Per DRAM Addressability (PDA).
- Fine granularity refresh is supported.
- Geardown Mode(1/2 rate, 1/4 rate) is supported.
- Self Refresh Abort is supported.
- Maximum power saving mode is supported.
- Banks Grouping is applied, and CAS to CAS latency(tCCD_L, tCCD_S) for the banks in the same or different bank group accesses are available.
- DMI pin support for write data masking and DBIdc functionality.

Revision History

Revision No.	History	Release date	Editor	Approved by
A00	Initial release	Jan 2024	Jona Lee	

**Products and specifications discussed herein are for evaluation and reference purposes only and are subject to change by without notice. All information discussed herein is provided on an "as is" basis, without warranties of any kind.*

Ordering Information

Part Number	Die revision	Organization (words x bits)	Internal Banks	JEDEC speed bin (CL-tRCD-tRP)	Package
D2516AN9EXGXN-TU	E	256M x 16	8	DDR4-3200 (22-22-22)	96-ball FBGA

Part Number

D 2516 A N9 E X G XN -TU

Type
D: Package Device

Organization
2516: 256M x 16

Product Family
A: DDR4, 1.2V

Manufacture
Kingston

Die Revision

Internal Code (Not in DRAM marking)

Speed
XN: 3200 22-22-22

Environment Code
G: Green
(RoHS Compliant+ Halogen Free)

Package Type
X: BGA 96

Pin Configurations

Pin Configurations (x16 configuration)

96-ball FBGA

	1	2	3	7	8	9
A	VDDQ	VSSQ	DQU0	DQSU_c	VSSQ	VDDQ
B	VPP	VSS	VDD	DQSU_t	DQU1	VDD
C	VDDQ	DQU4	DQU2	DQU3	DQU5	VSSQ
D	VDD	VSSQ	DQU6	DQU7	VSSQ	VDDQ
E	VSS	DMU_n, DBIU_n	VSSQ	DML_n, DBIL_n	VSSQ	VSS
F	VSSQ	VDDQ	DQSL_c	DQL1	VDDQ	ZQ
G	VDDQ	DQL0	DQSL_t	VDD	VSS	VDDQ
H	VSSQ	DQL4	DQL2	DQL3	DQL5	VSSQ
J	VDD	VDDQ	DQL6	DQL7	VDDQ	VDD
K	VSS	CKE	ODT	CK_t	CK_c	VSS
L	VDD	WE_n/ A14	ACT_n	CS_n	RAS_n/ A16	VDD
M	VREFCA	BG0	A10/AP	A12/ BC_n	CAS_n/ A15	VSS
N	VSS	BA0	A4	A3	BA1	TEN
P	RESET_n	A6	A0	A1	A5	ALERT_n
R	VDD	A8	A2	A9	A7	VPP
T	VSS	A11	PAR	NC	A13	VDD

Pin name	Function	Pin name	Function
A0 to A14*2	Address inputs A10(AP) : Auto precharge A12(/BC_n) : Burst chop	ODT*2	ODT control
BA0 to BA1*2	Bank select	RESET_n*2	Active low asynchronous reset
BG0	Bank group input	PAR	Command and address parity
DQU0 to DQU7 DQL0 to DQL7	Data input/output	ALERT_n	Alert
DQS_t, /DQS_c	Differential data strobe	TEN	Connectivity test mode enable
CS_n*2	Chip select	VDD	Supply voltage for internal circuit
RAS_n/A16*2 CAS_n/A15*2 WE_n/A14*2	Command input	VSS	Ground for internal circuit
ACT_n*2	Activation command input	VDDQ	Supply voltage for DQ circuit
CKE*2	Clock enable	VSSQ	Ground for DQ circuit
CK_t, CK_c	Differential clock input	VREFCA	Reference voltage for CA
DMU_n,DML_n	Write data mask	ZQ	Reference pin for ZQ calibration
DBIU_n,DBIL_n	Data bus inversion	NC*1	No connection

Notes :

1. Not internally connected with die.
2. Input only pins (address, command, CKE, ODT and RESET_n) do not supply termination.

Input/Output Functional Description

Table 1 : Input/Output function description

Symbol	Type	Function
CK_t, CK_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE, (CKE1)	Input	Clock Enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high through out read and write accesses input buffers, excluding CK_t, CK_c and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CS_n, (CS1_n)	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code.
ODT, (ODT1)	Input	On Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n/ TDQS_t, NU/TDQS_c (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x8 configurations. For x16 configuration ODT is applied to each DQ, DQSU_t, DQSU_c, DQSL_t, DQSL_c, DMU_n, and DML_n signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
ACT_n	Input	Activation Command Input : ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n, CAS_n/A15 and WE_n/A14 will be considered as Row Address A15 and A14
RAS_n/A16, CAS_n/A15, WE_n/A14	Input	Command Inputs RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, those are Addressing like A16,A15 and A14 but for non-activation com- mand with ACT_n High, those are Command pins for Read, Write and other command defined in command truth table.
DM_n/DBI_n/ TDQS_t, (DMU_n/DBI-U_n), (DML_n/ DBIL_n)	Input/Output	Input Data Mask and Data Bus Inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_nis sampled on both edges of DQS. DM is muxed with DBI function by Mode Register A10,A11,A12 setting in MR5. For x8 device, the function of DM or TDQS is enabled by Mode Register A11 setting in MR1. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH. TDQS is only supported in X8
BG0 - BG1	Input	Bank Group Inputs : BG0 - BG1 define to which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. x4/8 have BG0 and BG1 but x16 has only BG0
BA0 - BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A17	Input	Address Inputs: Provied the row address for ACTIVATE Commands and the column address for Read/Write commands th select one location out of the memory array in the respective bank. (A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have addi- tional functions, see other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is only defined for the x4 configration.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge).A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC_n	Input	Burst Chop: A12 / BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
RESET_n	Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of $V_{DD.}$

Symbol	Type	Function
DQ	Input / Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0~DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. During this mode, RTT value should be set to Hi-Z. Refer to vendor specific datasheets to determine which DQ is used.
DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c	Input / Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS_t, DQSL_t and DQSU_t are paired with differential signals DQS_c, DQSL_c and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.
TDQS_t, TDQS_c	Output	Termination Data Strobe: TDQS_t/TDQS_c is applicable for x8 DRAMs only. When enabled via Mode Register A11 = 1 in MR1, the DRAM will enable the same termination resistance function onTDQS_t/ TDQS_c that is applied to DQS_t/DQS_c. When disabled via mode register A11 = 0 in MR1, DM/DBI/ TDQS will provide the data mask function or Data Bus Inversion depending on MR5; A11,12,10and TDQS_c is not used. x4/x16 DRAMs must disable the TDQS function via mode register A11 = 0 in MR1.
PAR	Input	Command and Address Parity Input : DDR4 Supports Even Parity check in DRAMs with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity withACT_n,RAS_n,CAS_n/A15,WE_n/ A14,BG0-BG1,BA0-BA1,A15-A0. Input parity should maintain at the rising edge of the clock and at the same time with command & address with CS_n LOW
ALERT_n	Input/Output	Alert : It has multi functions such as CRC error flag , Command and Address Parity error flag as Output signal. If there is error in CRC, then Alert_n goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then Alert_n goes LOW for relatively long period until on going DRAM internal recovery transaction to complete. During Connectivity Test mode, this pin works as input. Using this signal or not is dependent on system. In case of not connected as Signal, ALERT_n Pin must be bounded to VDD on board.
TEN	Input	Connectivity Test Mode Enable : Required on x16 devices and optional input on x4/x8 with densities equal to or greater than 8Gb. HIGH in this pin will enable Connectivity Test Mode operation along with other pins. It is a CMOS rail to rail signal with AC high and low at 80% and 20% of VDD. Using this signal or not is dependent on System. This pin may be DRAM internally pulled low through a weak pull-down resistor to VSS.
NC		No Connect: No internal electrical connection is present.
VDDQ	Supply	DQ Power Supply: 1.2 V +/- 0.06 V
VSSQ	Supply	DQ Ground
VDD	Supply	Power Supply: 1.2 V +/- 0.06 V
VSS	Supply	Ground
VPP	Supply	DRAM Activating Power Supply: 2.5V (2.375V min , 2.75V max)
VREFCA	Supply	Reference voltage for CA
ZQ	Supply	Reference Pin for ZQ calibration

Table 2 : 4Gb Addressing Table

Configuration		256 Mb x16
Bank Address	# of Bank Groups	2
	BG Address	BG0
	Bank Address in a BG	BA0~BA1
Row Address		A0~A14
Column Address		A0~A9
Page size		2KB

CONTENTS

1. Electrical Conditions

- All voltages are referenced to VSS (GND)
- Execute power-up and Initialization sequence before proper device operation is achieved.

1.1. Absolute Maximum Ratings

Table 3: Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Notes
Power supply voltage	VDD	−0.3 to +1.50	V	1, 3
Power supply voltage for output	VDDQ	−0.3 to +1.50	V	1, 3
DRAM activation power supply	VPP	−0.3 to +3.0	V	4
Input voltage	VIN	−0.3 to +1.50	V	1, 3, 5
Output voltage	VOUT	−0.3 to +1.50	V	1, 3, 5
Storage temperature	Tstg	−55 to +100	°C	1,2

Notes:

1. Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage temperature is the case surface temperature on the center/top side of the DRAM.
3. VDD and VDDQ must be within 300mV of each other at all times; and VREFCA must be no greater than 0.6 × VDDQ, When VDD and VDDQ are less than 500mV; VREFCA may be equal to or less than 300mV.
4. VPP must be equal or greater than VDD/VDDQ at all times.
5. Overshoot area above 1.5V is specified in DDR4 Device Operation.

Caution: Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

1.2. Operating Temperature Condition

Table 4: Operating Temperature Condition

Parameter	Symbol	Rating	Unit	Notes
Commercial temperature	TC	0 to +95	°C	1,2,3

Notes:

1. Operating case temperature is the case surface temperature on the center/top side of the DRAM.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0°C to +85°C under all operating conditions.
3. Some applications require operation of the DRAM in the Extended Temperature Range between +85°C and +95°C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply: Refresh commands must be doubled in frequency, therefore reducing the refresh interval tREFI to 3.9µs. (This double refresh requirement may not apply for some devices.)

1.3. Recommended DC Operating Conditions

Table 5: Recommended DC Operating Conditions (TC = 0°C to +95°C)

Parameter	Symbol	min	typ	max	Unit	Notes
Supply voltage	VDD	1.14	1.2	1.26	V	1, 2, 3
Supply voltage for DQ	VDDQ	1.14	1.2	1.26	V	1, 2, 3
Dram activating power	VPP	2.375	2.5	2.75	V	3

Notes:

1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3. DC bandwidth is limited to 20MHz..

1.4. IDD, IPP and IDDQ Measurement Conditions

In this chapter, IDD, IPP and IDDQ measurement conditions such as test load and patterns are defined.
The figure Measurement Setup and Test Load for IDD, IPP and IDDQ Measurements shows the setup and test load for IDD, IPP and IDDQ measurements.

- IDD currents (such as IDD0, IDD0A, IDD1, IDD1A, IDD2N, IDD2NA, IDD2NL, IDD2NT, IDD2P, IDD2Q, IDD3N, IDD3NA, IDD3P, IDD4R, IDD4RA, IDD4W, IDD4WA, IDD5B, IDD5F2, IDD5F4, IDD6N, IDD6E, IDD6R, IDD6A, IDD7 and IDD8) are measured as time-averaged currents with all VDD balls of the DDR4 SDRAM under test tied together. Any IPP or IDDQ current is not included in IDD currents.
- IPP currents have the same definition as IDD except that the current on the VPP supply is measured.
- IDDQ currents (such as IDDQ2NT and IDDQ4R) are measured as time-averaged currents with all VDDQ balls of the DDR4 SDRAM under test tied together. Any IDD current is not included in IDDQ currents.

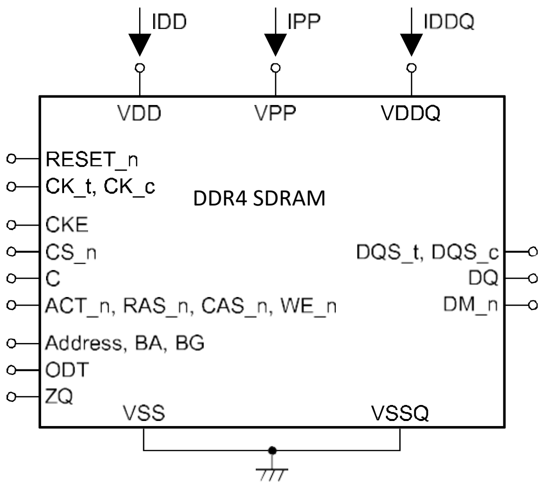
Note: IDDQ values cannot be directly used to calculate I/O power of the DDR4 SDRAM. They can be used to support correlation of simulated I/O power to actual I/O power as outlined in correlation from simulated channel I/O power to actual channel I/O power supported by IDDQ measurement.

For IDD, IPP and IDDQ measurements, the following definitions apply:

- L and 0: VIN ≤ VIL(AC) max
- H and 1: VIN ≥ VIH(AC) min
- MID-LEVEL: defined as inputs are VREFCA = VDD / 2
- Timings used for IDD, IPP and IDDQ measurement-loop patterns are provided in Table 8.
- Basic IDD, IPP and IDDQ measurement conditions are described in Table 9.

Note: The IDD, IPP and IDDQ measurement-loop patterns need to be executed at least one time before actual IDD or IDDQ measurement is started.

- Detailed IDD, IPP and IDDQ measurement-loop patterns are described in IDD0 Measurement-Loop Pattern table through IDD7 Measurement-Loop Pattern table.
- IDD Measurements are done after properly initializing the DDR4 SDRAM. This includes but is not limited to setting.
  RON = RZQ/7 (34Ω in MR1);
  Qoff = 0B (Output buffer enabled in MR1);
  RTT_Nom = RZQ/6 (40Ω in MR1);
  RTT_WR = RZQ/2 (120Ω in MR2);
  RTT_PARK = Disable;
  TDQS_t feature disabled in MR1;
  CRC disabled in MR2;
  CA parity feature disabled in MR5;
  Gear-down mode disabled in MR3;
  Read/Write DBI disabled in MR5;
  DM_n disabled in MR5
- Define D = {CS_n, ACT_n, RAS_n, CAS_n, WE_n} : = {H, L, L, L, L} ; apply BG/BA changes when directed.
- Define /D = {CS_n, ACT_n, RAS_n, CAS_n, WE_n} : = {H, H, H, H, H}; apply BG/BA changes when directed



Note: DIMM level Output test load condition may be different from above.

Figure 1: Measurement Setup and Test Load for IDD, IPP and IDDQ Measurements

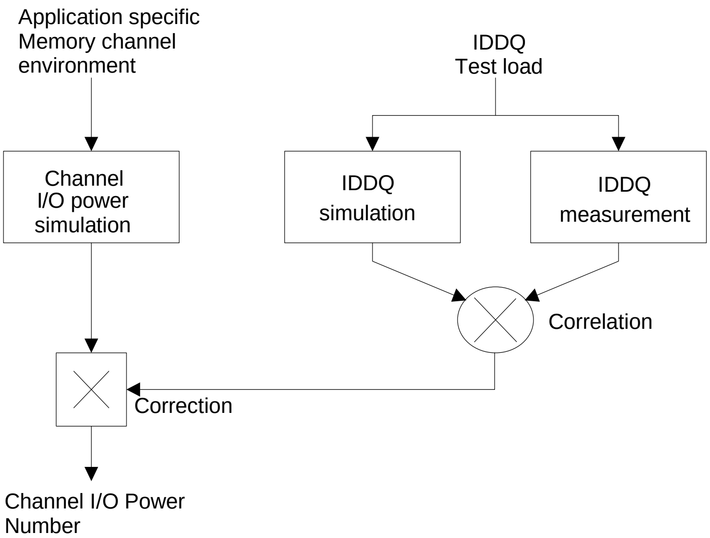


Figure 2: Correlation from Simulated Channel I/O Power to Actual Channel I/O Power Supported by IDDQ Measurement

1.4.1. Timings Used for IDD and IDDQ Measurement-Loop Patterns

Table 6 : Timings Used for IDD and IDDQ Measurement-Loop Patterns

Parameter	DDR4-3200	Unit
	22-22-22	
tCK	0.625	ns
CL	22	nCK
CWL	20	nCK
nRCD	22	nCK
nRC	74	nCK
nRAS	52	nCK
nRP	22	nCK
nFAW	48	nCK
nRRDS	9	nCK
nRRDL	11	nCK
tCCD_S	4	nCK
tCCD_L	8	nCK
tWTR_S	4	nCK
tWTR_L	12	nCK
nRFC 4Gb	416	nCK

1.4.2. Basic IDD and IDDQ Measurement Conditions

Table 7: Basic IDD, IPP and IDDQ Measurement Conditions

Parameter	Symbol	Description
Operating one bank active precharge current (AL=0)	IDD0	CKE: H; External clock: on; tCK, nRC, nRAS, CL: see Table 6; BL: 8*1; AL: 0; CS_n: H between ACT and PRE; Command, address, bank address inputs: partially toggling according to Table 8; Data I/O: VDDQ; DM_n: stable at 1; Bank activity: cycling with one bank active at a time: 0,0,1,1,2,2,... (see Table 8); Output buffer and RTT: enabled in MR*2; ODT signal: stable at 0; Pattern details: see Table 8
Operating One Bank Active-Precharge Current (AL=CL-1)	IDD0A	AL = CL-1, Other conditions: see IDD0
Operating One Bank Active-Precharge IPP Current	IPP0	Same condition with IDD0
Operating one bank active-read-precharge current (AL=0)	IDD1	CKE: H; External clock: On; tCK, nRC, nRAS, nRCD, CL: see Table 6; BL: 8*1, *6; AL: 0; CS_n: H between ACT, RD and PRE; Command, address, bank address inputs, data I/O: partially toggling according to Table 9; DM_n: stable at 1; Bank activity: cycling with one bank active at a time: 0,0,1,1,2,2,... (see Table 9); Output buffer and RTT: enabled in MR*2; ODT Signal: stable at 0; Pattern details: see Table 9
Operating One Bank Active-Read-Precharge Current (AL=CL-1)	IDD1A	AL=CL-1, Other conditions : see IDD1
Operating One Bank Active-Read-Precharge IPPCurrent	IPP1	Same condition with IDD1
Precharge standby current (AL=0)	IDD2N	CKE: H; External clock: on; tCK, CL: see Table 6 BL: 8*1; AL: 0; CS_n: stable at 1; Command, address, bank address Inputs: partially toggling according to Table 10; data I/O: VDDQ; DM_n: stable at 1; bank activity: all banks closed; output buffer and RTT: enabled in mode registers*2; ODT signal: stable at 0; pattern details: see Table 10
Precharge Standby Current (AL=CL-1)	IDD2NA	AL = CL-1, Other conditions: see IDD2N
Precharge Standby IPP Current	IPP2N	Same condition with IDD2N
Precharge standby ODT current	IDD2NT	CKE: H; External clock: on; tCK, CL: see Table 6; BL: 8*1; AL: 0; CS_n: stable at 1; Command, address, bank address Inputs: partially toggling according to Table 11; data I/O: VSSQ; DM_n: stable at 1; bank activity: all banks closed; output buffer and RTT: enabled in MR*2; ODT signal: toggling according to Table 11; pattern details: see Table 11
Precharge standby ODT IDDQ current	IDDQ2NT (Optional)	Same definition like for IDD2NT, however measuring IDDQ current instead of IDD current
Precharge Standby Current with CAL enabled	IDD2NL	Same definition like for IDD2N, CAL enabled*3
Precharge Standby Current with Gear Down mode enabled	IDD2NG	Same definition like for IDD2N, Gear Down mode enabled*3, *5
Precharge Standby Current with DLL disabled	IDD2ND	Same definition like for IDD2N, DLL disabled*3
Precharge Standby Current with CA parity enabled	IDD2N_par	Same definition like for IDD2N, CA parity enabled*3

Parameter	Symbol	Description
Precharge Power-Down Current	IDD2P	CKE: Low; External clock: on; tCK, CL: see Table 6; BL: 8*1; AL: 0; CS_n: stable at 1; Command, address, bank group address, bank address inputs: stable at 0; data I/O: VDDQ; DM_n: stable at 1; bank activity: all banks closed; output buffer and RTT: enabled in MR*2; ODT signal: stable at 0
Precharge Power-Down IPP Current	IPP2P	Same condition with IDD2P
Precharge Quiet Standby Current	IDD2Q	CKE: H; External clock: On; tCK, CL: see Table 6; BL: 8*1; AL: 0; CS_n: stable at 1; Command, address, bank group address, bank address Inputs: stable at 0; data I/O: VDDQ; DM_n: stable at 1;bank activity: all banks closed; output buffer and RTT: enabled in MR*2; ODT signal: stable at 0
Active standby current	IDD3N	CKE: H; External clock: on; tCK, CL: see Table 6; BL: 8*1; AL: 0; /CS: stable at 1; Command, address, bank group address, bank address Inputs: partially toggling according to Table 10; data I/O: VDDQ; DM_n:stable at 1; bank activity: all banks open; output buffer and RTT: enabled in MR*2; ODT signal: stable at 0; pattern details: see Table 10
Active Standby Current (AL=CL-1)	IDD3NA	AL = CL-1, Other conditions: see IDD3N
Active Standby IPP Current	IPP3N	Same condition with IDD3N
Active power-down current	IDD3P	CKE: L; External clock: on; tCK, CL: see Table 6; BL: 8*1; AL: 0; CS_n: stable at 1; Command, address, bank group address, bank address inputs: stable at 0; data I/O: VDDQ;; DM_n:stable at 1; bank activity: all banks open; output buffer and RTT: enabled in MR*2; ODT signal: stable at 0
Active Power-Down IPP Current	IPP3P	Same condition with IDD3P
Operating burst read current	IDD4R	CKE: H; External clock: on; tCK, CL: see Table 6; BL: 8*1, *6; AL: 0; CS_n: H between RD; Command, address, Bank group address, bank address Inputs: partially toggling according to Table 12; data I/O: seamless read data burst with different data between one burst and the next one according to Table 12; DM_n: stable at 1; Bank activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... (see Table 12); Output buffer and RTT: enabled in MR*2; ODT signal: stable at 0; pattern details: see Table 12
Operating Burst Read Current (AL=CL-1)	IDD4RA	AL = CL-1, Other conditions: see IDD4R
Operating Burst Read Current with Read DBI	IDD4RB	Read DBI enabled*3, Other conditions: see IDD4R
Operating Burst Read IPP Current	IPP4R	Same condition with IDD4R
Operating Burst Read IDDQ Current	IDDQ4R (Optional)	Same definition like for IDD4R, however measuring IDDQ current instead of IDD current
Operating Burst Read IDDQ Current with Read DBI	IDDQ4RB (Optional)	Same definition like for IDD4RB, however measuring IDDQ current instead of IDD current

Parameter	Symbol	Description
Operating Burst Write Current	IDD4W	CKE: H; External clock: on; tCK, CL: see Table 6; BL: 8*1; AL: 0; CS_n: H between WR; command, address, bank group address, bank address inputs: partially toggling according to Table 13; data I/O: seamless write data burst with different data between one burst and the next one according to Table 13;DM_n: stable at 1; bank activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,.. (see Table 13); output buffer and RTT: enabled in MR*2; ODT signal: stable at H; pattern details: see Table 13
Operating Burst Write Current(AL=CL-1)	IDD4WA	AL = CL-1, Other conditions: see IDD4W
Operating Burst Write Current with Write DBI	IDD4WB	Write DBI enabled*3, Other conditions: see IDD4W
Operating Burst Write Current with Write CRC	IDD4WC	Write CRC enabled*3, Other conditions: see IDD4W
Operating Burst Write Current with CA Parity	IDD4W_par	CA Parity enabled*3, Other conditions: see IDD4W
Operating Burst Write IPP Current	IPP4W	Same condition with IDD4W
Burst Refresh Current (1X REF)	IDD5B	CKE: H; External clock: on; tCK, CL, nRFC: see Table 6; BL: 8*1; AL: 0; CS_n: H between REF; Command, address, bank group address, bank address Inputs: partially toggling according to Table 14; data I/O: VDDQ; DM_n: stable at 1; bank activity: REF command every nRFC (Table 14); output buffer and RTT: enabled in MR*2; ODT signal: stable at 0; pattern details: see Table 14
Burst Refresh IPP Current (1X REF)	IPP5B	Same condition with IDD5B
Burst Refresh Current (2X REF)	IDD5F2	tRFC=tRFC_x2, Other conditions: see IDD5B
Burst Refresh Write IPP Current (2X REF)	IPP5F2	Same condition with IDD5F2
Burst Refresh Current (4X REF)	IDD5F4	tRFC=tRFC_x4, Other conditions: see IDD5B
Burst Refresh Write IPP Current (4X REF)	IPP5F4	Same condition with IDD5F4
Self Refresh Current: Normal Temperature Range	IDD6N	Commercial temperature : 0 to 85°C and Industrial temperature -40 to 85°C; LP ASR: Normal*4; CKE: L; External clock: off; CK_t and CK_c: L; CL: see Table 6; BL: 8*1; AL: 0; CS_n, command, address, bank group address, bank address, data I/O: H; DM_n: stable at 1; bank activity: self-refresh operation; Output buffer and RTT: enabled in MR*2; ODT signal: MID-LEVEL
Self Refresh IPP Current: Normal Temperature Range	IPP6N	Same condition with IDD6N
Self-Refresh Current: Extended Temperature Range	IDD6E	Commercial temperature : 0 to 95°C and Industrial temperature -40 to 95°C; LP ASR: Extended*4; CKE: L; External clock: off; CK_t and CK_c: L; CL: see Table 6; BL: 8*1; AL: 0; CS_n, command, address, bank group address, bank address, data I/O: H; DM_n: stable at 1; bank activity: Extended temperature self-refresh operation; Output buffer and RTT: enabled in MR*2; ODT signal: MID-LEVEL
Self Refresh IPP Current: Extended Temperature Range	IPP6E	Same condition with IDD6E

Parameter	Symbol	Description
Self-Refresh Current: Reduced Temperature Range	IDD6R	Commercial temperature : 0 to 45°C and Industrial temperature -40 to 45°C; LP ASR: Reduced*4; CKE: L; External clock: off; CK_t and CK_c: L; CL: see Table 6; BL: 8*1; AL: 0; CS_n, command, address, bank group address, bank address, data I/O: H; DM_n: stable at 1; bank activity: Reduced temperature self-refresh operation; Output buffer and RTT: enabled in MR*2; ODT signal: MID-LEVEL
Self Refresh IPP Current: Reduced Temperature Range	IPP6R	Same condition with IDD6R
Auto Self Refresh Current	IDD6A	Commercial temperature : 0 to 95°C and Industrial temperature -40 to 95°C; LP ASR: Auto*4; CKE: L; External clock: off; CK_t and CK_c: L; CL: see Table 6; BL: 8*1; AL: 0; CS_n, command, address, bank group address, bank address, data I/O: H; DM_n: stable at 1; bank activity: auto self-refresh operation; Output buffer and RTT: enabled in MR*2; ODT signal: MID-LEVEL
Auto Self Refresh IPP Current	IPP6A	Same condition with IDD6A
Operating bank interleave read current	IDD7	CKE: H; External clock: on; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: see Table 6; BL: 8*1 ; AL: CL-1; CS_n: H between ACT and RDA; Command, address, bank group address, bank address Inputs: partially toggling according to Table 15; data I/O: read data bursts with different data between one burst and the next one according to Table 15; DM_n: stable at 1; bank activity: two times interleaved cycling through banks (0, 1, …7) with different addressing, see Table 15; output buffer and RTT: enabled in MR*2; ODT signal: stable at 0; pattern details: see Table 15
Operating Bank Interleave Read IPP Current	IPP7	Same condition with IDD7
Maximum Power Down Current	IDD8	TBD
Maximum Power Down IPP Current	IPP8	Same condition with IDD8

Notes:

1. Burst Length: BL8 fixed by MRS: MR0 bits [1,0] = [0,0].
2. MR: Mode Register
   Output buffer enable: set MR1 bit A12 = 0 and MR1 bits [2, 1] = [0,0]; output driver impedance control = RZQ/7
   RTT_Nom enable: set MR1 bits A[10:8] = [0,1,1]: RTT_Nom = RZQ/6
   RTT_WR enable: set MR2 bits A[11:9] = [0,0,1]: RTT_WR = RZQ/2
   RTT_PARK disable: set MR5 bits A[8:6] = [0,0,0]
3. CAL enabled:set MR4 bits A[8:6] = [0,0,1]: 1600MT/s; [0,1,0]: 1866MT/s, 2133MT/s; [0,1,1]: 2400MT/s
   Gear down mode enabled : set MR3 bit A3 = 1: 1/4 Rate
   DLL disabled: set MR1 bit A0 = 0
   CA parity enabled: set MR5 bits A[2:0] = [0,0,1]: 1600MT/s,1866MT/s, 2133MT/s [0,1,0]: 2400MT/s
   Read DBI enabled: set MR5 bit A12 = 1
   Write DBI enabled: set :MR5 bit A11 = 1
4. Low Power Array Self-Refresh (LP ASR) set MR2 bits A[7:6] = [0,0]: Normal; [0,1]: Reduced temperature range; [1,0]: Extended temperature range; [1,1]: Auto self-refresh
5. IDD2NG should be measured after sync pulse(NOP) input.

Table 8: IDD0, IDD0A and IPP0 Measurement-Loop Pattern[1]

CK_t /CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/ A15	WE_n/ A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			1,2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			3,4	D#, D#	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	-
			…	repeat pattern 1...4 until nRAS - 1, truncate if necessary																
			nRAS	PRE	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	-
			…	repeat pattern 1...4 until nRC - 1, truncate if necessary																
		1	1*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 1, BA[1:0] = 1 instead																
		2	2*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 2 instead																
		3	3*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 1, BA[1:0] = 3 instead																
		4	4*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 1 instead																
		5	5*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 1, BA[1:0] = 2 instead																
		6	6*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 3 instead																
		7	7*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 1, BA[1:0] = 0 instead																
		8	8*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 0 instead																For x4 and x8 only
		9	9*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 3, BA[1:0] = 1 instead																
		10	10*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 2 instead																
		11	11*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 3, BA[1:0] = 3 instead																
		12	12*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 1 instead																
		13	13*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 3, BA[1:0] = 2 instead																
		14	14*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 3 instead																
		15	15*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 3, BA[1:0] = 0 instead																

Notes:
1. DQS_t, DQS_c are VDDQ.
2. BG1 is don’t care for x16 device
3. C[2:0] are used only for 3DS device
4. DQ signals are VDDQ

Table 9: IDD1, IDD1A and IPP1 Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n_/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/BC_n	A[13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			1, 2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			3, 4	D#, D#	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	-
			...	repeat pattern 1...4 until nRCD - AL - 1, truncate if necessary																
			nRCD -AL	RD	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	**D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF**
			...	repeat pattern 1...4 until nRAS - 1, truncate if necessary																
			nRAS	PRE	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	-
			...	repeat pattern 1...4 until nRC - 1, truncate if necessary																
		1	1*nRC + 0	ACT	0	0	0	1	1	0	0	1	1	0	0	0	0	0	0	-
			1*nRC + 1, 2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			1*nRC + 3, 4	D#, D#	1	1	1	1	1	0	0	3[b]	3	0	0	0	7	F	0	-
			...	repeat pattern nRC + 1...4 until 1*nRC + nRAS - 1, truncate if necessary																
			1*nRC + nRCD - AL	RD	0	1	1	0	1	0	0	1	1	0	0	0	0	0	0	**D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00**
			...	repeat pattern 1...4 until nRAS - 1, truncate if necessary																
			1*nRC + nRAS	PRE	0	1	0	1	0	0	0	1	1	0	0	0	0	0	0	-
			...	repeat nRC + 1...4 until 2*nRC - 1, truncate if necessary																
		2	2*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 2 instead																
		3	3*nRC	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 3 instead																
		4	4*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 1instead																
		5	5*nRC	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 2instead																
		6	6*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 3 instead																
		8	7*nRC	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 0 instead																
		9	9*nRC	repeat Sub-Loop 1, use BG[1:0][2] = 2, BA[1:0] = 0instead																For x4 and x8 only
		10	10*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 3, BA[1:0] = 1instead																
		11	11*nRC	repeat Sub-Loop 1, use BG[1:0][2] = 2, BA[1:0] = 2 instead																
		12	12*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 3, BA[1:0] = 3instead																
		13	13*nRC	repeat Sub-Loop 1, use BG[1:0][2] = 2, BA[1:0] = 1instead																
		14	14*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 3, BA[1:0] = 2 instead																
		15	15*nRC	repeat Sub-Loop 1, use BG[1:0][2] = 2, BA[1:0] = 3 instead																
		16	16*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 3, BA[1:0] = 0instead																

Notes:

1. DQS_t, DQS_c are used according to RD Commands, otherwise VDDQ
2. BG1 is don't care for x16 device
3. C[2:0] are used only for 3DS device
4. Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are VDDQ

Table 10: IDD2N, IDD2NA, IDD2NL, IDD2NG, IDD2N_par, IPP2, IDD3N, IDD3NA, and IDD3P Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
			1	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
			2	D#, D#	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	0
			3	D#, D#	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	0
		1	4-7	repeat Sub-Loop 0, use BG[1:0]2 = 1, BA[1:0] = 1 instead																
		2	8-11	repeat Sub-Loop 0, use BG[1:0]2 = 0, BA[1:0] = 2 instead																
		3	12-15	repeat Sub-Loop 0, use BG[1:0]2 = 1, BA[1:0] = 3 instead																
		4	16-19	repeat Sub-Loop 0, use BG[1:0]2 = 0, BA[1:0] = 1 instead																
		5	20-23	repeat Sub-Loop 0, use BG[1:0]2 = 1, BA[1:0] = 2 instead																
		6	24-27	repeat Sub-Loop 0, use BG[1:0]2 = 0, BA[1:0] = 3 instead																
		7	28-31	repeat Sub-Loop 0, use BG[1:0]2 = 1, BA[1:0] = 0 instead																
		8	32-35	repeat Sub-Loop 0, use BG[1:0]2 = 2, BA[1:0] = 0 instead																
		9	36-39	repeat Sub-Loop 0, use BG[1:0]2 = 3, BA[1:0] = 1 instead																
		10	40-43	repeat Sub-Loop 0, use BG[1:0]2 = 2, BA[1:0] = 2 instead																
		11	44-47	repeat Sub-Loop 0, use BG[1:0]2 = 3, BA[1:0] = 3 instead																
		12	48-51	repeat Sub-Loop 0, use BG[1:0]2 = 2, BA[1:0] = 1 instead																
		13	52-55	repeat Sub-Loop 0, use BG[1:0]2 = 3, BA[1:0] = 2 instead																
		14	56-59	repeat Sub-Loop 0, use BG[1:0]2 = 2, BA[1:0] = 3 instead																
		15	60-63	repeat Sub-Loop 0, use BG[1:0]2 = 3, BA[1:0] = 0 instead																

Notes:
1. DQS_t, DQS_c are VDDQ
2. BG1 is don’t care for x16 device
3. C[2:0] are used only for 3DS device
4. DQ signals are VDDQ

Table 11: IDD2NT and IDDQ2NT Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_nA16	CAS_n/A15	WE_n/A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			1	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			2	D#, D#	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	-
			3	D#, D#	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	-
		1	4-7	repeat Sub-Loop 0, but ODT = 1 and BG[1:0][2] = 1, BA[1:0] = 1 instead																
		2	8-11	repeat Sub-Loop 0, but ODT = 0 and BG[1:0][2] = 0, BA[1:0] = 2 instead																
		3	12-15	repeat Sub-Loop 0, but ODT = 1 and BG[1:0][2] = 1, BA[1:0] = 3 instead																
		4	16-19	repeat Sub-Loop 0, but ODT = 0 and BG[1:0][2] = 0, BA[1:0] = 1 instead																
		5	20-23	repeat Sub-Loop 0, but ODT = 1 and BG[1:0][2] = 1, BA[1:0] = 2 instead																
		6	24-27	repeat Sub-Loop 0, but ODT = 0 and BG[1:0][2] = 0, BA[1:0] = 3 instead																
		7	28-31	repeat Sub-Loop 0, but ODT = 1 and BG[1:0][2] = 1, BA[1:0] = 0 instead																
		8	32-35	repeat Sub-Loop 0, but ODT = 0 and BG[1:0][2] = 2, BA[1:0] = 0 instead																For x4 and x8 only
		9	36-39	repeat Sub-Loop 0, but ODT = 1 and BG[1:0][2] = 3, BA[1:0] = 1 instead																
		10	40-43	repeat Sub-Loop 0, but ODT = 0 and BG[1:0][2] = 2, BA[1:0] = 2 instead																
		11	44-47	repeat Sub-Loop 0, but ODT = 1 and BG[1:0][2] = 3, BA[1:0] = 3 instead																
		12	48-51	repeat Sub-Loop 0, but ODT = 0 and BG[1:0][2] = 2, BA[1:0] = 1 instead																
		13	52-55	repeat Sub-Loop 0, but ODT = 1 and BG[1:0][2] = 3, BA[1:0] = 2 instead																
		14	56-59	repeat Sub-Loop 0, but ODT = 0 and BG[1:0][2] = 2, BA[1:0] = 3 instead																
		15	60-63	repeat Sub-Loop 0, but ODT = 1 and BG[1:0][2] = 3, BA[1:0] = 0 instead																

Notes:

1. DQS_t, DQS_c are VDDQ
2. BG1 is don't care for x16 device
3. C[2:0] are used only for 3DS device
4. DQ signals are VDDQ

Table 12: IDD4R, IDD4RA, IDD4RB and IDDQ4R Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	RD	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	**D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF**
			1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			2,3	D#, D#	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	-
		1	4	RD	0	1	1	0	1	0	0	1	1	0	0	0	7	F	0	**D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00**
			5	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			6,7	D#, D#	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	-
		2	8-11	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 2 instead																
		3	12-15	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 3 instead																
		4	16-19	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 1 instead																
		5	20-23	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 2 instead																
		6	24-27	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 3 instead																
		7	28-31	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 0 instead																
		8	32-35	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 0 instead																For x4 and x8 only
		9	36-39	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 1 instead																
		10	40-43	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 2 instead																
		11	44-47	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 3 instead																
		12	48-51	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 1 instead																
		13	52-55	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 2 instead																
		14	56-59	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 3 instead																
		15	60-63	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 0 instead																

Notes:

1. DQS_t, DQS_c are used according to RD Commands, otherwise VDDQ
2. BG1 is don't care for x16 device
3. C[2:0] are used only for 3DS device
4. Burst Sequence driven on each DQ signal by Read Command

Table 13: IDD4W, IDD4WA, IDD4WB and IDD4W_par Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	WR	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	**D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF**
			1	D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	-
			2,3	D#, D#	1	1	1	1	1	1	0	3[2]	3	0	0	0	7	F	0	-
		1	4	WR	0	1	1	0	1	1	0	1	1	0	0	0	7	F	0	**D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00**
			5	D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	-
			6,7	D#, D#	1	1	1	1	1	1	0	3[2]	3	0	0	0	7	F	0	-
		2	8-11	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 2 instead																
		3	12-15	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 3 instead																
		4	16-19	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 1 instead																
		5	20-23	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 2 instead																
		6	24-27	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 3 instead																
		7	28-31	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 0 instead																
		8	32-35	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 0 instead																For x4 and x8 only
		9	36-39	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 1 instead																
		10	40-43	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 2 instead																
		11	44-47	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 3 instead																
		12	48-51	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 1 instead																
		13	52-55	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 2 instead																
		14	56-59	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 3 instead																
		15	60-63	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 0 instead																

Notes:

1. DQS_t, DQS_c are used according to WR Commands, otherwise VDDQ
2. BG1 is don't care for x16 device
3. C[2:0] are used only for 3DS device
4. Burst Sequence driven on each DQ signal by Write Command

Table 14: IDD4WC Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	WR	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF D8=CRC
			1,2	D, D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	-
			3,4	D#, D#	1	1	1	1	1	1	0	3[2]	3	0	0	0	7	F	0	-
			5	WR	0	1	1	0	1	1	0	1	1	0	0	0	7	F	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00 D8=CRC
			6,7	D, D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	-
			8,9	D#, D#	1	1	1	1	1	1	0	3[2]	3	0	0	0	7	F	0	-
		2	10-14	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 2 instead																
		3	15-19	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 3 instead																
		4	20-24	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 1 instead																
		5	25-29	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 2 instead																
		6	30-34	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 3 instead																
		7	35-39	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 0 instead																
		8	40-44	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 0 instead																For x4 and x8 only
		9	45-49	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 1 instead																
		10	50-54	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 2 instead																
		11	55-59	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 3 instead																
		12	60-64	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 1 instead																
		13	65-69	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 2 instead																
		14	70-74	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 3 instead																
		15	75-79	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 0 instead																

Notes:

1. DQS_t, DQS_c are VDDQ
2. BG1 is don't care for x16 device
3. C[2:0] are used only for 3DS device
4. Burst Sequence driven on each DQ signal by Write Command

Table 15: IDD5B Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	REF	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
		1	1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			2	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			3	D#, D#	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	-
			4	D#, D#	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	-
			4-7	repeat pattern 1...4, use BG[1:0][2] = 1, BA[1:0] = 1 instead																
			8-11	repeat pattern 1...4, use BG[1:0][2] = 0, BA[1:0] = 2 instead																
			12-15	repeat pattern 1...4, use BG[1:0][2] = 1, BA[1:0] = 3 instead																
			16-19	repeat pattern 1...4, use BG[1:0][2] = 0, BA[1:0] = 1 instead																
			20-23	repeat pattern 1...4, use BG[1:0][2] = 1, BA[1:0] = 2 instead																
			24-27	repeat pattern 1...4, use BG[1:0][2] = 0, BA[1:0] = 3 instead																
			28-31	repeat pattern 1...4, use BG[1:0][2] = 1, BA[1:0] = 0 instead																
			32-35	repeat pattern 1...4, use BG[1:0][2] = 2, BA[1:0] = 0 instead																For x4 and x8 only
			36-39	repeat pattern 1...4, use BG[1:0][2] = 3, BA[1:0] = 1 instead																
			40-43	repeat pattern 1...4, use BG[1:0][2] = 2, BA[1:0] = 2 instead																
			44-47	repeat pattern 1...4, use BG[1:0][2] = 3, BA[1:0] = 3 instead																
			48-51	repeat pattern 1...4, use BG[1:0][2] = 2, BA[1:0] = 1 instead																
			52-55	repeat pattern 1...4, use BG[1:0][2] = 3, BA[1:0] = 2 instead																
			56-59	repeat pattern 1...4, use BG[1:0][2] = 2, BA[1:0] = 3 instead																
			60-63	repeat pattern 1...4, use BG[1:0][2] = 3, BA[1:0] = 0 instead																
		2	64 ... nRFC - 1	repeat Sub-Loop 1, Truncate, if necessary																

Notes:

1. DQS_t, DQS_c are VDDQ
2. BG1 is don’t care for x16 device
3. C[2:0] are used only for 3DS device
4. DQ signals are VDDQ

Table 16: IDD7 Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			1	RDA	0	1	1	0	1	0		0	0	0	0	1	0	0	0	**D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF**
			2	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			3	D#	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	-
			...	repeat pattern 2...3 until nRRD - 1, if nRRD > 4. Truncate if necessary																
		1	nRRD	ACT	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	-
			nRRD + 1	RDA	0	1	1	0	1	0		1	1	0	0	1	0	0	0	**D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00**
			...	repeat pattern 2 ... 3 until 2*nRRD - 1, if nRRD > 4. Truncate if necessary																
		2	2*nRRD	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 2 instead																
		3	3*nRRD	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 3 instead																
		4	4*nRRD	repeat pattern 2 ... 3 until nFAW - 1, if nFAW > 4*nRRD. Truncate if necessary																
		5	nFAW	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 1 instead																
		6	nFAW + nRRD	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 2 instead																
		7	nFAW + 2*nRRD	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 3 instead																
		8	nFAW + 3*nRRD	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 0 instead																
		9	nFAW + 4*nRRD	repeat Sub-Loop 4																
		10	2*nFAW	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 0 instead																For x4 and x8 only
		11	2*nFAW + nRRD	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 1 instead																
		12	2*nFAW + 2*nRRD	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 2 instead																
		13	2*nFAW + 3*nRRD	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 3 instead																
		14	2*nFAW + 4*nRRD	repeat Sub-Loop 4																
		15	3*nFAW	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 1 instead																
		16	3*nFAW + nRRD	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 2 instead																
		17	3*nFAW + 2*nRRD	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 3 instead																
		18	3*nFAW + 3*nRRD	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 0 instead																
		19	3*nFAW + 4*nRRD	repeat Sub-Loop 4																
		20	4*nFAW	repeat pattern 2 ... 3 until nRC - 1, if nRC > 4*nFAW. Truncate if necessary																

Notes:

1. DQS_t, DQS_c are VDDQ
2. BG1 is don't care for x16 device
3. C[2:0] are used only for 3DS device
4. Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are VDDQ

2. Electrical Specifications

2.1 IDD Specifications

IDD and IPP values are for full operating range of voltage and temperature unless otherwise noted. IDD and IPP values are for full operating range of voltage and temperature unless otherwise noted.

Table 17: IDD and IDDQ Specification

Parameter	Symbol	DDR4-3200	unit
		x16	
Operating current (ACT-PRE)	IDD0	82	mA
	IDD0A	82	mA
Operating current (ACT-RD-PRE)	IDD1	108	mA
	IDD1A	111	mA
Precharge Standby current	IDD2N	59	mA
	IDD2NA	59	mA
Precharge Standby ODT current	IDD2NT	79	mA
Precharge Standby Current with CAL enabled	IDD2NL	37	mA
Precharge Standby Current with Gear Down mode enabled	IDD2NG	58	mA
Precharge Standby Current with DLL disabled	IDD2ND	66	mA
Precharge Standby Current with CA parity enabled	IDD2N_par	70	mA
Precharge Power-Down Current	IDD2P	28	mA
Precharge quiet standby current	IDD2Q	37	mA
Active standby current	IDD3N	84	mA
Active Standby Current (AL=CL-1)	IDD3NA	85	mA
Active power-down current	IDD3P	45	mA
Operating current (Burst read operating)	IDD4R	278	mA
Operating Burst Read Current (AL=CL-1)	IDD4RA	300	mA
Operating Burst Read Current with Read DBI	IDD4RB	283	mA
Operating current (Burst write operating)	IDD4W	268	mA
Operating Burst Write Current(AL=CL-1)	IDD4WA	278	mA
Operating Burst Write Current with Write DBI	IDD4WB	269	mA
Operating Burst Write Current with Write CRC	IDD4WC	348	mA
Operating Burst Write Current with CA Parity	IDD4W_par	293	mA
Burst refresh current	IDD5B	148	mA
Burst Refresh Current (2X REF)	IDD5F2	132	mA
Burst Refresh Current (4X REF)	IDD5F4	117	mA
Self Refresh Current: Normal Temperature Range	IDD6N	19	mA
Self Refresh Current: Extended Temperature Range	IDD6E	30	mA
Self Refresh IPP Current: Reduced Temperature Range	IDD6R	8.5	mA
Auto Self Refresh Current	IDD6A	30	mA
All bank interleave read current	IDD7	256	mA
RESET low current	IDD8	21	mA

Note: Published IDD values are the maximum of the distribution of the arithmetic mean and are measured at 95 °C

Table 18: IPP Specification

Symbol	DDR4-3200	Unit	Note
	x16		
I_{PP0}	6	mA	
I_{PP1}	6	mA	
I_{PP2N}	1.2	mA	
I_{PP2P}	1.2	mA	
I_{PP3N}	1.2	mA	
I_{PP3P}	1.2	mA	
I_{PP4R}	1.2	mA	
I_{PP4W}	1.2	mA	
I_{PP5B}	36	mA	
I_{PP5F2}	31	mA	
I_{PP5F4}	24	mA	
I_{PP6N}	2.5	mA	
I_{PP6E}	3.7	mA	
I_{PP6R}	1.7	mA	
I_{PP6A}	3.7	mA	
I_{PP7}	34	mA	
I_{PP8}	1	mA	

Notes:

1. User should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR4 SDRAM devices support the following options or requirements referred to in this material.

Table 19: IDD6 Specification

Parameter	Symbol	Temperature Range	DDR4-3200	unit	Notes
			x16		
Self Refresh Current: Normal Temperature Range	IDD6N	0-85℃	19	mA	1
Self-Refresh Current: Extended Temperature Range	IDD6E	0-95℃	30	mA	2
Self-Refresh Current: Reduced Temperature Range	IDD6R	0-45℃	8.5	mA	3
Auto Self Refresh Current	IDD6A	0-95℃	30	mA	4

Notes:

1. Applicable for MR2 settings A6 = 0 and A7 = 0
2. Applicable for MR2 settings A6 = 0 and A7 =1 . IDD6E is only specified for devices which support the extended temperature range feature C[2:0] are used only for 3DS device
3. Applicable for MR2 settings A6 = 1 and A7 = 0. IDD6R is only specified for devices which support the reduced temperature range feature
4. Applicable for MR2 settings A6 = 1 and A7 = 0. IDD6A is only specified for devices which support the auto self-refresh feature

2.2 Pin Capacitance

Table 20: Silicon pad I/O Capacitance

Parameter	Symbol	DDR4-3200		Unit	NOTE
		min	max		
Input/output capacitance	C_{IO}	0.55	1.00	pF	1,2,3
Input/output capacitance delta	C_{DIO}	-0.1	0.1	pF	1,2,3,11
Input/output capacitance delta DQS_t and DQS_c	C_{DDQS}	-	0.05	pF	1,2,3,5
Input capacitance, CK_t and CK_c	C_{CK}	0.2	0.7	pF	1,3
Input capacitance delta CK_t and CK_c	C_{DCK}	-	0.05	pF	1,3,4
Input capacitance(CTRL, ADD, CMD pins only)	C_{I}	0.2	0.55	pF	1,3,6
Input capacitance delta(All CTRL pins only)	$C_{DI\_ CTRL}$	-0.1	0.1	pF	1,3,7,8
Input capacitance delta(All ADD/CMD pins only)	$C_{DI\_ADD\_CMD}$	-0.1	0.1	pF	1,2,9,10
Input/output capacitance of ALERT	C_{ALERT}	0.5	1.5	pF	1,3
Input/output capacitance of ZQ	C_{ZQ}	-	2.3	pF	1,3,12
Input capacitance of TEN	CTEN	0.2	2.3	pF	1,3,13

Notes:

1. This parameter is not subject to production test. It is verified by design and characterization. The silicon only capacitance is validated by de-embedding the package L & C parasitic. The capacitance is measured with VDD, VDDQ, VSS, VSSQ applied with all other signal pins floating. Measurement procedure TBDApplicable for MR2 settings A6 = 0 and A7 =1 . IDD6E is only specified for devices which support the extended temperature range feature C[2:0] are used only for 3DS device
2. DQ, DM_n, DQS_T, DQS_C, TDQS_T, TDQS_C. Although the DM, TDQS_T and TDQS_C pins have different functions, the loading matches DQ and DQS
3. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here
4. Absolute value CK_T-CK_C
5. Absolute value of CIO(DQS_T)-CIO(DQS_C)
6. CI applies to ODT, CS_n, CKE, A0-A15, BA0-BA1, BG0-BG1, RAS_n, CAS_n/A15, WE_n/A14, ACT_n and PAR
7. CDI CTRL applies to ODT, CS_n and CKE
8. CDI_CTRL = CI(CTRL)-0.5*(CI(CLK_T)+CI(CLK_C))
9. CDI_ADD_ CMD applies to, A0-A15, BA0-BA1, BG0-BG1,RAS_n, CAS_n/A15, WE_n/A14, ACT_n and PAR
10. CDI_ADD_CMD = CI(ADD_CMD)-0.5*(CI(CLK_T)+CI(CLK_C))
11. CDIO = CIO(DQ,DM)-0.5*(CIO(DQS_T)+CIO(DQS_C))
12. Maximum external load capacitance on ZQ pin: TBD pF
13. TEN pin is DRAM internally pulled low through a weak pull-down resistor to VSS

Table 21 : DRAM package electrical specifications(x16)

Symbol	Parameter	DDR4-3200		Unit	NOTE
		min	max		
Z_{IO}	Input/output Zpkg	45	85	W	1
T_{dIO}	Input/output Pkg Delay	14	45	ps	1
L_{io}	Input/Output Lpkg	-	3.4	nH	1, 2
C_{io}	Input/Output Cpkg	-	0.82	pF	1, 3
$Z_{IO\ DQS}$	DQS_t, DQS_c Zpkg	45	85	W	1
$Td_{IO\ DQS}$	DQS_t, DQS_c Pkg Delay	14	45	ps	1
$L_{io\ DQS}$	DQS Lpkg	-	3.4	nH	1, 2
$C_{io\ DQS}$	DQS Cpkg	-	0.82	pF	1, 3
$DZ_{DIO\ DQS}$	Delta Zpkg DQSU_t, DQSU_c	-	10	W	-
$D_{TdDIO\ DQS}$	Delta Delay DQSU_t, DQSU_c	-	5	ps	-
$Z_{I\ CTRL}$	Input- CTRL pins Zpkg	50	90	W	1
$T_{dI\_\ CTRL}$	Input- CTRL pins Pkg Delay	14	42	ps	1
$L_{i\ CTRL}$	Input CTRL Lpkg	-	3.4	nH	1, 2
$C_{i\ CTRL}$	Input CTRL Cpkg	-	0.7	pF	1, 3
$Z_{IADD\ CMD}$	Input- CMD ADD pins Zpkg	50	90	W	1
$Td_{IADD\_\ CMD}$	Input- CMD ADD pins Pkg Delay	14	52	ps	1
$L_{i\ ADD\ CMD}$	Input CMD ADD Lpkg	-	3.9	nH	1, 2
$C_{i\ ADD\ CMD}$	Input CMD ADD Cpkg	-	0.86	pF	1, 3
Z_{CK}	CLK_t & CLK_c Zpkg	50	90	W	1
Td_{CK}	CLK_t & CLK_c Pkg Delay	14	42	ps	1
$L_{i\ CLK}$	Input CLK Lpkg	-	3.4	nH	1, 2
$C_{i\ CLK}$	Input CLK Cpkg	-	0.7	pF	1, 3
DZ_{DCK}	Delta Zpkg CLK_t & CLK_c	-	10	W	-
D_{TdCK}	Delta Delay CLK_t & CLK_c	-	5	ps	-
Z_{OZQ}	ZQ Zpkg	-	100	W	-
$Td_{O\ ZQ}$	ZQ Delay	20	90	ps	-
$Z_{O\ ALERT}$	ALERT Zpkg	40	100	W	-
$Td_{O\ ALERT}$	ALERT Delay	20	55	ps	-

Notes:
1. Package implementations shall meet spec if the Zpkg and Pkg Delay fall within the ranges shown, and the maximum Lpkg and Cpkg do not exceed the maximum value shown
2. It is assumed that Lpkg can be approximated as Lpkg = Zo*Td
3. It is assumed that Cpkg can be approximated as Cpkg = Td/Zo

2.3 Standard Speed Bins

Table 22: DDR4-3200 Speed Bins and Operations

Speed Bin				DDR4-3200		Unit	NOTE
CL-nRCD-nRP				22-22-22			
Parameter			Symbol	min	max		
Internal read command to first data			tAA	13.75	18.00	ns	11
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min) + 4nCK	tAA(max) +4nCK	ns	11
ACT to internal read or write delay time			tRCD	13.75	-	ns	11
PRE command period			tRP	13.75	-	ns	11
ACT to PRE command period			tRAS	32	9 x tREFI	ns	11
ACT to ACT or REF command period			tRC	45.75	-	ns	11
	Normal	Read DBI					
CWL =9	CL = 9	CL = 11	tCK(AVG)	Reserved		ns	4
	CL = 10	CL = 12	tCK(AVG)	1.5	1.6	ns	1,2,3,10,15
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,10,15
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,10,15
CWL = 10,12	CL = 12	CL = 14	tCK(AVG)	Reserved		ns	4
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,10,15
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,10,15
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	Reserved		ns	4
	CL = 15	CL = 18	tCK(AVG)	0.937	<1.071	ns	1,2,3,10,15
	CL = 16	CL = 19	tCK(AVG)	0.937	<1.071	ns	1,2,3,10,15
CWL = 12,16	CL = 15	CL = 18	tCK(AVG)	Reserved		ns	4
	CL = 16	CL = 19	tCK(AVG)	Reserved		ns	4
	CL = 17	CL = 20	tCK(AVG)	0.833	<0.937	ns	1,2,3,10,15
	CL = 18	CL = 21	tCK(AVG)	0.833	<0.937	ns	1,2,3,10,15
CWL = 14,18	CL = 17	CL = 20	tCK(AVG)	Reserved		ns	4
	CL = 18	CL = 21	tCK(AVG)	Reserved		ns	4
	CL = 19	CL = 22	tCK(AVG)	0.75	<0.833	ns	1,2,3,10,15
	CL = 20	CL = 23	tCK(AVG)	0.75	<0.833	ns	1,2,3,10,15
CWL = 16, 20	CL = 20	CL = 24	tCK(AVG)	Reserved		ns	4
	CL = 21	CL = 25	tCK(AVG)	0.682	<0.75	ns	1,2,3,10,15
	CL = 22	CL = 26	tCK(AVG)	0.682	<0.75	ns	1,2,3,10,15
	CL = 24	CL = 28	tCK(AVG)	0.682	<0.75	ns	1,2,3,10,15
CWL = 16, 20	CL = 20	CL = 24	tCK(AVG)	Reserved		ns	4
	CL = 22	CL = 26	tCK(AVG)	0.625	<0.682	ns	1,2,3,10,15
	CL = 24	CL = 28	tCK(AVG)	0.625	<0.682	ns	1,2,3,10,15
Supported CL Settings				10,11,12,13,14,15,16,17,18,19,20,21,22,24		nCK	12,15
Supported CL Settings with read DBI				12,13,14,15,16,18,19,20,21,22,23,25,26,28		nCK	15
Supported CWL Settings				9,10,11,12,14,16,18,20		nCK	15

Speed Bin Table Notes

Absolute Specification

- VDDQ = VDD = 1.20V +/- 0.06 V
- VPP = 2.5V +0.25/-0.125 V
- The values defined with above-mentioned table are DLL ON case.

1. The CL setting and CWL setting result in tCK(avg).MIN and tCK(avg).MAX requirements. When making a selection of tCK(avg), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. tCK(avg).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK(avg) value (1.5, 1.25, 1.071, 0.938 or 0.833 ns) when calculating CL [nCK] = tAA [ns] / tCK(avg) [ns], rounding up to the next 'Supported CL', where tAA = 12.5ns and tCK(avg) = 1.3 ns should only be used for CL = 10 calculation.
3. tCK(avg).MAX limits: Calculate tCK(avg) = tAA.MAX / CL SELECTED and round the resulting tCK(avg) down to the next valid speed bin (i.e. 1.5ns or 1.25ns or 1.071 ns or 0.938 ns or 0.833 ns). This result is tCK(avg).MAX corresponding to CL SELECTED.
4. 'Reserved' settings are not allowed. User must program a different value.
5. 'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. Refer to supplier's data sheet and/or the DIMM SPD information if and how this setting is supported.
6. Any DDR4-2666 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
7. Any DDR4-3200 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
8. Parameters apply from tCK(avg)min to tCK(avg)max at all standard JEDEC clock period values as stated in the Speed Bin Tables.
9. CL number in parentheses, it means that these numbers are optional.
10. DDR4 SDRAM supports CL=9 as long as a system meets tAA(min).
11. Each speed bin lists the timing requirements that need to be supported in order for a given DRAM to be JEDEC compliant. JEDEC compliance does not require support for all speed bins within a given speed. JEDEC compliance requires meeting the parameters for a leas t one of the listed speed bins.
12. Supporting CL setting herewith is a reference base on JEDEC's. Precise CL & tCK setting needs to follow where defined on speed compatible table in section "Operating frequency", exceptional setting please confirm with NTC.CWL setting follow CL value in above table in section "Speed Bin"

2.4 tREFI

Average periodic Refresh interval (tREFI) of DDR4 SDRAM is defined as shown in the table.

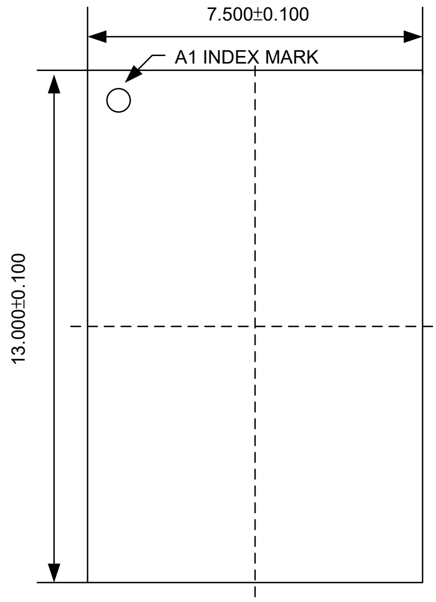
Table 23 : tREFI by device density

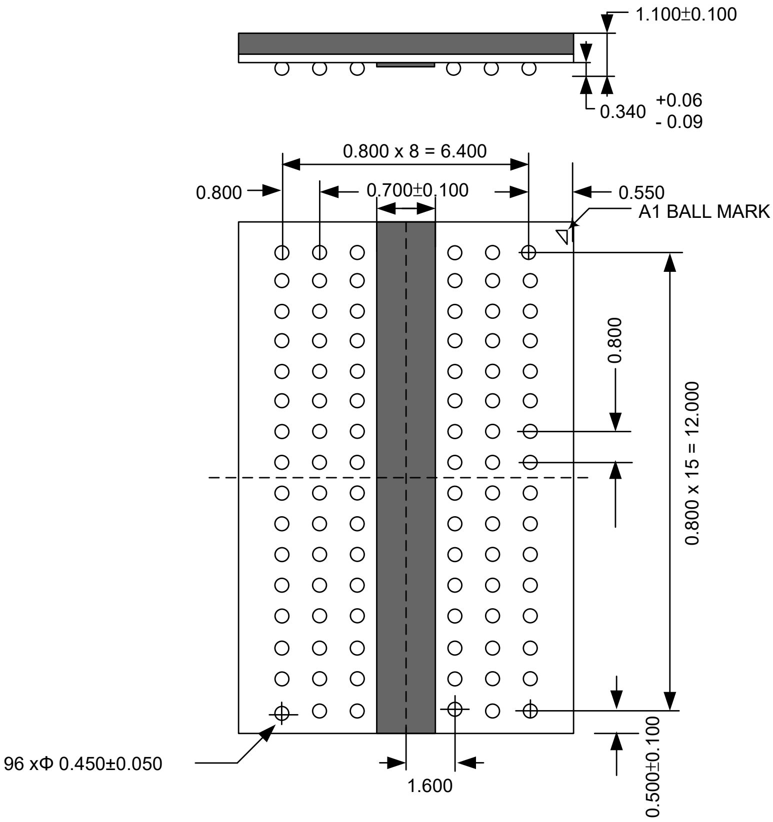
<table>
<tr><th>Refresh Mode</th><th colspan="2">Parameter</th><th>4 Gb</th><th>Unit</th></tr>
<tr><td></td><td colspan="2">tREFI(base)</td><td>7.8</td><td>us</td></tr>
<tr><td rowspan="3">1X mode</td><td rowspan="2">tREFI1</td><td>0ºC <= TCASE <= 85ºC</td><td>tREFI(base)</td><td>us</td></tr>
<tr><td>85ºC < TCASE <= 95ºC</td><td>tREFI(base)/2</td><td>us</td></tr>
<tr><td colspan="2">tRFC1(min)</td><td>260</td><td>ns</td></tr>
<tr><td rowspan="3">2X mode</td><td rowspan="2">tREFI2</td><td>0ºC <= TCASE <= 85ºC</td><td>tREFI(base)/2</td><td>us</td></tr>
<tr><td>85ºC < TCASE <= 95ºC</td><td>tREFI(base)/4</td><td>us</td></tr>
<tr><td colspan="2">tRFC2(min)</td><td>160</td><td>ns</td></tr>
<tr><td rowspan="3">4X mode</td><td rowspan="2">tREFI4</td><td>0ºC <= TCASE <= 85ºC</td><td>tREFI(base)/4</td><td>us</td></tr>
<tr><td>85ºC < TCASE <= 95ºC</td><td>tREFI(base)/8</td><td>us</td></tr>
<tr><td colspan="2">tRFC4(min)</td><td>110</td><td>ns</td></tr>
</table>

3. Package Drawing

3.1 96-ball FBGA

Solder ball: Lead free (Sn-Ag-Cu)   unit:mm





NOTES FOR CMOS DEVICES

① **PRECAUTION AGAINST ESD FOR MOS DEVICES**

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

② **HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES**

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

③ **STATUS BEFORE INITIALIZATION OF MOS DEVICES**

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.

No part of this document may be copied or reproduced in any form or by any means without the prior written consent of Kingston Technology Company, Inc.

Kingston Technology Company, Inc. does not assume any liability for infringement of any intellectual property rights (including but not limited to patents, copyrights, and circuit layout licenses) of Kingston Technology Company, Inc. or third parties by or arising from the use of the products or information listed in this document. No license, express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of Kingston Technology Company, Inc. or others.

Descriptions of circuits, software and other related information in this document are provided for illustrative purposes in semiconductor product operation and application examples. The incorporation of these circuits, software and information in the design of the customer's equipment shall be done under the full responsibility of the customer. Kingston Technology Company, Inc. assumes no responsibility for any losses incurred by customers or third parties arising from the use of these circuits, software and information.

[Product applications]
Be aware that this product is for use in typical electronic equipment for general-purpose applications. Kingston Technology Company, Inc. makes every attempt to ensure that its products are of high quality and reliability. However, this product is not intended for use in the product in aerospace, aeronautics, nuclear power, combustion control, transportation, traffic, safety equipment, medical equipment for life support, or other such application in which especially high quality and reliability is demanded or where its failure or malfunction may directly threaten human life or cause risk of bodily injury. Customers are instructed to contact Kingston Technology Company's sales office before using this product for such applications.

[Product usage]
Design your application so that the product is used within the ranges and conditions guaranteed by Kingston Technology Company, Inc., including the maximum ratings, operating supply voltage range, heat radiation characteristics, installation conditions and other related characteristics. Kingston Technology Company, Inc. bears no responsibility for failure or damage when the product is used beyond the guaranteed ranges and conditions. Even within the guaranteed ranges and conditions, consider normally foreseeable failure rates or failure modes in semiconductor devices and employ systemic measures such as fail-safes, so that the equipment incorporating Kingston Technology Company, Inc. products does not cause bodily injury, fire or other consequential damage due to the operation of the Kingston Technology Company, Inc. product.

[Usage environment]
Usage in environments with special characteristics as listed below was not considered in the design. Accordingly, our company assumes no responsibility for loss of a customer or a third party when used in environments with the special characteristics listed below.

Example:

1) Usage in liquids, including water, oils, chemicals and organic solvents.
2) Usage in exposure to direct sunlight or the outdoors, or in dusty places.
3) Usage involving exposure to significant amounts of corrosive gas, including sea air, CL_2, H_2S, NH_3, SO_2, and NOx.
4) Usage in environments with static electricity, or strong electromagnetic waves or radiation.
5) Usage in places where dew forms.
6) Usage in environments with mechanical vibration, impact, or stress.
7) Usage near heating elements, igniters, or flammable items.

If you export the products or technology described in this document that are controlled by the Foreign Exchange and Foreign Trade Law of Taiwan, you must follow the necessary procedures in accordance with the relevant laws and regulations of Taiwan. Also, if you export products/technology controlled by U.S. export control regulations, or another country's export control laws or regulations, you must follow the necessary procedures in accordance with such laws or regulations.
If these products/technology are sold, leased, or transferred to a third party, or a third party is granted license to use these products, that third party must be made aware that they are responsible for compliance with the relevant laws and regulations.

Contact Kingston

For more information, visit us at: https://www.kingston.com/en/solutions/embedded-and-industrial

For direct support, please contact us at: https://www.kingston.com/en/form/embedded

For quick questions, please email us at: emmc@kingston.com