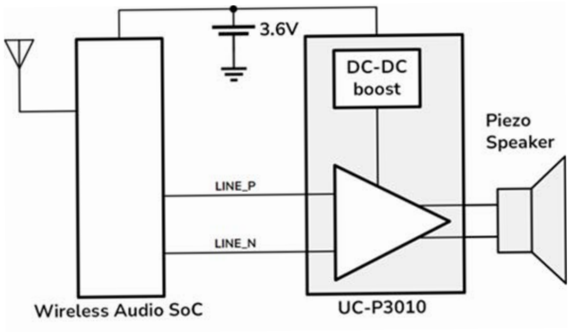
PIEZO SPEAKER
ASIC LINEAR AMPLIFIER

TARVOS 1.0 UC-P3010 | DATASHEET



UC-P3010 application example

Tarvos 1.0 UC-P3010 is a high-voltage ASIC linear audio amplifier designed for a 3.6 V supply voltage, such as Li-Ion batteries. With less than a 1 mA quiescent current draw, it significantly reduces power consumption. Its analog audio input is compatible with the analog audio outputs of the most common Bluetooth audio SoCs.

At ultrasound frequencies Tarvos's linear amplification allows the use of advanced signal modulation and windowing techniques.

FEATURES

- Class H-amplifier
- Frequency range 20 Hz- 80 kHz
- Output voltage range of up to 27 V_{PP} within 20 Hz-80 kHz
- Available gains: 18, 24, 30 dB
- Sub-mA quiescent current draw from a 3.6 V supply
- THD+N < 0.2% at 1 kHz
- SNR > 103 dB
- Integrated DC-DC Boost converter
- Build in DC bias voltage source
- Load capacitance up to 50 nF
- In a compact 16-balls 2x2 mm^2 WLSCP package

APPLICATIONS

Designed for capacitive loads, Tarvos 1.0 is the ideal solution for integrating USound MEMS speakers and other piezo transducers in a wide range of audio products, such as true wireless earphones, over-the-counter (OTC) hearing aids, and wideband ultrasonic applications.

Released in March 2023 | Updated in August 2024

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CONTENT

REVISION HISTORY

March 2023: First release

July 2023: updated pages 4, 5; 7; 10

September 2023: updated page 4

December 2023: updated page 4; page 8

June 2024: updated page 4, 5; 9; 10

August 2024: updated page 1, 6, 9

U))) SOUND

WLCSP BGA PINOUT

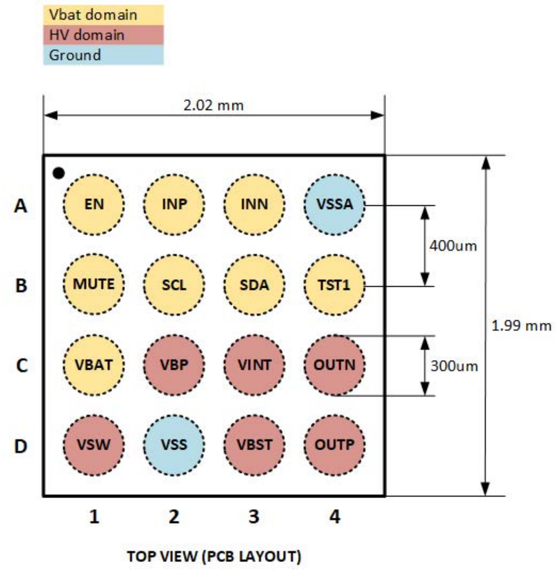


Figure 1: **WLCSP BGA pinout including the chip dimensions.**

Pin	Name	Function
A1	EN	Enable/disable
A2	INP	Amplifier input positive
A3	INN	Amplifier input negative
A4	VSSA	Signal ground
B1	MUTE	MUTE pin
B2	SCL	I2C clock (Factory Programming only)
B3	SDA	I2C data (Factory Programming only)
B4	TST1	Test pin
C1	VBAT	Power supply
C2	VBP	MEMS DC bias
C3	VINT	Internal voltage (NC)
C4	OUTN	Amplifier output negative
D1	VSW	Boost converter switching mode
D2	VSS	Power ground
D3	VBST	Boost converter output
D4	OUTP	Amplifier output positive

ABSOLUTE MAXIMUM RATINGS (NON-OPERATING)

Stress beyond the absolute maximum ratings will reduce the lifetime or cause permanent damage to the device. Functional operation is guaranteed only under the conditions listed in “Operating conditions”.

Parameter	Min	Max	Unit
Junction Temperature		150	˚C
Storage Temperature	-55	150	˚C
Power supply (VBAT)	-0.3	5.5	V
ESD – Human Body Model (JEDEC JS-001)		2000[1]	
ESD – Charged Device Model (JEDEC JS-002)		500[1]	

[1] For all pins on the VBAT domain

OPERATING CONDITIONS

Parameter	Min	Typ	Max	Unit
Junction Temperature	-20	25	125	˚C
Storage Temperature	-20	25	85	˚C
Power supply (VBAT)	2.7	3.6	5.5	V

IBAT CHARACTERISTICS

Conamara MEMS speaker series as load, V_{BAT}=3.6 V, T_{AMB}=25˚C, H-configuration.

Parameter	Min	Typ	Max	Unit	Conditions
Quiescent supply current		0.98		mA	V_{AC}= 0 V, V_{BST}= 14 V
Shutdown current			0.5	µA	EN=0
Supply current H-configuration		5.91		mA	V_{AC}= 27 V_{PP} @ 1 kHz [2], V_{BST}= 14 V, V_{BP} = 10 V
		0.99			V_{AC}= 2.9 V_{PP} @ 1 kHz [3], V_{BST}= 14 V, V_{BP} = 10 V
		1.04			V_{AC}= 1,24 V_{RMS} IEC 60268-1 noise, crest factor 12 dB [3], V_{BST}= 14 V, V_{BP} =10 V
		2.27			V_{AC}= 3,37 V_{RMS} EN 50332-1 noise, crest factor 6 dB [4], V_{BST}= 14 V, V_{BP}= 10 V

Please note, that the VBP refers to the V_{DC}, used in the speaker datasheet.

[2] Maximum dBSPL, Conamara UA-C0603-3F in IEC 60318-4 Coupler ('711')
[3] 94 dBSPL, Conamara UA-C0603-3F in IEC 60318-4 Coupler ('711')
[4] 103 dBSPL, Conamara UA-C0603-3F in IEC 60318-4 Coupler ('711')

Ganymede MEMS speaker series as load, V_{BAT}=3.6 V, T_{AMB}=25°C, G-configuration.

Parameter	Min	Typ	Max	Unit	Conditions
Quiescent supply current		0.98		mA	V_{AC}= 0 V, V_{BST}= 14 V
Shutdown current			0.5	µA	EN= 0
Supply current G-configuration		12.2		mA	V_{AC}= 27 V_{PP} @ 1 kHz [5], V_{BST}=14 V, V_{BP}= 14V
		1.13			V_{AC}= 2.8 V_{PP} @ 1 kHz [6], V_{BST}= 14 V, V_{BP}= 14 V
		1.17			V_{AC}= 1.0 V_{RMS} IEC 60268-1 noise, crest factor 12 dB [6], V_{BST}= 14 V, V_{BP}= 14 V
		2.48			V_{AC}= 2.8 V_{RMS} EN 50332-1 noise, crest factor [6] dB [7], V_{BST}= 14 V, V_{BP}= 14 V

The V_{BP} voltage refers to the V_{DC} used in the speaker datasheet.

[5] Maximum dBSPL, Achelous UT-P2020 in IEC 60318-4 Coupler (711)
[6] 94 dBSPL, Achelous UT-P2020 in IEC 60318-4 Coupler (711)
[7] 103 dBSPL, Achelous UT-P2020 in IEC 60318-4 Coupler (711)

CONTROL INPUT PINS

Parameter	Min	Typ	Max	Unit	Comments
Input low level	0		0.4	V	1.8 V and V_{BAT} logic threshold compatible
Input high level	1.2		V_{BAT}	V	1.8 V and V_{BAT} logic threshold compatible
Voltage range	0		V_{BAT}	V	

AC AUDIO CHARACTERISTICS

Unless otherwise specified: Conamara MEMS speaker as a load, V_{BAT}=3.6 V, T_{AMB}=25ºC.

Parameter	Min	Typ	Max	Unit	Conditions
Load capacitance	0		50	nF	For unconditional stability
Input differential voltage			3	V_{PP}	See Note 1 below
Input differential resistance		10		kΩ	Resistance between the input pins INP and INN, Gain = 30 dB
		20			Resistance between the input pins INP and INN, Gain = 24 dB
		40			Resistance between the input pins INP and INN, Gain = 18 dB
Gain		18		dB	
		24			
		30			
Output Noise (A-Weighted, 20 Hz-20 kHz)		63.4			AC grounded inputs INP and INN, at 30 dB gain
		50.0			AC grounded inputs INP and INN, at 24 dB gain
		42.8			AC grounded inputs INP and INN, at 18 dB gain
Signal to Noise Ratio		103.0	42.8	dB	A-Weighted, 20 Hz-20 kHz, Fout=1 kHz, V_{AC}=27 V_{PP}, at 30 dB gain
		105.4	42.8		A-Weighted, 20 Hz-20 kHz, Fout=1 kHz, VAC=27 V_{PP}, at 24 dB gain
		106.9	42.8		A-Weighted, 20 Hz-20 kHz, Fout=1 kHz, V_{AC}=27 V_{PP}, at 18 dB gain
Total Harmonic Distortion		0.2		%	Fout=1 kHz, V_{AC}=27 V_{PP}, at any gain
Output voltage			27		With THD ≤ 0.4%

Note 1: To keep the THD within specification, please guarantee V_{IN} to be maximum 0.80 V_{PP} for 30 dB gain, 1.6 V_{PP} for 24 dB gain and 3 V_{PP} for 18 dB gain.

THEORY OF OPERATION

Tarvos 1.0 features a Low Noise Amplifier to deliver a low noise voltage to the AB output stage. The output stage is based on a differential topology and is assisted by a Dynamic Power Control block, that analyses the audio signal and decides on how to efficiently use the battery charge. In case of audio signal voltage peaks, the Dynamic Power Control supplies the amplifier from the DC-DC boost converter. In the absence of the high peaks, the current flows directly from VBAT.
The common-mode distortion added by DPC, is canceled out due to the differential architecture of the amplifier.

Tarvos 1.0 has a DC bias source that provides a voltage output that improves the performance of USound MEMS speakers. The LBAT sensing circuit will detect if the battery level is under 3.0 V and reduce the amplifier's gain by 6 dB, which will reduce the current drawn from VBAT.

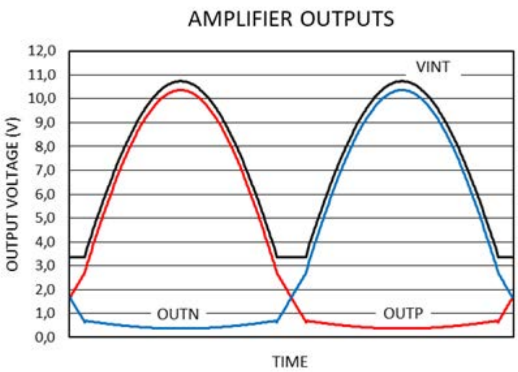


Figure 2: **Single-ended outputs.**

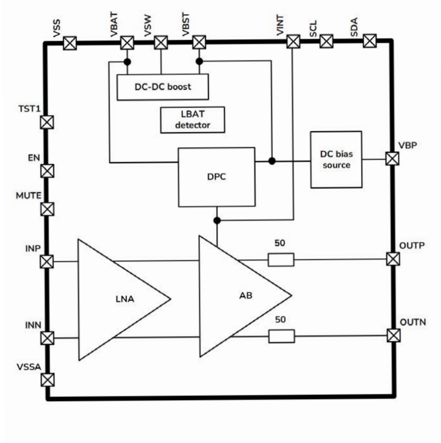


Figure 3: **UC-P3010 block diagram.**

PERFORMANCE PLOTS

All below measurement results were obtained with the circuit shown in Figure 9.
Large-Signal frequency response measured at output amplitude 27 V_{PP} with a Conamara MEMS speaker as load (Figure 4 and Figure 5). Total Harmonic Distortion + Noise (with a measurement bandwidth up to 20 kHz) measured at output amplitude 27 V_{PP} with a Conamara MEMS speaker as a load across the frequency range (Figure 6).

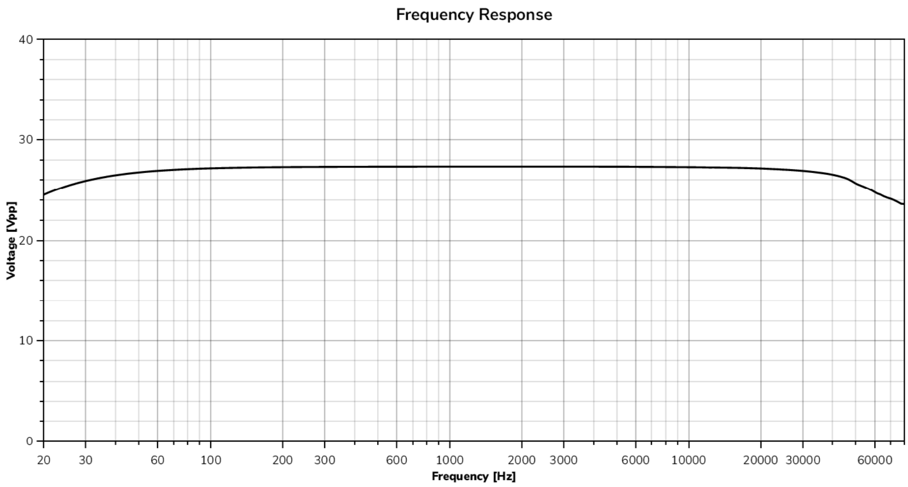


Figure 4: **Output Voltage vs frequency.**

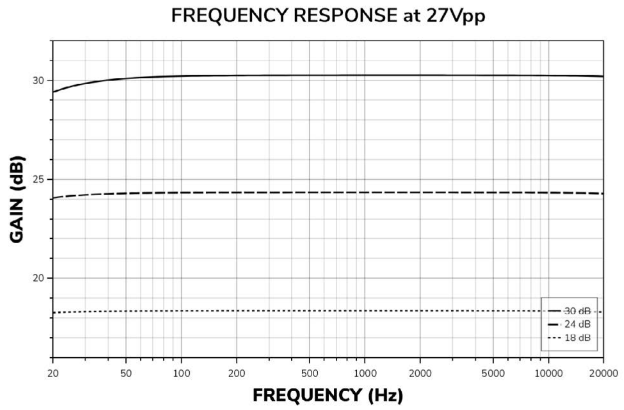


Figure 5: **Gain vs frequency.**

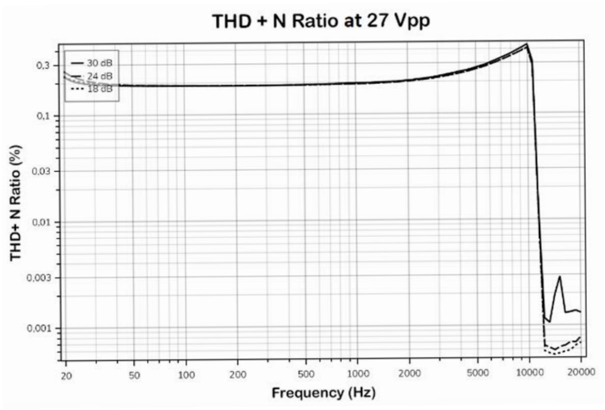


Figure 6: **THD+N responses vs. frequency.**

Total Harmonic Distortion + Noise measured at 1 kHz with a Conamara MEMS speaker as load, is < 0.2% across the amplitude range, indicating low cross-over distortion at low signal amplitude and across the power control envelope (Figure 7).

Output RMS Noise is measured with gains 18 dB, 24 dB and 30 dB with both inputs INP and INN connected to VSS through the input capacitors. A-weighting filter is included in the post-processing and the RMS value of the consecutive readouts is plotted in Figure 8. This reflects in noise under 12 dB SPL A-weighted acoustic noise with any USound MEMS speaker.

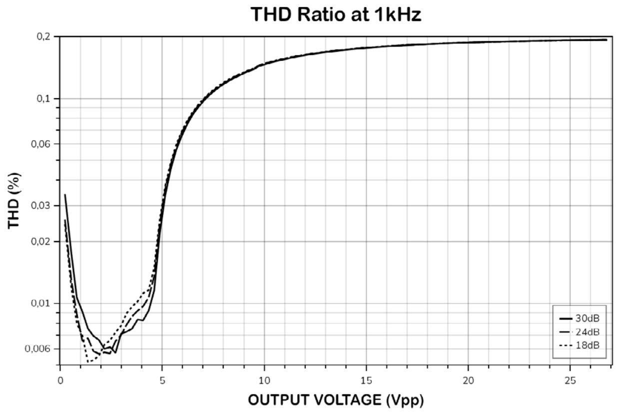


Figure 7: **THD+N responses vs. amplitude.**

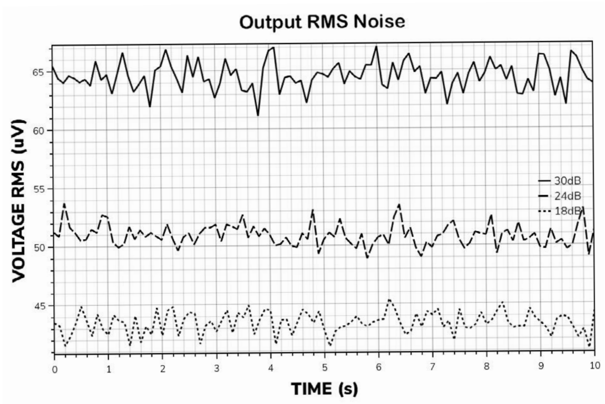


Figure 8: **Output RMS noise readouts.**

ACOUSTIC NOISE PERFORMANCE

Calculated acoustic noise based on the speaker sensitivity and the measured output electrical noise in IEC 60318-4 Coupler ('711'). (SPL units in dBA).

Product code/Gain	18 dB	24 dB	30 dB
UT-P2020	6.6	8.0	10.0
UT-P2023	6.6	8.0	10.0
UA-C0503-3T	7.3	8.6	10.7
UA-C0603-3F	4.5	5.8	7.9

TYPICAL APPLICATION SCHEMATIC

The analog outputs of a typical aAudio (Bluetooth) SoC processor are connected to the input of Tarvos 1.0 UC-P3010 through two DC blocking capacitors.

The input capacitors C6 and C7, as well as the output capacitors C4 and C5 linearity (change of capacitance over voltage) areis important for minimal contribution to the THD.

The recommended maximum output voltage of Tarvos 1.0 UC-P3010 depends on the given V_{BST} level:

$$V_{Out\_Max}(V_{PP}) = 2 \cdot VBST - 1$$

For example, for VBST= 14 V, the recommended maximum output voltage is 27 V_{PP}.

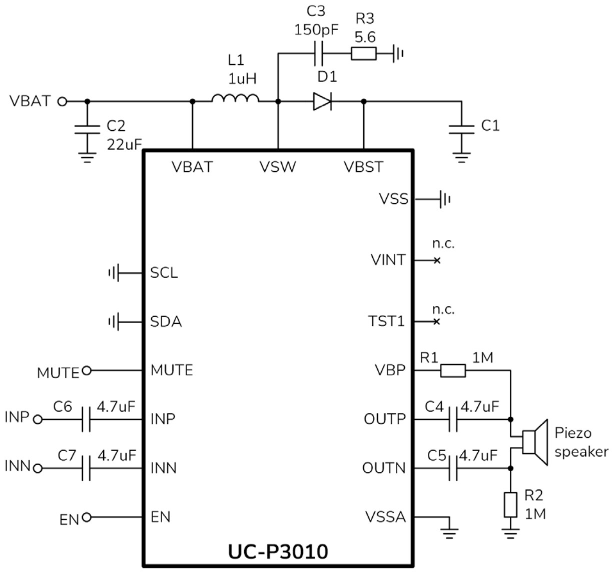


Figure 9: **Application schematic (differential input).**

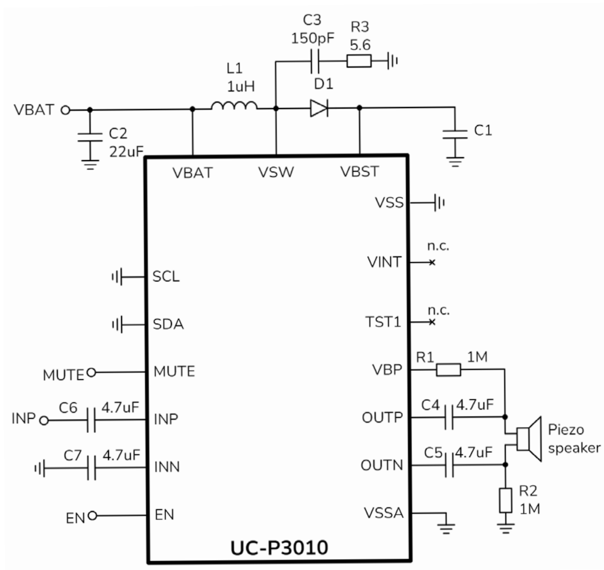


Figure 10: **Figure 10: Application schematic (single-ended input).**

DESIGN REQUIREMENTS

SELECTION OF EXTERNAL COMPONENTS

1. V_{BST} and output capacitor selection

The Tarvos boost converter reservoir capacitor (C1 in **Figure 9**) needs to fulfill one of two requirements:

- One capacitor with minimum voltage rating of 25 V and at least 9 µF capacitance
- Two capacitors in parallel with a minimum voltage rating of 25 V and 4.7 µF capacitance

C3 must have a higher voltage rating and is widely available with 50 V rating.
The recommended capacitance for the output capacitors (C4 and C5 in **Figure 9**) is 4.7 µF with an at least 25 V rating and a temperature coefficient of X5R or better.

2. Input capacitors selection

The DC block input capacitors (C6, C7), see **Figure 9**, form a high pass filter with the internal resistance of Tarvos 1.0 that removes the DC bias from an incoming signal. Assuming an ideal scenario with a negligible source impedance, the cut-off frequency (3 dB point) of the high pass filter is given by:

$$f_{-3dB} = \frac{1}{2\pi CR}$$

where C is the capacitance of C6 or C7, and R is the differential internal resistance divided by two (i.e. for 18 dB gain, R=20 kΩ).

3. Diode (D1) selection

A Schottky diode (D1 in **Figure 9**) is necessary for the boost converter. The peak current rating required for this diode is at least 1.5 A for repetitive peak time ≤ 500 ns and duty cycle ≤ 35%. The voltage rating required for this diode is at least 20 V reverse voltage. To optimize the efficiency of the DC-DC boost converter, the recommended leakage current should be below 10 µA at 20 V. The Nexperia PMEG4010ESBYL is recommended.

4. Inductor (L1) selection

The required inductor for the boost converter (L1 in **Figure 9**) must have an inductance of 1 µH and its saturation current must be higher than 1.5 A. Therefore, Taiyo Yuden LSCNA1608FKT1R0MA is recommended. Other inductors with equal or higher saturation current, while having a DCR<250 mΩ (series resistance) to minimize efficiency losses, are appropriate.

LAYOUT GUIDELINE

A low-impedance compact PCB layout design is required in the DC-DC part. This includes the pins VSW, VSS, VBST, the inductor L1 and the Schottky diode D1. Design a short and wide connection for VSW (L1-D1) and VBAT, especially in the connectivity of the boost diode (D1), boost Inductor (L1), boost capacitor (C1) and VBAT bypass capacitor (C2).

Components C3 and R3 require a very short and wide connection as well to function appropriately. The unused pins B2 and B3 should be grounded. The unused pins C3 and B4 should be floating.

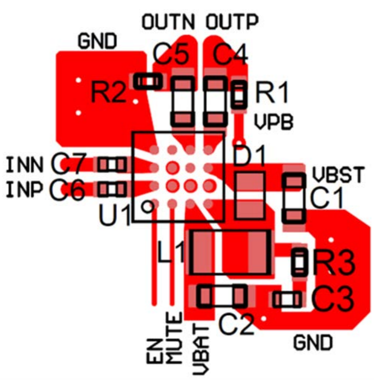


Figure 11: **Recommended PCB layout with DC bias.**

ADDITIONAL APPLICATION

With Tarvos 1.0,piezo speakers can be driven without DC bias voltage. The information about this application is presented in Figure 12 and Figure 13.

SCHEMATIC

The differential outputs of up to 3 V_{PP} are connected to the input of Tarvos 1.0 UC-P3010 through two DC blocking capacitors.

The input capacitors C6 and C7 linearity (change of capacitance over voltage) is important for minimal contribution to the THD.

The recommended maximum output voltage of Tarvos 1.0 UC-P3010 depends on the given VBST level:

$$V_{Out\_Max}(V_{PP}) = 2 \cdot VBST - 1$$

For example, for V_{BST}= 14 V, the recommended maximum output voltage is 27 V_{PP}.

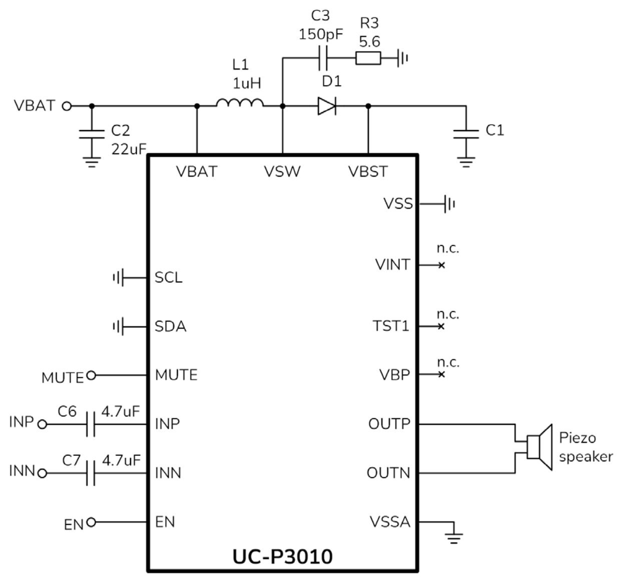


Figure 12: **Application schematic (differential input) without DC bias.**

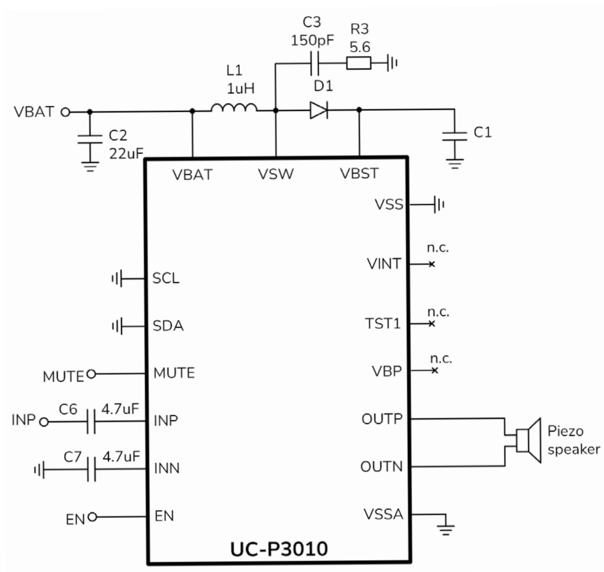


Figure 13: **Application schematic (single-ended input) without DC bias.**

SELECTION OF EXTERNAL COMPONENTS

1. V_{BST} and output capacitor selection

The Tarvos boost converter reservoir capacitor (C1 in Figure 12) needs to fulfill one of two requirements:

- One capacitor with minimum 25 V rating and at least 9 μF capacitance
- Two capacitors in parallel with minimum 25 V rating and 4.7 μF capacitance

C3 must have a higher voltage rating and can be easily found with 50 V rating.

2. Input capacitors selection

The DC block input capacitors (C6, C7), see Figure 12, form a high pass filter with the internal resistance of Tarvos 1.0 that removes the DC bias from an incoming signal. Assuming an ideal scenario with a negligible source impedance, the cut-off frequency (3 dB point) of the high pass filter is given by:

$$f_{-3dB} = \frac{1}{2\pi C R}$$

where C is the capacitance of C6 or C7, and R is the differential internal resistance divided by two (i.e. for 18 dB gain, R=20 kΩ).

3. Inductor (L1) selection

The required inductor for the boost converter (L1 in Figure 12) must have an inductance of 1 μH and its saturation current must be higher than 1.5 A. Therefore, Taiyo Yuden LSCNA1608FKT1R0MA is recommended. Other inductors with equal or higher saturation current, while having a DCR<250 mΩ (series resistance) to minimize efficiency losses, are appropriate.

LAYOUT GUIDELINE

Low-impedance compact PCB layout design is required in the DC-DC part. This includes the pins VSW, VSS, VBST, the inductor L1 and the Schottky diode D1. Design a short and wide connection for VSW (L1-D1) and VBAT, especially in the connectivity of the boost diode (D1), boost Inductor (L1), boost capacitor (C1) and VBAT bypass capacitor (C2).

Components C3 and R3 require a very short and wide connection as well to function appropriately.
The unused pins B2 and B3 should be grounded. The unused pins C2, C3 and B4 should be floating.

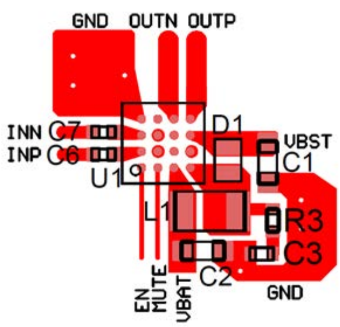
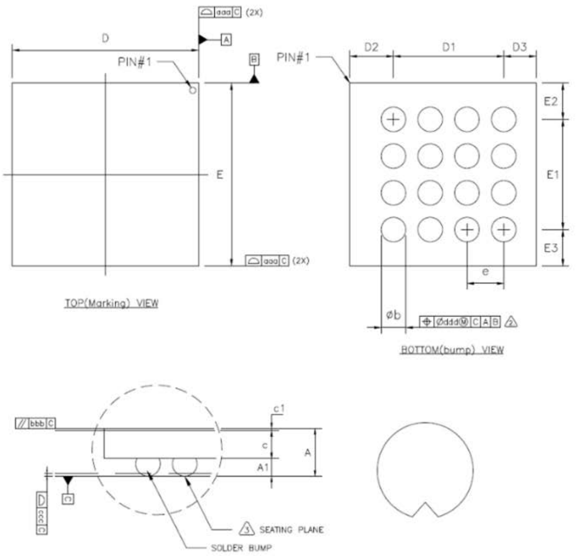


Figure 14: Recommended PCB layout without DC bias.

PACKAGE DRAWING



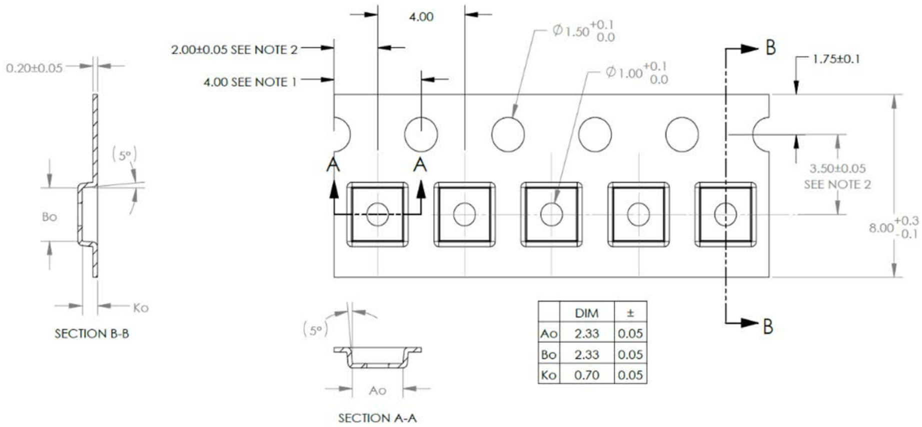
Symbol	Dimensions in mm			Dimensions in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.4716	0.5190	0.5664	0.0186	0.0204	0.0223
A1	0.1746	0.1940	0.2134	0.0069	0.0076	0.0084
c1	0.0220	0.0250	0.0280	0.0009	0.0010	0.0011
c	0.2750	0.3000	0.3250	0.0108	0.0118	0.0128
D	1.9990	2.0265	2.0540	0.0787	0.0798	0.0809
E	1.9650	1.9925	2.0200	0.0774	0.0784	0.0795
b	0.2278	0.2680	0.3082	0.0090	0.0106	0.0121
D1	---	1.2000	---	---	0.0472	---
D2	---	0.4753	---	---	0.0187	---
D3	---	0.3513	---	---	0.0138	---
E1	---	1.2000	---	---	0.0472	---
E2	---	0.3963	---	---	0.0156	---
E3	---	0.3963	---	---	0.0156	---
e	---	0.4000	---	---	0.0157	---
aaa	---	0.0275	---	---	0.0011	---
bbb	---	0.1000	---	---	0.0039	---
ccc	---	0.0300	---	---	0.0012	---
ddd	---	0.1500	---	---	0.0059	---

Figure 15: **Package dimensions.**

Notes:

1. Controlling dimensions: Millimetre.
2. Dimension is measured at the maximum ball diameter, parallel to primary datum c.
3. Primary datum c and seating plane are defined by the spherical crowns of the solder balls.

TAPE AND REEL



	DIM	±
Ao	2.33	0.05
Bo	2.33	0.05
Ko	0.70	0.05

Figure 16: **Pocket and part dimensions.**

Notes:

1. 10 sprocket hole pitch cumulative tolerance ±0.2 mm.
2. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

ORDERING INFORMATION

Available configurations for USound MEMS speakers: G for Ganymede series and H for Conamara series.

Product code	Description	MOQ
UC-P3010-G18	Tarvos ASIC linear amplifier G-configuration for Ganymede series UT-P2020, UT-P2023, UT-P2016, gain 18 dB	2.5 k
UC-P3010-G24	Tarvos ASIC linear amplifier G-configuration for Ganymede series UT-P2020, UT-P2023,UT-P2016, gain 24 dB	2.5 k
UC-P3010-G30	Tarvos ASIC linear amplifier G-configuration for Ganymede series UT-P2020, UT-P2023, UT-P2016, gain 30 dB	2.5 k
UC-P3010-H18	Tarvos ASIC linear amplifier H-configuration for Conamara series UA-C0503-3T, UA-C0603-3T, UA-C0603-3F, gain 18 dB	2.5 k
UC-P3010-H24	Tarvos ASIC linear amplifier H-configuration for Conamara series UA-C0503-3T, UA-C0603-3T, UA-C0603-3F, gain 24 dB	2.5 k
UC-P3010-H30	Tarvos ASIC linear amplifier H-configuration for Conamara series UA-C0503-3T, UA-C0603-3T, UA-C0603-3F , gain 30 dB	2.5 k
UC-P3010 custom	Tarvos ASIC linear amplifier with custom configuration/ NRE costs apply	6 k

COMPATIBLE PRODUCTS

Product Name	Description
Tarvos evaluation board 1.0 UC-E3010	Evaluation board for testing key features of the USound ASIC linear audio amplifier
Achelous UT-P2020	MEMS speaker for in-ear audio solution, hearables, full-bandwidth, rectangular (Ganymede series)
Achelous UT-P2016	MEMS speaker for in-ear audio solution, hearables, full-bandwidth, rectangular and plastic cover (Ganymede series)
Adap UT-P2023	MEMS speaker for free-field applications, rectangular (Ganymede series)
Conamara UA-C0503-3T	MEMS speaker for 2-way speaker solution in wearables and hearables, tweeter, 5 mm diameter
Conamara UA-C0603-3T	MEMS speaker for 2-way speaker solution in wearables and hearables, tweeter, 6 mm diameter
Conamara UA-C0603-3F	MEMS speaker for wearables and hearables, full bandwidth, 6 mm diameter

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