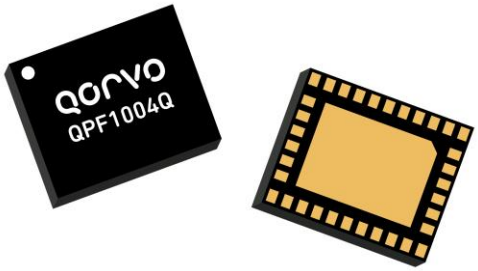
Product Status

Preview: This product has been announced but is not yet in full production. Specifications are subject to change based on final AEC-Q product qualification. Samples may or may not be available. Please contact your Qorvo representative for the latest product status and performance data.

PRELIMINARY
QPF1004Q
5GHz C-V2X/DSRC/Wi-Fi FEM

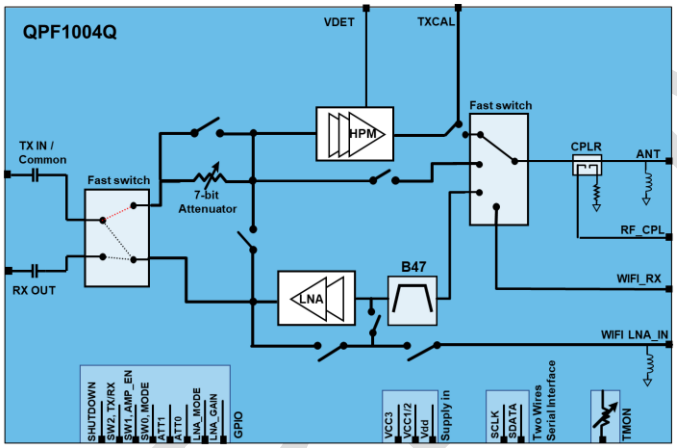
Product Overview

The QPF1004Q AEC-Q100 qualified is an integrated front end module (FEM) designed to support multi-Standard systems such as C-V2X, DSRC/11p and Wi-Fi. The FEM integrates a wide bandwidth PA and LNA along with fast T/R switching, B47 BAW, RF Coupler, Analog Temperature Sensor, and a high dynamic range Digital Step Attenuator (DSA) for use in both the TCU and Compensator mode accessible from both TX and RX paths. The QPF1004Q offers GPIO and Serial control interfaces for critical functions as well as a calibration mode to measure cable loss. Both transmit and receiver paths include high gain and bypass states for wide dynamic range operation.
The combination of package size, high level of integration and minimal external components significantly reduces layout area in the application. The QPF1004Q architecture control interface are optimized for next generation Automotive wireless systems.



34-Pin 4.5x5.5x0.64 mm Laminate Package

Functional Block Diagram



Key Features

- AEC-Q100 Grade 2 target
- High Output Power >29dBm, C-V2X mode
- DSRC/11p Pout = +26dBm, Class C Mask
- Integrated BAW with bypass
- Integrated Attenuator and PA with bypass
- 33dB TX Gain
- Integrated Analog Temperature Sensor
- 2.1 dB RX Noise Figure (LNA+Input switch)
- 26 dB Rx Gain in unfiltered path
- Dual GPIO and Serial control interfaces
- Optimized for +5V Operation

Applications

- ITS C-V2X, B47
- DSRC/11p Applications
- Wi-Fi Infotainment
- Automotive Telematics

Ordering Information

Part Number	Description
QPF1004QSB	5 pc sample bag
QPF1004QSQ	25 pc sample bag
QPF1004QSR	100 pcs 7” Short Reel
QPF1004QTR13	13” Tape and Reel, 2,500 pieces
QPF1004QEVB	Evaluation Board
QPF1004QDK	Evaluation Board Design Kit

Absolute Maximum Ratings

Parameter	Conditions	Rating
VDD (LNA Supply Voltage)		-0.5 to +5.25V
VCC (PA Supply Voltage)	No RF Input	-0.5 to +5.25V
Vlogic (Logic Voltage Inputs)		-0.5 to +5.25V
SDATA, SCLK (Serial Bus)		-0.5 to +5.25V
TX Input Power (Modulated)	@ PA attenuator Input (attenuator set to keep power at PA input <+7 dBm input)	+24 dBm
	@ Bypassing attenuator	+7 dBm
CW ANT power input power	Rx Mode	+25 dBm
Storage Temperature (Tstorage)		-55 to 150 °C

Notes:
1. Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device.
2. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

Parameter		Min.	Typ.	Max.	Units
TX/RX Operating Frequency Range	Tx	5.855		5.925	GHz
	Rx	5.150		5.925	GHz
Temperature (ambient) [1]		-40		105	°C
Junction Temperature [2]				173	°C
Supply Voltage (VCC & VDD)		+4.5	+5.0	+5.25	V
GPIO and Serial Write Logic Voltage – High		+1.35	+1.8	+5.25	V
GPIO and Serial Write Logic Voltage – Low		0		+0.35	V
Serial Input Voltage – READ, HIGH		1.7	1.8	1.9	V
Serial Input Voltage – READ, LOW		0		0.35	V

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

[1] Case Temperature allows 10°C max rise over ambient
[2] Tj based on Pout=29 dBm, 10M12RB LTE 4ms waveform, 50% Duty Cycle, VCC=VDD=5.25 V.

Test Signal Conditions

Name	Definition	MPR
TC1	TC1 LTE modulation	10M12RB QPSK (MPR0), 5M1RB QPSK (MPR0)
TC2	TC2 LTE modulation	10M50RB QPSK (MPR1)
TC3	TC3 DSRC/11p	BPSK/QPSK meeting Class C mask (10MHz, M7)
TC4	TC4 LTE modulation	20M100RB QPSK (MPR1)
TC5	TC5 LTE modulation	5M1RB QPSK (MPR0), for Harmonic measurement

TX Electrical Specifications

(Unless otherwise noted : Digital attenuator state=bypass, VCC/VDD=5V, T=+25°C)

C-V2X (TX_IN -ANT)	Conditions[1]	Min.	Typ.	Max.	Units
Frequency Range		5.855		5.925	GHz
Maximum Linear Power	TC1, LTE Modulation, 10MHz, 12RB QPSK (MPR=0dB)	TBD	29		dBm
	TC2, LTE Modulation, 10MHz, 50RB QPSK (MPR = 1dB)	TBD	28		dBm
	TC3, DSRC/11p, BPSK/QPSK meeting Class C mask	TBD	26		dBm
	TC4, LTE Modulation, 20MHz, 100RB QPSK (MPR = 1dB)	TBD	28		dBm
Gain	C-V2X, TC, ATT0/1=00 and TX_ATTN=0	TBD	33	TBD	dB
Gain Flatness	In-band, over any 10 MHz Channel			0.4	dBp_p
ACPR – EUTRA	TC1 modulation, Pout≤Pmax		-40	TBD	dBc
DEVM	DSRC, TC3, EVM		-32	TBD	dB
Operating Current	TC1 modulation, Pout=Pmax		680	TBD	mA
Quiescent Current	RF OFF		380		mA
2nd Harmonics	Vcc=5.0V, TC5 modulation, Pout≤ 29 dBm		-52	-39	dBm/MHz
3rd Harmonics			-52	-42	dBm/MHz
TX_IN Port Return Loss	ATT0/1=00-11 and TX_ATTN=0/1	TBD	12		dB
ANT Port Return Loss		TBD	16		dB

Notes : [1] Recommended EVB schematic/layout/BOM/PCB should be followed in order to achieve specified performance.

RX Electrical Specifications

(Unless otherwise noted: Digital attenuator state=Bypass, VDD=5V, T=+25ºC, Reg03=0x6B)

C-V2X/DSRC/11p (Through B47 BAW, ANT-RX_OUT or ANT-TX_IN/)	Conditions[1]		Min	Typ	Max	Unit
Frequency Range			5.855		5.925	GHz
Gain[2]	High Gain, Atten State 0		TBD	23	TBD	dB
	Low Gain, Atten State 0		TBD	12.5	TBD	
Gain Flatness	Over any 10 MHz Channel		-0.5		0.5	dB
Noise Figure[2]	High Gain	Atten State 0, 5855-5875 MHz		4.7	TBD	dB
		Atten State 0, 5875-5925 MHz		4.0	TBD	
	Low Gain	Atten State 0, 5855-5875 MHz		4.7	TBD	
		Atten State 0, 5875-5925 MHz		4.0	TBD	
Input Return Loss (Ant Port)	LNA_GAIN=0/1 and RX_ATTN=0/1		TBD	18.5		dB
Output Return Loss (Either TX_IN or RX_OUT port)			TBD	14.6		dB
Input P_{1dB}	High Gain		TBD	-13		dBm
	Low Gain		TBD	-2.9		
Input IP3	High Gain		TBD	-1.8		dBm
	Low Gain		TBD	10.9		
Operating Current	High Gain, Atten State 0			65	TBD	mA
	Low Gain, Atten State 0			25	TBD	
OOB Gain (Low Gain)	LB block, 663 – 915MHz			-64		dB
	MB block, 1700 – 2100MHz			-59		dB
	HB block, 2300 – 2700MHz			-52		dB
	N77 block, 3300 – 4200MHz			-30		dB
	N79 block, 4400 – 5000MHz			-33		dB
	UNII 1-3, 5110 – 5775MHz			-33		dB
LNA Bypass Mode (Through B47 BAW but bypassing LNA)						
Insertion Loss	V2X Rx mode, Bypass State		TBD	5.5	TBD	dB
Input IP3			TBD	35		dBm

Notes :

[1] Recommended EVB schematic/layout/BOM/PCB should be followed in order to achieve specified performance.

[2] DSA is in bypass mode

RX Electrical Specifications

(Unless otherwise noted: Digital attenuator state=Bypass, VDD=5V, T=+25ºC, Reg03=0x6B)

802.11ac (Bypass B47 BAW, ANT-RX_OUT or ANT- TX_IN/Common)	Conditions[1]	Min	Typ	Max	Unit
Frequency Range		5.15		5.850	GHz
Gain[2]	High Gain, Atten State 0	TBD	26	TBD	dB
	Low Gain, Atten State 0	TBD	15	TBD	dB
Gain Flatness	Over any 80 MHz Channel			1	dBp_p
Noise Figure[2]	High Gain, Atten State 0		2.1	TBD	dB
	Low Gain, Atten State 0		2.1	TBD	
Input Return Loss (Ant Port)	LNA_GAIN=0/1 and RX_ATTN=0/1	TBD	19		dB
Output Return Loss (Either TX_IN or RX_OUT port)		TBD	14.7		dB
Input P_{1dB}	High Gain	TBD	-14.5		dBm
	Low Gain	TBD	-5.25		
Input IP3	High Gain	TBD	-3.1		dBm
	Low Gain	TBD	7.3		
Operating Current	High Gain, Atten State 0		65	TBD	mA
	Low Gain, Atten State 0		25	TBD	
OOB Gain (Low Gain)	LB block, 663 – 915MHz		-60		dB
	MB block, 1700 – 2100MHz		-22		dB
	HB block, 2300 – 2700MHz		-11		dB
	N77 block, 3300 – 4200MHz		8		dB
	N79 block, 4400 – 5000MHz		13		dB
LNA Bypass Mode (Bypass B47 BAW)					
Insertion Loss		TBD	3.2	TBD	dB
Input IP3		TBD	33		dBm

Notes :

[1] Recommended EVB schematic/layout/BOM/PCB should be followed in order to achieve specified performance.

[2] DSA is in bypass mode

General Specifications(1)

(Unless otherwise noted: VCC/VDD=5V, T=+25ºC)

General Items	Conditions	Min	Typ	Max	Unit
VCC Leakage Current	Sleep Mode			10	µA
VDD Leakage Current				725	µA
Leakage Current on GPIO	High, Logic Input (per input)			115	µA
Coupler	Forward TX Coupling, PA in HPM	25	26.2	28	dB
	Forward Directivity, PA in HPM	11	15	23	dB
Switching Time	Sleep mode → TX or RX On		3.5	5.5	µs
	TX or RX → Sleep mode		170	500	ns
	TX → RX and RX → TX		300	650	ns
	Tx-Tx Attenuator Transition		165	300	ns
	Rx-Rx State Transition		230	600	ns
TX Stability[2] – Spurious levels	Spurious output level with Load VSWR=6:1, step phase angle in 30 deg step, Pfwd=max rated power (closed loop) Max spurious level, CW measurement, -40 to +105C			-70	dBc
Tx Ruggedness Room[2]	Temperature 25°: VSWR=10:1, Pdel <= Pmax with Pin <=+7 dBm	No Damage			
Tx Ruggedness[2]	Over Temperature: VSWR=6:1, Pdel <= Pmax with Pin <=+7 dBm	No Damage			
LNA Stability (K Factor)	All gain and bias states, PA disabled, -40 to +105C	1			N/A
Tx Active attenuator, f=5855-5925, +25C unless otherwise noted					
Attenuation using GPIO state 1[3]	Relative to ATT0/1=00	11.9	12.3	12.9	dB
Attenuation using GPIO state 2[3]		21.8	22.3	22.8	dB
Attenuation using GPIO state 3[3]		31	32	33.5	dB
Fine step attenuator insertion loss	Delta Gain TX_ATTN 0 to 1		2.4	3.35	dB
Gain Step	Using fine step serial port		0.23		dB
Successive Step Attenuator Error	TX_ATTN_STE<=80	-0.3	-0.02	0.4	dB
	TX_ATTN_STE>80	-0.4	-0.02	0.76	dB
Attenuation dynamic Range	Attenuation delta from TX_ATTN_STE=1 to TX_ATTN_STE=127		29.4		dB
Tx PA Bypass Attenuator, f=5855-5925, +25C unless otherwise noted					
Attenuation using GPIO state 1[3]	Relative to ATT0/1=00	9.1	9.3	9.7	dB
Attenuation using GPIO state 2[3]		20.5	20.75	21	dB
Attenuation using GPIO state 3[3]		31.3	31.8	32.3	dB
Gain Step	Using fine step serial port		0.25		dB
Successive Step Attenuator Error		-0.2		0.32	dB
Attenuation dynamic Range		31.2	31.8	32.3	dB
Rx path attenuator, f=5150-5925, +25C unless otherwise noted, ANT to TX_IN, All RX states					
Fine step attenuator insertion loss	Delta Gain RX_ATTN 0 to 1		3.3	4	dB
Gain Step	Using fine step serial port		0.26		dB
Successive Step Attenuator Error		-0.2		0.53	dB
Attenuation dynamic Range	Attenuation delta from RX_ATTN_STE=0 to RX_ATTN_STE=127	32.5	33.6	34.6	dB

[1] Recommended EVB schematic/layout/BOM/PCB should be followed in order to achieve specified performance.

[2] The expected minimum post TX FEM loss = 3dB; typical loss with external filter = 5dB

[3] Tx Mode Only. Coarse attenuation control

General Specifications[1]

(Unless otherwise noted: VCC/VDD=5V, T=+25ºC)

General Items	Conditions	Min	Typ	Max	Unit
Temperature Sensor					
Output Voltage	At room temperature	0.32	0.43	0.6	V
Output Range	T= -40C to +105ºC	0		1.11	V
Temperature Accurracy	T= -40C to +105ºC, Assume DC Calibration	-10		10	Deg
Power Detector					
Output Voltage	Output range 3dBm-29dBm over temperature	0.05		1.1	V
	Pout = +28.5 dBm	0.88	0.95	0.99	
	Pout = +20 dBm	0.5	0.57	0.63	
	P_{OUT} = +10 dBm	0.2	0.25	0.33	
Power Accuracy	3dBm ~ 28dBm		-0.4 / +0.7		dB
Calibration Mode Switch					
Gain (Cal Pin→Antenna)	PA in CAL Mode, Delta from ANT mode	1	2	3.5	dB

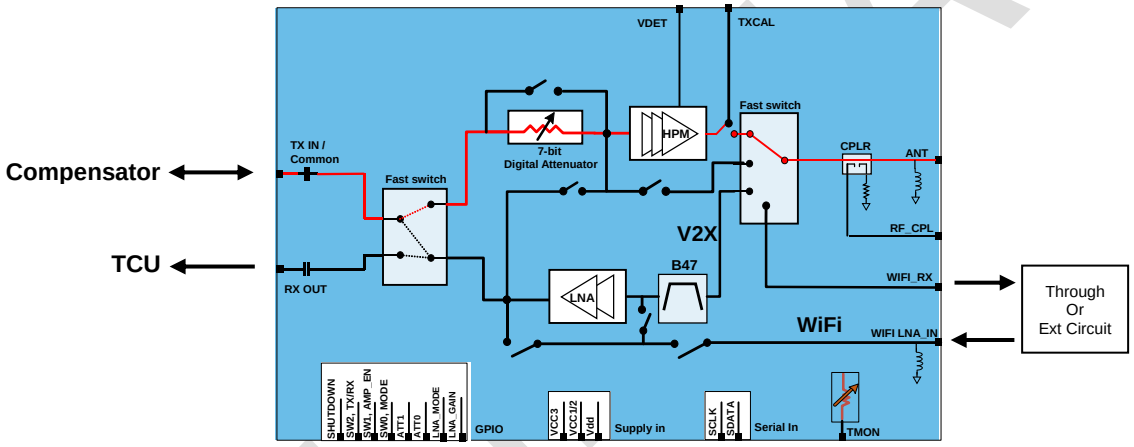
[1] Recommended EVB schematic/layout/BOM/PCB should be followed in order to achieve specified performance.

Control – Logic Truth Table

The logic tables are for GPIO Control Only; Alternative serial control is described in the register map

PA+Switch Control

Operating Mode	Shut down	SW2	SW1	SW0	Input SW State	Output SW State	LNA bias	PA bias
Sleep mode	1	X	X	X	OFF (iso)	OFF (iso)	OFF	OFF
Transmit mode	0	1	0	X	TX_IN to ATT input	PA out to ANT	OFF	ON
PA bypass mode	0	1	1	X	TX_IN to ATT input	ATT output to ANT	OFF	OFF
V2X Receive mode - TCU	0	0	0	0	RX_OUT to LNA out	B47 filter to ANT	ON	OFF
WiFi Receive mode -TCU	0	0	1	0	RX_OUT to LNA out	WIFI_RX to ANT	ON	OFF
V2X Receive mode - compensator	0	0	0	1	TX_IN to LNA output	B47 filter to ANT	ON	OFF
WiFi Receive mode - compensator	0	0	1	1	TX_IN to LNA output	WIFI_RX to ANT	ON	OFF



LNA control

Operating Mode	LNA_MODE	LNA_GAIN
Low gain state	0	0
High gain state	0	1
LNA bypass	1	X

Digital Attenuator & Bypass Control(1,2)

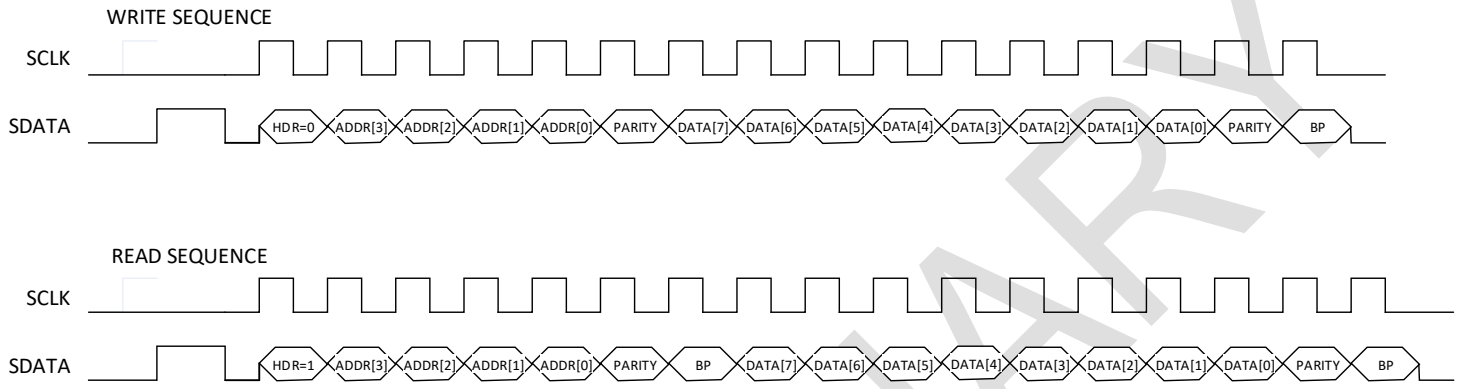
Operating Mode	ATT1	ATT0
Attenuator bypass - highest gain (3)	0	0
10 dB loss added	0	1
21 dB loss added	1	0
32 dB loss added	1	1

Notes :

1. GPIO ATT1/ATT0 controls the coarse step attenuation for Tx only.
2. For fine step attenuation control or Switching between DSA and Bypass mode on both Tx and Rx, Use the serial interface
3. The bypass mode is accessible for both Serial and GPIO.
   ATT0/ATT1=0 state means attenuator bypass mode in GPIO control
4. Default mode is fast bit GPIO mode. SPI commands override GPIO

Serial Communication Link

The serial interface that implemented is not RFFE. It is a slightly customized interface that is much like SPI but adds some RFFE like features that let it only require 2-wires.



- ADDR[3]-ADDR[0] is the address of the register to write
- At the start of the SDATA is pulled high for duration of one clock cycle, which wakes up the bus and necessary to achieve the two wire interface and used to synchronize the logic.
- Header bit, HDR: 0 = WRITE, 1 = READ
- BP: Bus Park which allows clean transition from write to read to write. During writes, the master forces SDATA low during the first half of the Bus Park period and then stops driving SDATA. On reads, the slave QPF1004Q drives SDATA low during the first half of the Bus Park period and stops driving on the second half. A weak pull-down resistor (100k Ohm) on SDATA and SCLK inside the slave ensures bus is not floating during this period.
- Parity: Odd parity covering header and address and a second odd parity covering data on write and read. If parity check fails, command sequence is aborted and parity bit is set in a status register.
- The maximum clock frequency is 52 MHz.
- Lead/Lag : SDATA can lead or lag SCLK by 5ns.

Serial Register Overview

Reg \ bits	7	6	5	4	3	2	1	0
reg00 (0x00)	GPIO_ORIDE	reserved	RX_BYPASS_MODE_ATTN	LNA_GAIN	TX_CAL	SHUTDOWN	SW[1:0]	
reg01 (0x01)	TX_ATTN	TX_ATTN_STE[6:0]						
reg02 (0x02)	RX_ATTN	RX_ATTN_STE[6:0]						
reg03 (0x03)	PROT_STAT[1:0]		LNA_DRI_BIAS[2:0]			LNA_OUT_BIAS[2:0]		
reg07 (0x07)	PA_BIAS[3:0]				RESERVED[1:0]		ADDR_PARITY_ERR	DATA_PARITY_ERR

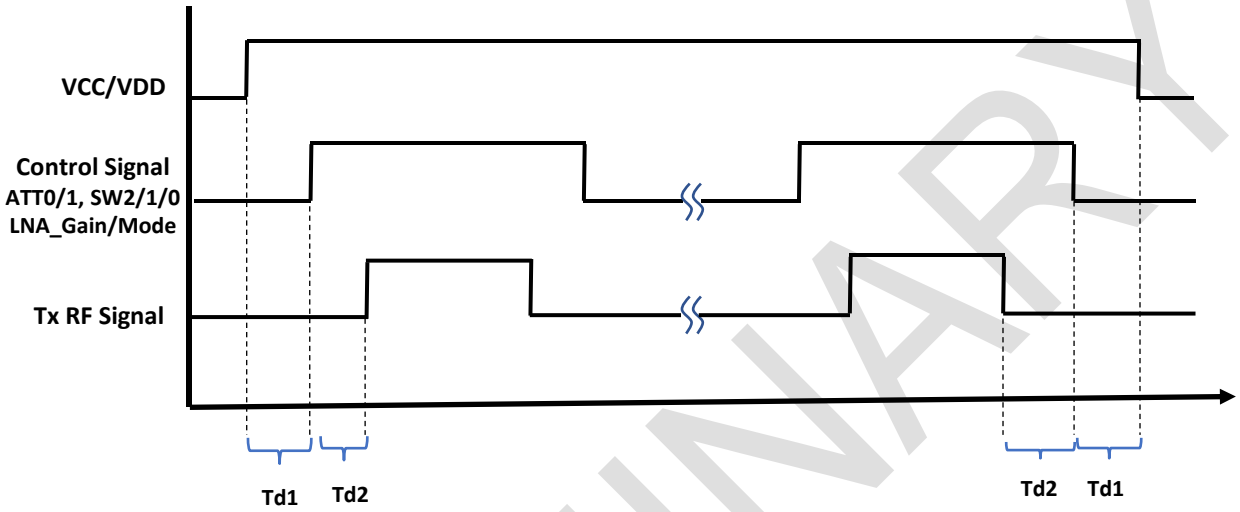
- Positive override of GPIO required (0x00[7])
- Fast control bits (SW2=Tx/Rx, LNA_MODE) are still handled using GPIO inputs
- Serial control offers fine control of the attenuator as well as the LNA bias setting

Detailed SPI Register Map

Register address	Data Bits	Register Name	Qorvo Bit Field Name	Default [msb:lsb]	Qorvo Description	Read/ Write
0x00	Reg00[7]	OPERATING_MODE	GPIO_ORIDE	1b0	0: Fast bit GPIO inputs are used (Default) 1: Use SPI regsiters for all inputs	R/W
0x00	Reg00[6]	OPERATING_MODE	reserved	1b0		R/W
0x00	Reg00[5]	OPERATING_MODE	RX_BYPASS_MODE_ATTN	1b0	0: normal operation 1: Add 3dB attenuation in Rx bypass mode	R/W
0x00	Reg00[4]	OPERATING_MODE	LNA_GAIN	1b0	0: LNA Low gain mode 1: LNA High gain mode	R/W
0x00	Reg00[3]	OPERATING_MODE	TX_CAL	1b0	0: normal operation 1: Antenna output connected to dummy load	R/W
0x00	Reg00[2]	OPERATING_MODE	SHUTDOWN	1b0	0: Normal Operation 1: Sleep Mode (Bias Shutdown)	R/W
0x00	Reg00[1:0]	OPERATING_MODE	SW[1:0]	2b0	OPERATING_MODE Tx mode (SW2=1) 0X: Normal Transmit Mode - TCU or compensator 1X: PA bypass mode Rx mode (SW2=0) 00: Normal V2X Receive Mode - TCU 10: Normal 802.11ac Receive Mode - TCU 01: Normal V2X Receive Mode - Compensator 11: Normal 802.11ac Receive Mode - Compensator	R/W
0x01	Reg01[7]	TX_ATTN_CTRL	TX_ATTN	1b0	0: PA Attenuator bypass 1: Use PA Attenuator	R/W
0x01	Reg01[6:0]	TX_ATTN_CTRL	TX_ATTN_STE[6:0]	7b0000000	Sets the TX Attenuator MSB-->LSB Binary ladder from 0000000-->1111111 0000000=1dB added attenuation 1111111=32dB added attenuation 0.25dB step	R/W
0x02	Reg02[7]	RX_ATTN_CTRL	RX_ATTN	1b0	0: RX Attenuator Bypass to TXIN 1: Use RX Attenuator	R/W
0x02	Reg02[6:0]	RX_ATTN_CTRL	RX_ATTN_STE[6:0]	7b0000000	Sets the RX Attenuator MSB-->LSB Binary ladder from 0000000-->1111111 0000000=1dB added attenuation 1111111=32dB added attenuation 0.25dB step	R/W
0x03	Reg03[7:6]	LNA_BIAS_CTRL	PROT_STAT[1:0]	2b00	00: Protection circuits enabled 01: Tx protection circuit disabled 10: Rx protection circuit disabled 11: Tx and Rx protection circuits disabled	R/W
0x03	Reg03[5:3]	LNA_BIAS_CTRL	LNA_DRI_BIAS[2:0]	3b101	000: Min bias 111: Max Bias	R/W
0x03	Reg03[2:0]	LNA_BIAS_CTRL	LNA_OUT_BIAS[2:0]	3b011	000: Min bias 111: Max Bias	R/W
0x07	Reg07[7:4]	STATUS	PA_BIAS[3:0]	4b0000	0000 - Min PA Bias 1111 - Max PA Bias	R/W

Power On and Off Sequence

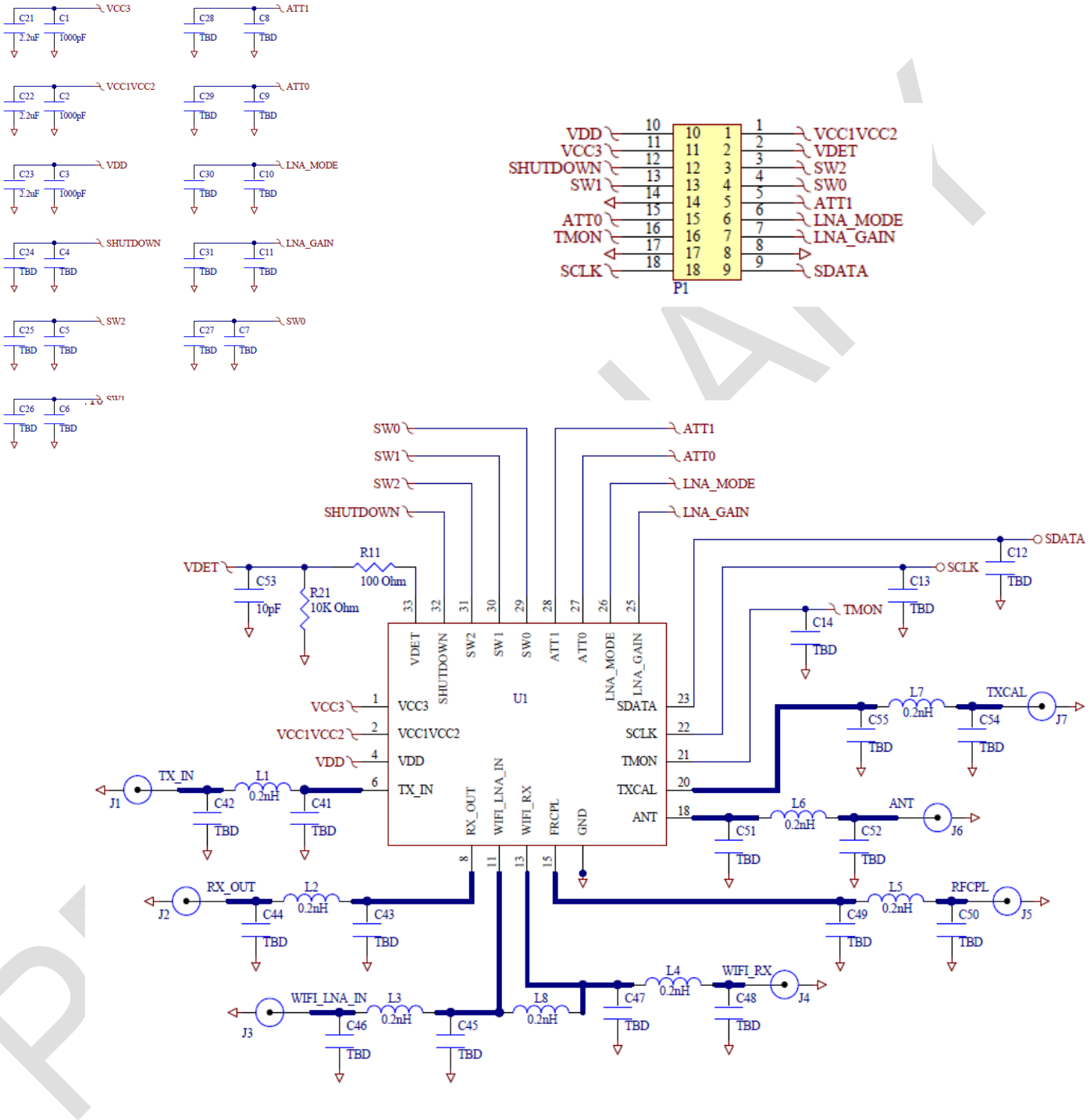
QPF1004Q Transmit
RF Signal/DC Power ON/OFF Sequence



Note :
Observe the timing sequence shown in the diagram above and described below.
DC, RF Signal, and Time Delay (Td) signal levels per datasheet specifications.

- Apply VCC/VDD prior to turning on or pulsing Control Signal
- Turn on Control Signal prior to applying RF Signal
- Turn off RF Signal prior to turning off Control Signal
- Turn off Control Signal prior to turning off VCC/VDD
- Td1 = 5 usec Min.
- Td2 = 500 nsec Min.

QPF1004Q-EVB Schematic



Notes:

1. For Rx Wi-Fi mode, 0 ohm resistor or 0.2nH should be placed between WIFI_RX and WIFI_LNA_IN, (L8 in schematic)
2. If SCLK and SDATA pins are not being used, two pins are internally pulled down and can be left open.
3. Recommend to place 50 ohms on unused RF ports.
4. LC matching networks on RF ports are place holders for external matching if needed.

QPF1004Q-EVB Bill of Materials

Ref Des	Qty	Material#	Alt Grp	Usage Prob%	Description	Manufacturer	Manufacturer Part Number
EVB	1	298466			PCB, QPF1004Q	TTM TECHNOLOGIES INC	QPF100X-4000(A)
C1,C2,C3	3	269505			CAP, 1000pF, 10%, 10V, X7R, 01005	TAIYO YUDEN (SINGAPORE) PTE LTD	LMK042B7102KC-W
C53	1	270215			CAP, 10pF, +/-0.25pF, 16V, C0G, 01005	TAIYO YUDEN (SINGAPORE) PTE LTD	RM EMK042 CG100CD-W
C21,C22,C23	3	277672			CAP, 2.2uF, 10%, 10V, X7S, 0.65mm, 0402	TDK SINGAPORE (PTE) LTD	C1005X7S1A225KT000E
R21	1	23152			RES, 10K, 1%, 1/20W, 0201	Kamaya, Inc	RMC1/20-1002FPA15
R11	1	260036			RES, 100 OHM, 5%, 1/32W, 01005	Kamaya, Inc	RMC1/32-101JPA
L1,L2,L8,L5,L6,L7	6	273713			IND, 0.2nH, +/-0.1nH, T/F, HI-Q, 01005	MURATA ELECTRONICS SINGAPORE PTE LT	LQP02TN0N2B02L
P1	1	280114			CONN, HDR, 2x9, RT-ANG, 0.100", T/H	SAMTEC INC.	TSW-109-08-G-D-RA
J1,J2,J3,J4,J5,J6,J7	7	21419	A2	100	CONN, SMA, EL MINI FLT 0.048" SPE-000311	Aliner Industries, Inc.	20-001CG-T
J1,J2,J3,J4,J5,J6,J7	7	270274	A2	0	CONN, SMA, END LNCH, MINI, FLT, 0.048"	Aliner Industries, Inc.	20-001CG-T
U1	1	QPF1004Q			Automotive C-V2X B47/ 802.11p / 802.11ac		
C41, C42, C43, C44, C45, C46, C47, C48,C49, C50, C51, C52,	14	4XXX1			NOT POPULATED ITEM-1		DUMMY PART
C24,C25,C26,C27,C28,C29,C30 ,C31	8	4XXX2			NOT POPULATED ITEM-2		DUMMY PART
C4,C5,C6,C7,C8,C9,C10,C11,C1 2,C13,C14	11	4XXX3			NOT POPULATED ITEM-3		DUMMY PART
L3,L4	2	4XXX4			NOT POPULATED ITEM-4		DUMMY PART

QPF1004Q-EVB PCB Information

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	L1	Copper	1.70mil		
4	Dielectric1	RO4350B	6.60mil	3.66	
5	L2	Copper	0.70mil		
6	Dielectric 3	ISOLA 408HR	26.00mil	3.68	
7	L3	Copper	0.70mil		
8	Dielectric 2	RO4350B	6.60mil	3.66	
9	L4	Copper	1.70mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				

TOTAL THICKNESS: .045+/- 10%

CONTROLLED IMPEDANCE: ☒ YES ☐ NO

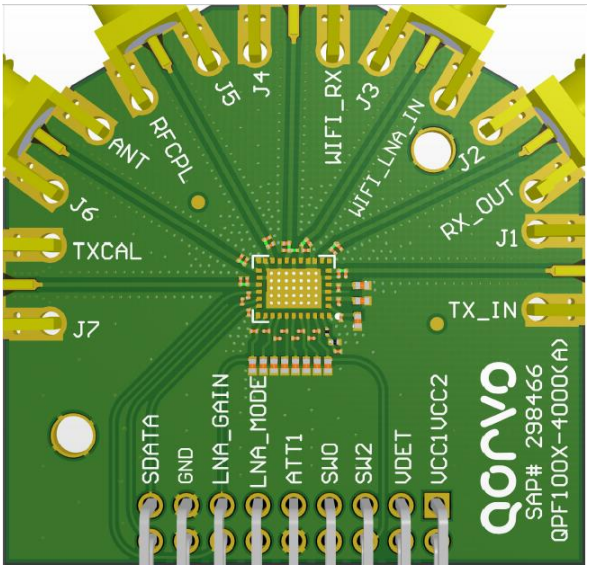
MICROSTRIP LAYER 1	0.013 +/-0.001	REF LAYER 2
TARGET IMPEDANCE:	50 OHMS +/-10%	
TARGET FREQUENCY:	2.50 GHz	
DIELECTRIC CONSTANT:	3.66	

* DIELECTRIC(S) THAT CAN BE ADJUSTED TO OBTAIN FINISHED THICKNESS: LAYER 2-3

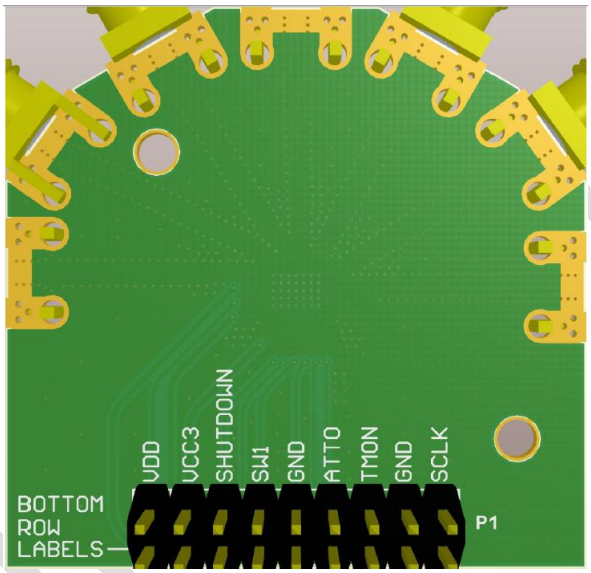
* GERBER DATA SUPPLIED WITH DESIRED FINAL TRACE WIDTHS. PROCESS COMPENSATION TRACE WIDTH ADJUSTMENT TO BE DONE BY PCB FABRICATOR. IF TRACE WIDTH OR GAP HAS TO BE ADJUSTED PLEASE VERIFY WITH QORVO

QPF1004Q-EVB Layout

Top View

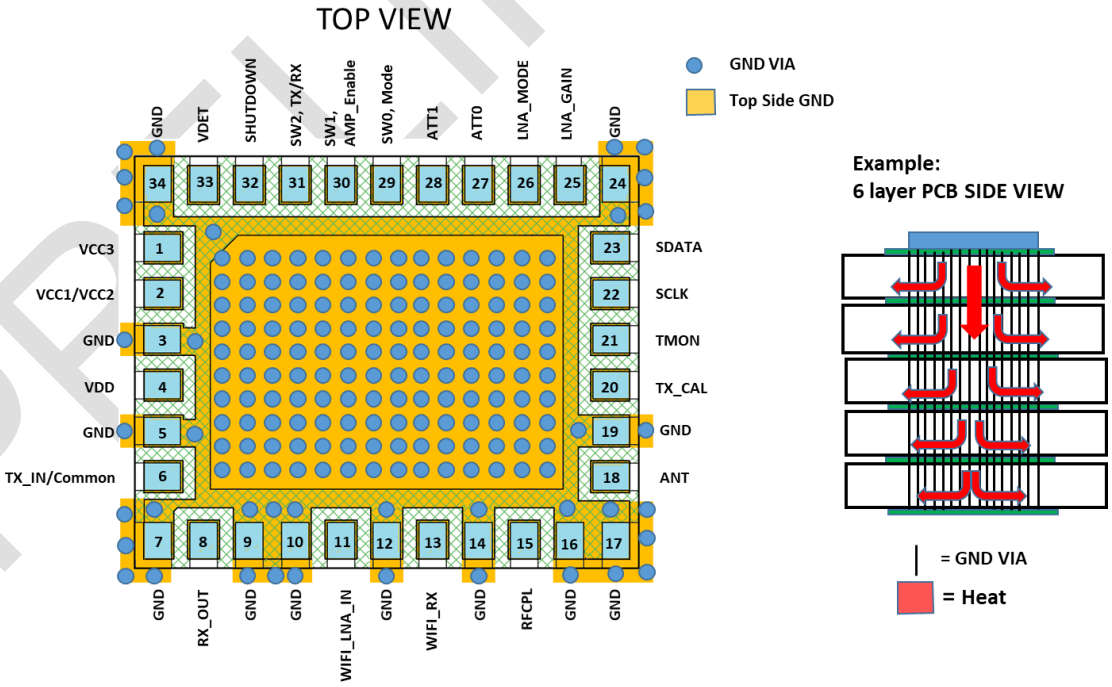


Bottom View

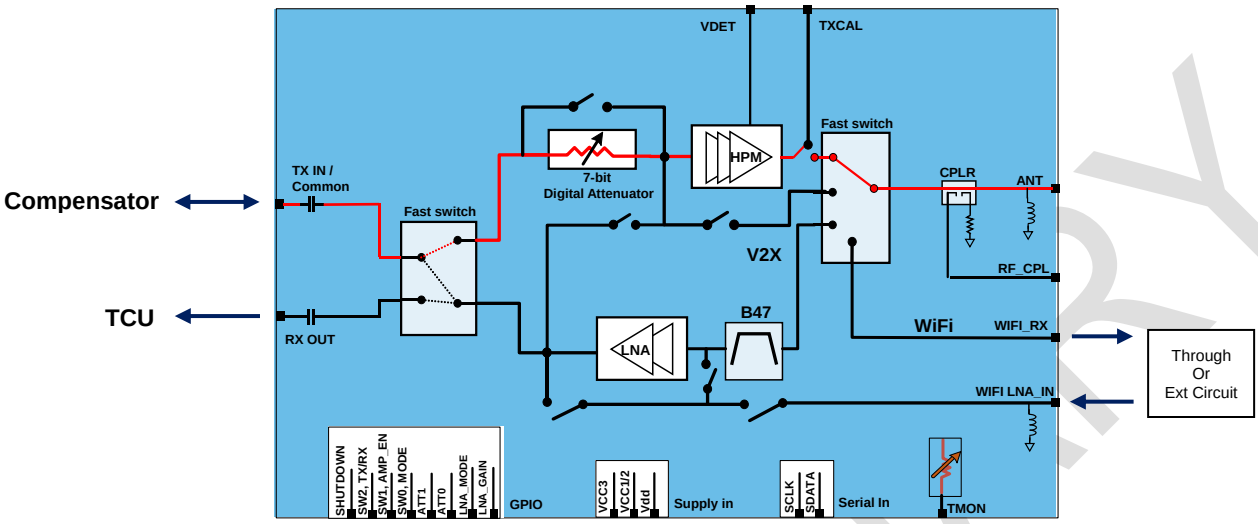


Heat dissipation is a major concern as the device gain is effected by high thermal temperatures. A suggested layout providing a large ground area with adequate GND vias is provided below. Internal ground islands are also suggested to be used to draw heat from the device. The goal is to lower the thermal resistivity to other layers and also lower the electrical inductance.

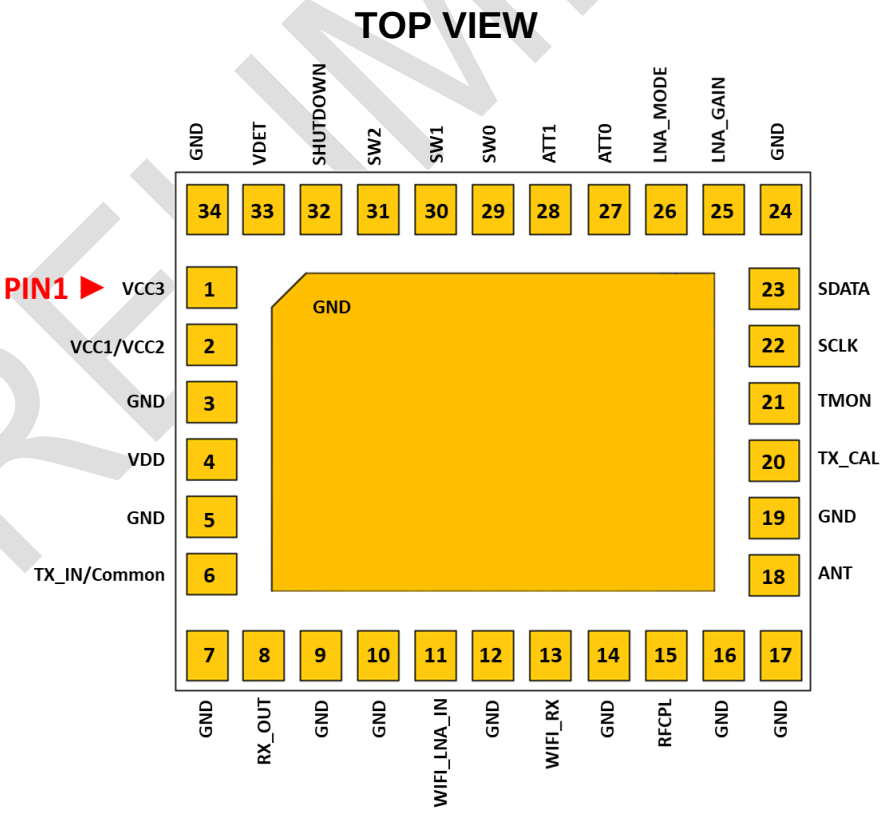
PCB layout recommendation



Pin-Out Configuration



Pin Map



Pin Description

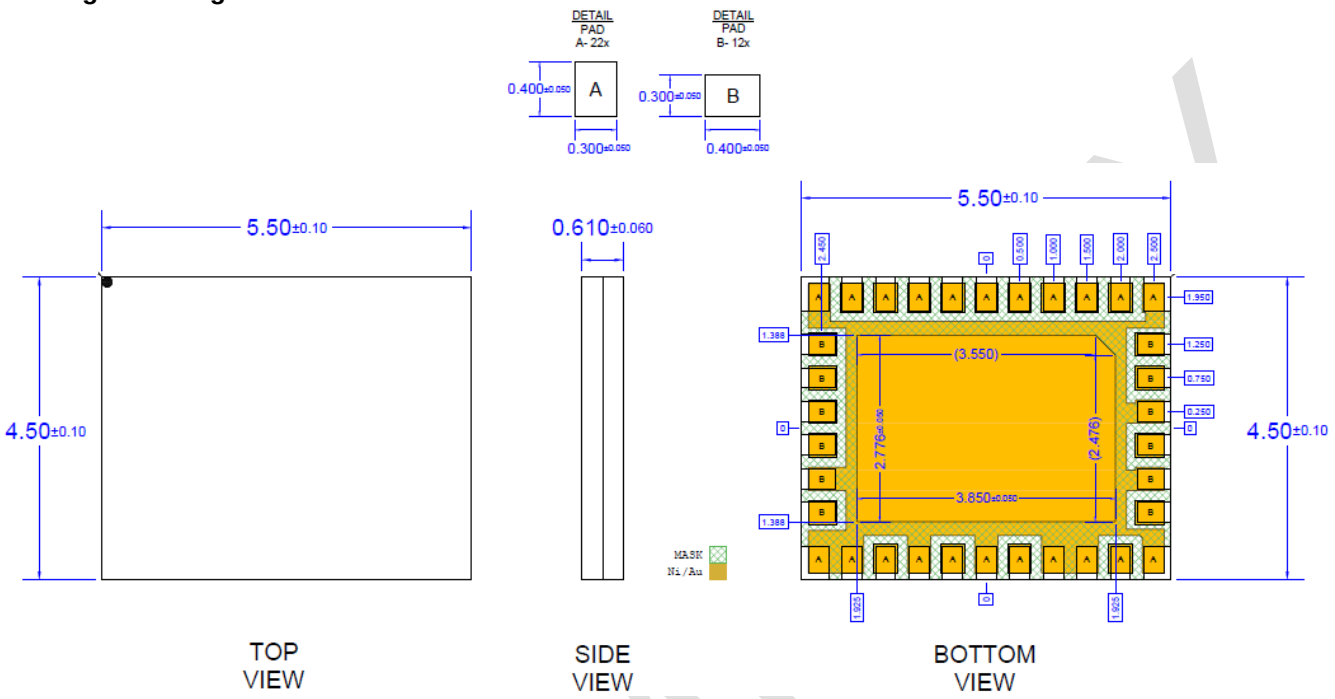
PIN NO.	LABEL	DESCRIPTION
1	VCC3	Supply voltage for output stage of PA
2	VCC1/VCC2	Supply voltage for driver stages of PA
4	VDD	Supply voltage for LNA, voltage for Ant SW and PA Bias control
6	TX_IN/Common	Common RF Tx input, also Rx output in compensator mode, Internally DC Blocked
8	RX_OUT	RX output to chipset for use in standalone mode for TCU configuration, Internally DC Blocked
11	WIFI_LNA_IN	Rx input that bypasses internal B47 filter, External DC block is required if DC is on line
13	WIFI_RX	Rx output from antenna switch used for bypassing internal B47 filter, External DC block is required if DC is on line
15	RFCPL	Coupler output
18	ANT	Antenna Port, External DC block is required if DC is on line
20	TX_CAL	PA output for use in calibration mode, External DC block is required if DC is on line
21	TMON	Analog temperature sensor output
22	SCLK	Clock signal for serial interface
23	SDATA	Data signal for serial interface
25	LNA_GAIN	GPIO control for LNA gain step
26	LNA_MODE	GPIO control for LNA bypass
27	ATT0	GPIO control for Tx course step attenuator
28	ATT1	GPIO control for Tx course step attenuator
29	SW0, Mode	GPIO control for I/O switches, PA
30	SW1, AMP_Enable	GPIO control for I/O switches, PA
31	SW2, Tx/Rx	GPIO control for I/O switches, PA, Toggle Tx/Rx
32	SHUTDOWN	Disables LNA, PA bias, device into low current state, SHUTDOWN when active High
33	VDET	Power detector voltage
3, 5, 7, 9, 10, 12, 14, 16, 17, 19, 24, 34	GND	Ground connection.

Notes :

1. All GPIO pins are internally pulled down with a 50 Kohm.
2. Control pins can be left open but recommend to ground pins rather than float to avoid picking up noise
3. No observed bad effects from unterminated unused RF ports, but recommend placing 50 ohms on unused RF ports by default
4. If serial interface is enabled, only GPIO pins SW2 and LNA_MODE are accessible
5. SDATA and SCLK can be left open when not using the serial interface. They are internally pulled down.
6. RFCPL, Coulpler inside is not bi-directional and able to measure forward power only.

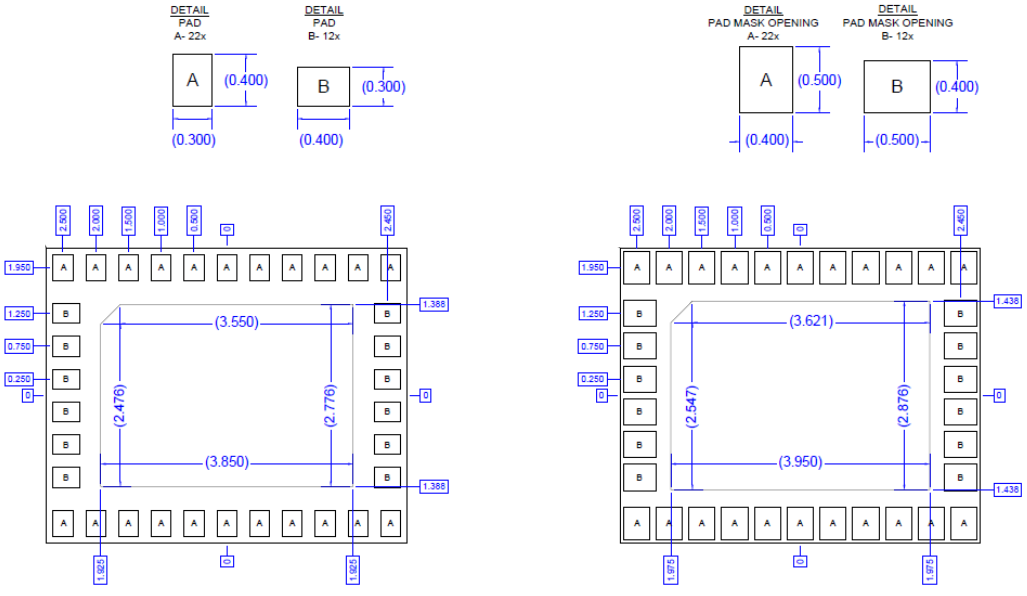
Mechanical Information

Package Drawing

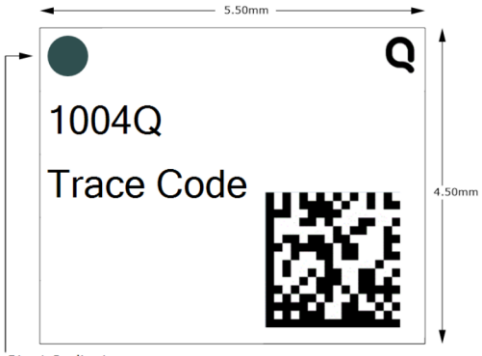


Notes:

1. The PIN 1 location in this drawing is for just mechanical drawing not electrical pin.



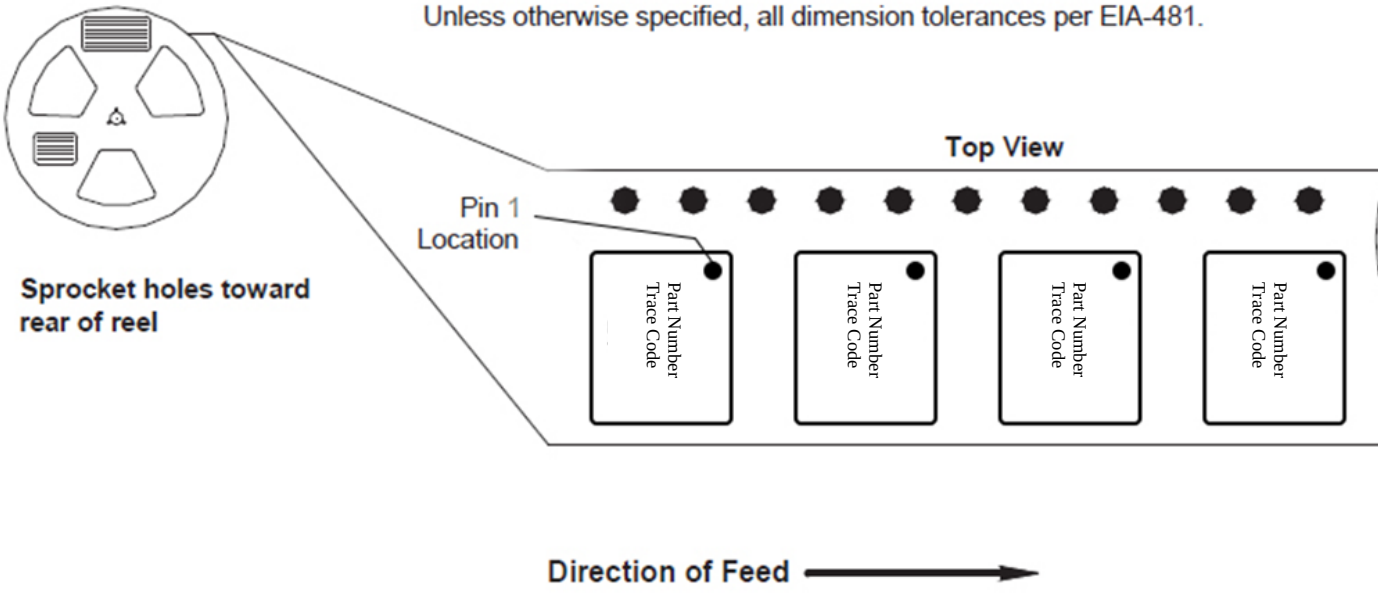
Marking Diagram



Tape and Reel Information

Table 1. Tape and Reel

Qorvo Part Number	Reel Diameter Inch (mm)	Hub Diameter Inch (mm)	Width (mm)	Pocket Pitch (mm)	Feed	Units Per Reel
QPF1004QTR13	13 (330)	4 (102)	12(305)	8(203)	Single	2500
QPF1004QSR	7 (178)	2.4 (60)	12(305)	8(203)	Single	100



Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	TBD	ANSI/ESD/JEDEC JS-001
ESD – Charged Device Model (CDM)	TBD	JEDEC JESD22-C101
MSL – Moisture Sensitivity Level	TBD	IPC/JEDEC J-STD-020

Caution!

ESD sensitive device

Solderability

Compatible with both lead-free (260 °C max. reflow temperature) and tin/lead (245 °C max. reflow temperature) soldering processes.
Package lead plating: ENEPIG (Electroless-Nickel Electroless-Palladium Immersion-Gold)

RoHS Compliance

This part is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.

This product also has the following attributes:

PFOS Free
Product uses RoHS Exemption 7c-I to meet RoHS Compliance requirements
Halogen Free (Chlorine, Bromine)
Antimony Free
TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
SVHC Free

REVISION HISTORY

Revision	Description	
A	• Initial draft datasheet • Updated spec table, plots and EVB information	
B	• Update spec based on PRD • Update EVB information, Part drawing and dimensions, Mechanical information • Update Logic and Register table • Add Timing Diagram, Update Functional Block Diagram • Add Pin Map diagram,	Jan 3rd, 2021
C	• Updated Spec based on PRD • Added comments for Pin configuration and details of serial communication • Updated EVB information, BOM • Simplified Block Diagram	Sep 14th, 2021
D	• Updated description on Application section, Block Diagram and Ordering Information • Updated voltage limits in AMR and Operating condition, Test Signal Conditions • Updated Tx Spec and condition, Removed Tx spec for WiFi mode • Updated Rx Spec, Separate Freq range for NF, General specifications • Add Notes for GPIO control, EVB matching networks, External jumper for WiFi • Fix description fault for SHUTDOWN in register map • Update descriptions for LNA BIAS_CTRL and PA_BIAS in register map	Jan 19th, 2022

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:
Web: www.qorvo.com
Tel: 1-844-890-8163
Email: customer.support@qorvo.com

Important Notice