

MOSFET– N & P-Channel, POWERTRENCH® 20 V

FDG6332C

General Description

The N & P-Channel MOSFETs are produced using ON Semiconductor's advanced POWERTRENCH process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.

These devices have been designed to offer exceptional power dissipation in a very small footprint for applications where the bigger more expensive TSSOP-8 and SSOP-6 packages are impractical.

Features

- $Q1$ 0.7 A, 20 V
 - ♦ $R_{DS(ON)} = 300\text{ m}\Omega$ @ $V_{GS} = 4.5\text{ V}$
 - ♦ $R_{DS(ON)} = 400\text{ m}\Omega$ @ $V_{GS} = 2.5\text{ V}$
- $Q2$ -0.6 A, -20 V
 - ♦ $R_{DS(ON)} = 420\text{ m}\Omega$ @ $V_{GS} = -4.5\text{ V}$
 - ♦ $R_{DS(ON)} = 630\text{ m}\Omega$ @ $V_{GS} = -2.5\text{ V}$
- Low Gate Charge
- High Performance Trench Technology for Extremely Low $R_{DS(ON)}$
- SC70-6 Package: Small Footprint (51% Smaller than SSOT-6); Low Profile (1 mm Thick)
- These Devices are Pb-Free and are RoHS Compliant

Applications

- DC/DC Converter
- Load Switch
- LCD Display Inverter

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

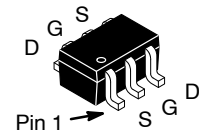
Symbol	Parameter		Q1	Q2	Units
V _{DSS}	Drain–Source Voltage		20	–20	V
V _{GSS}	Gate–Source Voltage		±12	±12	V
I _D	Drain Current	Continuous (Note 1)	0.7	–0.6	A
		Pulsed	2.1	–2	
P _D	Power Dissipation for Single Operation (Note 1)		0.3		W
T _J , T _{STG}	Operating and Storage Junction Temperature Range		–55 to 150		°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.



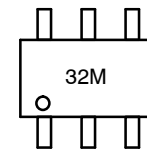
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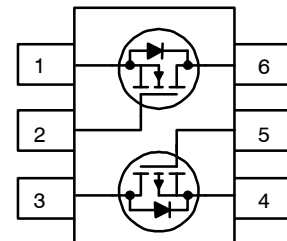
SC-88/SC70-6/SOT-363
CASE 419B-02

MARKING DIAGRAM



32 = Specific Device Code
M = Assembly Operation Month

PIN CONNECTIONS



Complementary

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FDG6332C

THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	415	$^{\circ}\text{C/W}$

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. $R_{\theta JA} = 415^{\circ}\text{C/W}$ on minimum pad mounting on FR-4 board in still air.

ORDERING INFORMATION

Device Marking	Device	Reel Size	Tape Width	Shipping†
32	FDG6332C	7"	8 mm	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS ($T_A = 25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV_{DSS}	Drain-Source Breakdown Voltage	Q1	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	20	–	–	V
		Q2	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-20	–	–	
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	Q1	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C	–	14	–	$\text{mV}/^{\circ}\text{C}$
		Q2	$I_D = -250\text{ }\mu\text{A}$, Referenced to 25°C	–	-14	–	
I_{DSS}	Zero Gate Voltage Drain Current	Q1	$V_{DS} = 16\text{ V}, V_{GS} = 0\text{ V}$	–	–	1	μA
		Q2	$V_{DS} = -16\text{ V}, V_{GS} = 0\text{ V}$	–	–	-1	
I_{GSSF} / I_{GSSR}	Gate-Body Leakage, Forward	$V_{DS} = \pm 12\text{ V}, V_{GS} = 0\text{ V}$		–	–	± 100	nA
I_{GSSF} / I_{GSSR}	Gate-Body Leakage, Reverse	$V_{GS} = \pm 12\text{ V}, V_{DS} = 0\text{ V}$		–	–	± 100	nA

ON CHARACTERISTICS (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	Q1	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	0.6	1.1	1.5	V
		Q2	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-0.6	-1.2	-1.5	
$\Delta V_{GS(th)} / \Delta T_J$	Gate Threshold Voltage Temperature Coefficient	Q1	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C	–	-2.8	–	$\text{mV}/^{\circ}\text{C}$
		Q2	$I_D = -250\text{ }\mu\text{A}$, Referenced to 25°C	–	3	–	
$R_{DS(on)}$	Static Drain-Source On-Resistance	Q1	$V_{GS} = 4.5\text{ V}, I_D = 0.7\text{ A}$	–	180	300	$\text{m}\Omega$
			$V_{GS} = 2.5\text{ V}, I_D = 0.6\text{ A}$	–	293	400	
			$V_{GS} = 4.5\text{ V}, I_D = 0.7\text{ A}, T_J = 125^{\circ}\text{C}$	–	247	442	
		Q2	$V_{GS} = -4.5\text{ V}, I_D = -0.6\text{ A}$	–	300	420	
			$V_{GS} = -2.5\text{ V}, I_D = -0.5\text{ A}$	–	470	630	
			$V_{GS} = -4.5\text{ V}, I_D = -0.6\text{ A}, T_J = 125^{\circ}\text{C}$	–	400	700	
g_{FS}	Forward Transconductance	Q1	$V_{DS} = 5\text{ V}, I_D = 0.7\text{ A}$	–	2.8	–	S
		Q2	$V_{DS} = -5\text{ V}, I_D = -0.6\text{ A}$	–	1.8	–	
$I_{D(on)}$	On-State Drain Current	Q1	$V_{GS} = 4.5\text{ V}, V_{DS} = 5\text{ V}$	1	–	–	A
		Q2	$V_{GS} = -4.5\text{ V}, V_{DS} = -5\text{ V}$	-2	–	–	

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	Q1	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	–	113	–	pF
		Q2	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	–	114	–	
C_{oss}	Output Capacitance	Q1	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	–	34	–	pF
		Q2	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	–	24	–	

FDG6332C

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted) (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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DYNAMIC CHARACTERISTICS

C_{rss}	Reverse Transfer Capacitance	Q1	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	–	16	–	pF
		Q2	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	–	9	–	

SWITCHING CHARACTERISTICS (Note 2)

$t_{d(on)}$	Turn-On Delay Time	Q1	For Q1 $V_{DS} = 10\text{ V}, I_D = 1\text{ A},$ $V_{GS} = 4.5\text{ V}, R_{GEN} = 6\ \Omega$	–	5	10	ns
		Q2		–	5.5	11	
t_r	Turn-On Rise Time	Q1	For Q2 $V_{DS} = -10\text{ V}, I_D = -1\text{ A},$ $V_{GS} = -4.5\text{ V}, R_{GEN} = 6\ \Omega$	–	7	15	ns
		Q2		–	14	25	
$t_{d(off)}$	Turn-Off Delay Time	Q1		–	9	18	ns
		Q2		–	6	12	
t_f	Turn-Off Fall Time	Q1		–	1.5	3	ns
		Q2		–	1.7	3.4	
Q_g	Total Gate Charge	Q1	For Q1 $V_{DS} = 10\text{ V}, I_D = 0.7\text{ A},$ $V_{GS} = 4.5\text{ V}, R_{GEN} = 6\ \Omega$	–	1.1	1.5	nC
		Q2		–	1.4	2	
Q_{gs}	Gate–Source Charge	Q1	For Q2 $V_{DS} = -10\text{ V}, I_D = -0.6\text{ A},$ $V_{GS} = -4.5\text{ V}, R_{GEN} = 6\ \Omega$	–	0.24	–	nC
		Q2		–	0.3	–	
Q_{gd}	Gate–Drain Charge	Q1		–	0.3	–	nC
		Q2		–	0.4	–	

DRAIN–SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

I_S	Maximum Continuous Drain–Source Diode Forward Current	Q1		–	–	0.25	A
		Q2		–	–	–0.25	
V_{SD}	Drain–Source Diode Forward Voltage	Q1	$V_{GS} = 0\text{ V}, I_S = 0.25\text{ A (Note 2)}$	–	0.74	1.2	V
		Q2	$V_{GS} = 0\text{ V}, I_S = -0.25\text{ A (Note 2)}$	–	–0.77	–1.2	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$

TYPICAL PERFORMANCE CHARACTERISTICS: N-CHANNEL

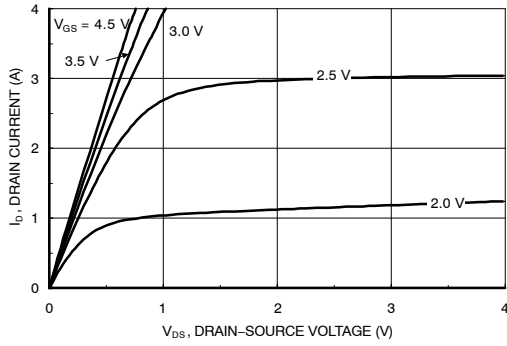


Figure 1. On-Region Characteristics

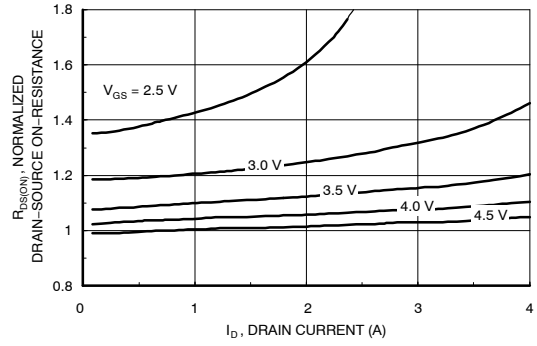


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

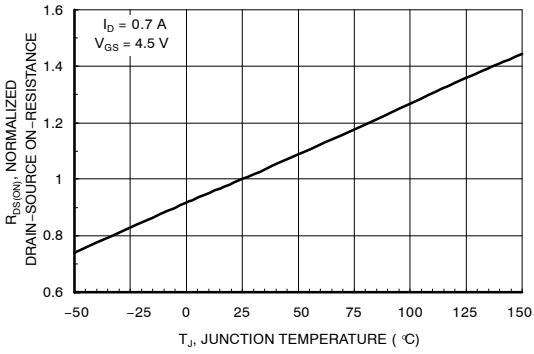


Figure 3. On-Resistance Variation with Temperature

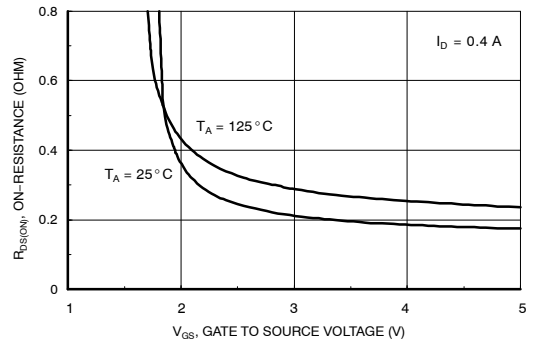


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

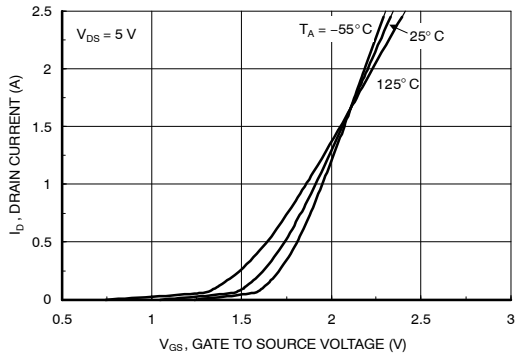


Figure 5. Transfer Characteristics

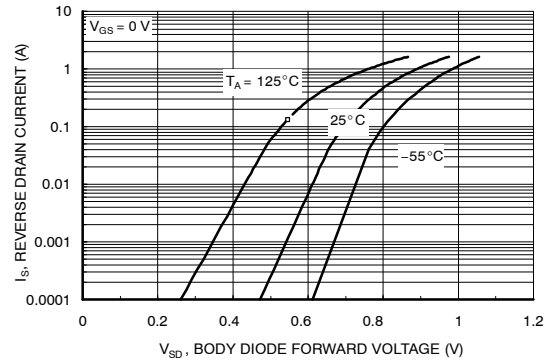


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL PERFORMANCE CHARACTERISTICS: N-CHANNEL (continued)

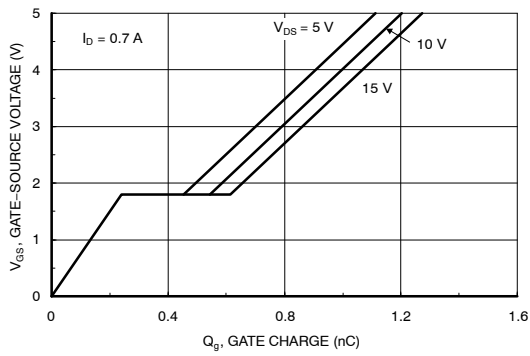


Figure 7. Gate Charge Characteristics

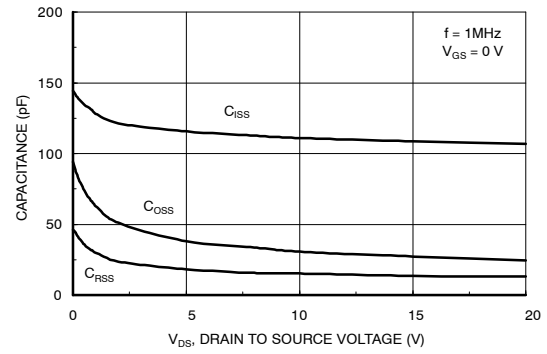


Figure 8. Capacitance Characteristics

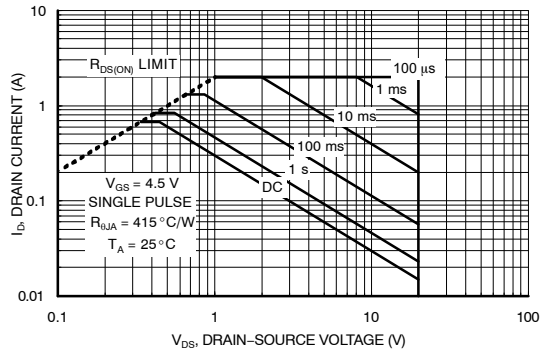


Figure 9. Maximum Safe Operating Area

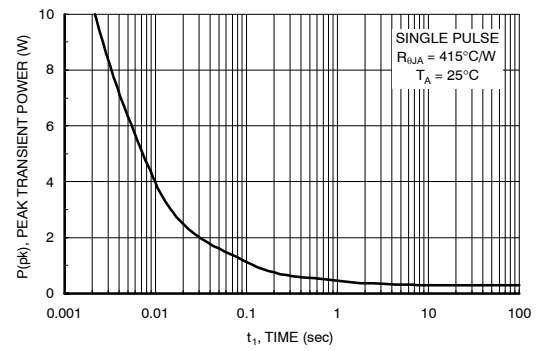


Figure 10. Single Pulse Maximum Power Dissipation

TYPICAL PERFORMANCE CHARACTERISTICS: P-CHANNEL

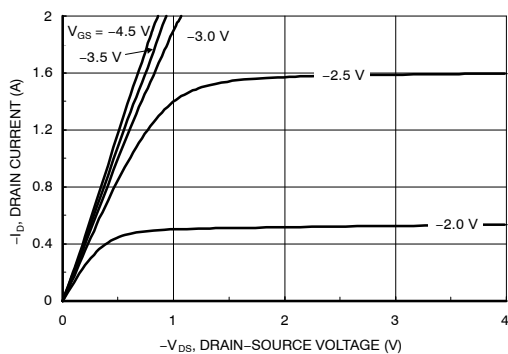


Figure 11. On-Region Characteristics

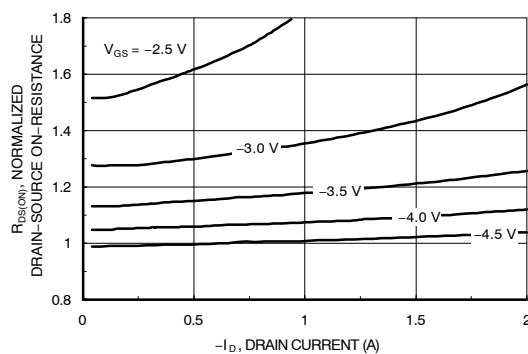


Figure 12. On-Resistance Variation with Drain Current and Gate Voltage

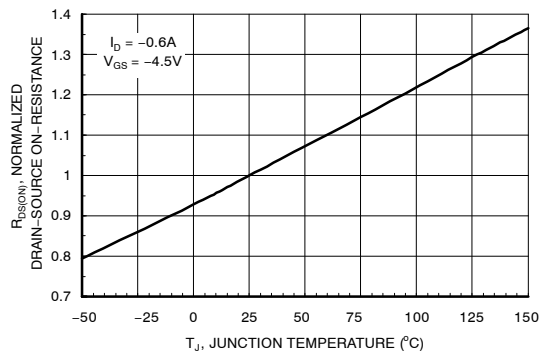


Figure 13. On-Resistance Variation with Temperature

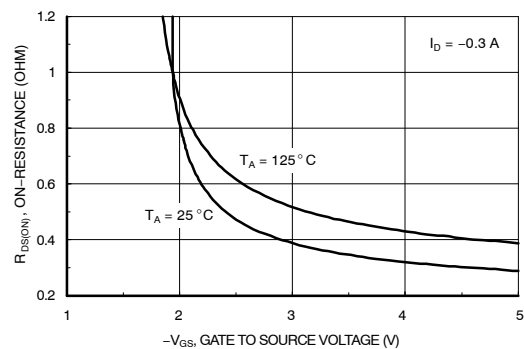


Figure 14. On-Resistance Variation with Gate-to-Source Voltage

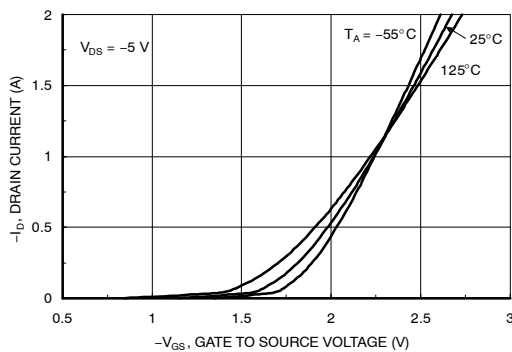


Figure 15. Transfer Characteristics

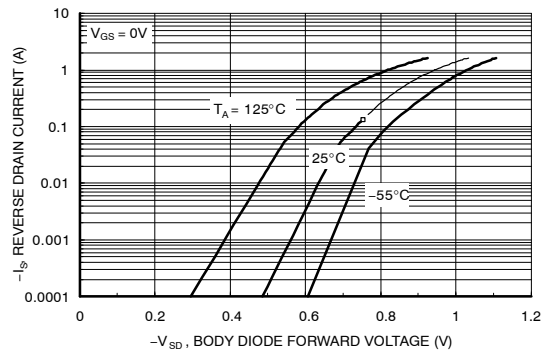


Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL PERFORMANCE CHARACTERISTICS: P-CHANNEL (continued)

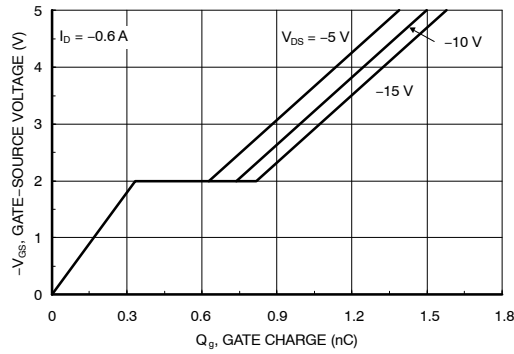


Figure 17. Gate Charge Characteristics

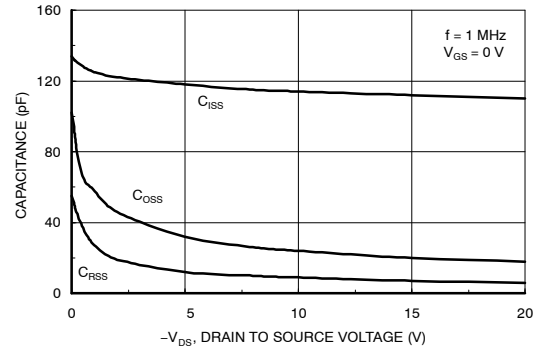


Figure 18. Capacitance Characteristics

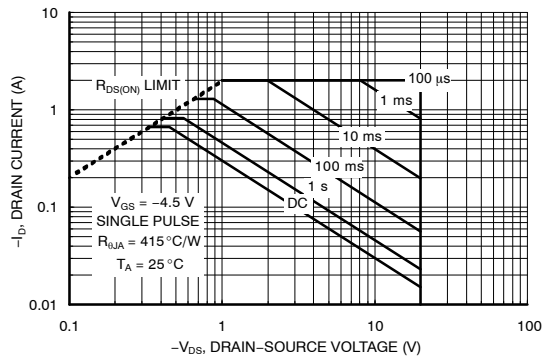


Figure 19. Maximum Safe Operating Area

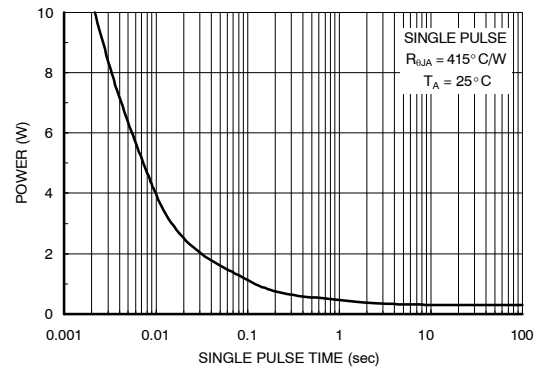
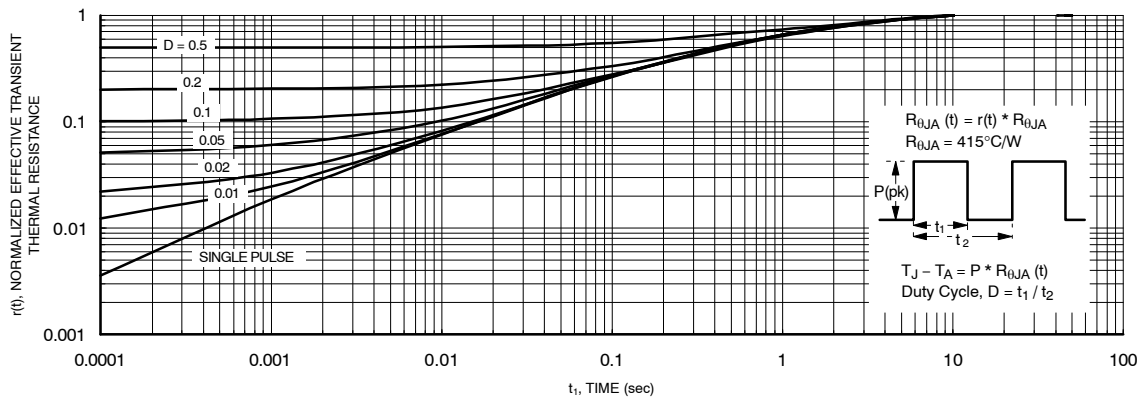


Figure 20. Single Pulse Maximum Power Dissipation



Thermal characterization performed using the conditions described in Note 1.
Transient thermal response will change depending on the circuit board design.

Figure 21. Transient Thermal Response Curve

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 2:1

SC-88/SC70-6/SOT-363
CASE 419B-02
ISSUE Y

DATE 11 DEC 2012

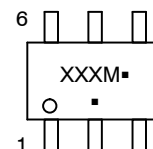


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.10	---	---	0.043
A1	0.00	---	0.10	0.000	---	0.004
A2	0.70	0.90	1.00	0.027	0.035	0.039
b	0.15	0.20	0.25	0.006	0.008	0.010
C	0.08	0.15	0.22	0.003	0.006	0.009
D	1.80	2.00	2.20	0.070	0.078	0.086
E	2.00	2.10	2.20	0.078	0.082	0.086
E1	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65 BSC			0.026 BSC		
L	0.26	0.36	0.46	0.010	0.014	0.018
L2	0.15 BSC			0.006 BSC		
aaa	0.15			0.006		
bbb	0.30			0.012		
ccc	0.10			0.004		
ddd	0.10			0.004		

GENERIC MARKING DIAGRAM*



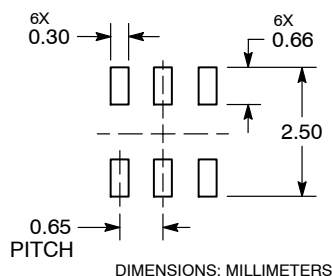
XXX = Specific Device Code
M = Date Code*
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

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SC-88/SC70-6/SOT-363
CASE 419B-02
ISSUE Y

DATE 11 DEC 2012

STYLE 1: PIN 1. EMITTER 2 2. BASE 2 3. COLLECTOR 1 4. EMITTER 1 5. BASE 1 6. COLLECTOR 2	STYLE 2: CANCELLED	STYLE 3: CANCELLED	STYLE 4: PIN 1. CATHODE 2. CATHODE 3. COLLECTOR 4. EMITTER 5. BASE 6. ANODE	STYLE 5: PIN 1. ANODE 2. ANODE 3. COLLECTOR 4. EMITTER 5. BASE 6. CATHODE	STYLE 6: PIN 1. ANODE 2 2. N/C 3. CATHODE 1 4. ANODE 1 5. N/C 6. CATHODE 2
STYLE 7: PIN 1. SOURCE 2 2. DRAIN 2 3. GATE 1 4. SOURCE 1 5. DRAIN 1 6. GATE 2	STYLE 8: CANCELLED	STYLE 9: PIN 1. EMITTER 2 2. EMITTER 1 3. COLLECTOR 1 4. BASE 1 5. BASE 2 6. COLLECTOR 2	STYLE 10: PIN 1. SOURCE 2 2. SOURCE 1 3. GATE 1 4. DRAIN 1 5. DRAIN 2 6. GATE 2	STYLE 11: PIN 1. CATHODE 2 2. CATHODE 2 3. ANODE 1 4. CATHODE 1 5. CATHODE 1 6. ANODE 2	STYLE 12: PIN 1. ANODE 2 2. ANODE 2 3. CATHODE 1 4. ANODE 1 5. ANODE 1 6. CATHODE 2
STYLE 13: PIN 1. ANODE 2. N/C 3. COLLECTOR 4. EMITTER 5. BASE 6. CATHODE	STYLE 14: PIN 1. VREF 2. GND 3. GND 4. IOUT 5. VEN 6. VCC	STYLE 15: PIN 1. ANODE 1 2. ANODE 2 3. ANODE 3 4. CATHODE 3 5. CATHODE 2 6. CATHODE 1	STYLE 16: PIN 1. BASE 1 2. EMITTER 2 3. COLLECTOR 2 4. BASE 2 5. EMITTER 1 6. COLLECTOR 1	STYLE 17: PIN 1. BASE 1 2. EMITTER 1 3. COLLECTOR 2 4. BASE 2 5. EMITTER 2 6. COLLECTOR 1	STYLE 18: PIN 1. VIN1 2. VCC 3. VOUT2 4. VIN2 5. GND 6. VOUT1
STYLE 19: PIN 1. IOUT 2. GND 3. GND 4. V CC 5. V EN 6. V REF	STYLE 20: PIN 1. COLLECTOR 2. COLLECTOR 3. BASE 4. EMITTER 5. COLLECTOR 6. COLLECTOR	STYLE 21: PIN 1. ANODE 1 2. N/C 3. ANODE 2 4. CATHODE 2 5. N/C 6. CATHODE 1	STYLE 22: PIN 1. D1 (i) 2. GND 3. D2 (i) 4. D2 (c) 5. VBUS 6. D1 (c)	STYLE 23: PIN 1. Vn 2. CH1 3. Vp 4. N/C 5. CH2 6. N/C	STYLE 24: PIN 1. CATHODE 2. ANODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE
STYLE 25: PIN 1. BASE 1 2. CATHODE 3. COLLECTOR 2 4. BASE 2 5. EMITTER 6. COLLECTOR 1	STYLE 26: PIN 1. SOURCE 1 2. GATE 1 3. DRAIN 2 4. SOURCE 2 5. GATE 2 6. DRAIN 1	STYLE 27: PIN 1. BASE 2 2. BASE 1 3. COLLECTOR 1 4. EMITTER 1 5. EMITTER 2 6. COLLECTOR 2	STYLE 28: PIN 1. DRAIN 2. DRAIN 3. GATE 4. SOURCE 5. DRAIN 6. DRAIN	STYLE 29: PIN 1. ANODE 2. ANODE 3. COLLECTOR 4. EMITTER 5. BASE/ANODE 6. CATHODE	STYLE 30: PIN 1. SOURCE 1 2. DRAIN 2 3. DRAIN 2 4. SOURCE 2 5. GATE 1 6. DRAIN 1

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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