PCN	N Nu	mber:	202	4060	5000.2						ate:	June 05, 2024	
Title	e:	Add Cu	as Al	terna	tive Wi	re Ba	ise Metal for	Selected D	evice	e(s)			
Cus	tom	er Conta	ct:	Cha	nge Ma	nage	ment team	Dept:	Qι	Quality Services			
Pro	pose	d 1st Shi	ip Da	ate:	Decem	ber	02, 2024	Sample requests accepted until:				05, 2024	
*Sa	ımple	e reques	ts re	eceiv	ed afte	r Jul	y 05, 2024 1	will not be	sup	ported.			
Cha	nge	Type:											
	Asse	embly Sit	e				Design			Wafe	r Bum	p Material	
	Asse	embly Pro	cess				Data Shee	t	Wa		Wafer Bump Process		
\square	Asse	embly Ma	teria	ls			Part numb	er change		Wafer Fab Site			
	Mec	hanical S	pecif	icatio	n		Test Site	<u> </u>		Wafe	r Fab l	Material	
	Packing/Shipping/Labeling						Test Proce	SS		Wafe	r Fab l	Process	
							•			•			

PCN Details

Description of Change:

Texas Instruments is pleased to announce the qualification of new assembly material set to add Cu as an additional bond wire option for devices listed in "Product affected" section below. Devices will remain in current assembly facility and piece part changes as follows:

Material	Current*	Proposed
Wire type	0.96mil Au, 1.0mil Cu	0.8mil Cu

Note: * - Au wire: Die to die bonding, Cu wire: Die to leadframe

Reason for Change:

Continuity of supply.

- 1) To align with world technology trends and use wiring with enhanced mechanical and electrical properties
- 2) Maximize flexibility within our Assembly/Test production sites.
- 3) Cu is easier to obtain and stock

Anticipated impact on Form, Fit, Function, Quality or Reliability (positive / negative):

None

Impact on Environmental Ratings:

Checked boxes indicate the status of environmental ratings following implementation of this change. If below boxes are checked, there are no changes to the associated environmental ratings.

RoHS	REACH	Green Status	IEC 62474
No Change	🔀 No Change	No Change	⊠ No Change

Changes to product identification resulting from this PCN:

None

Product Affected:

ISO1540QDRQ1 ISC	O1640BQDRQ1	ISO6720FBQDRQ1	ISO6721FBQDRQ1
ISO1541QDRQ1 ISO	O6720BQDRQ1	ISO6721BQDRQ1	UCC5350SBQDRQ1

Automotive Qualification Summary (As per AEC-Q100 and JEDEC Guidelines) Approve Date 01-May-2024

Product Attributes

Attributes	Qual Device:	QBS Package Reference:	QBS Package Reference:	QBS Process Reference:	QBS Product Reference:
Attributes	ISO6721RBQDRQ1	<u>ISO6721BQDRQ1</u>	TLV9022QDRQ1	UCC23513QDWYQ1	ISO1640QDWRQ1
Automotive Grade Level	Grade 1	Grade 1	Grade 1	Grade 1	Grade 1
Operating Temp Range (C)	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125
Product Function	Interface	Interface	Signal Chain	Power Management	Interface
Wafer Fab Supplier	RFAB, RFAB	MH8, MH8	RFAB	RFAB, RFAB	RFAB, RFAB
Assembly Site	MLA	MLA	MLA	TAI	MLA
Package Group	SOIC	SOIC	-	SOIC	SOIC
Package Designator	D	D	D	DWY	DW
Pin Count	8	8	8	6	16

QBS: Qual By Similarity

Qual Device ISO6721RBQDRQ1 is qualified at MSL2 260C

Qualification Results

			Date	פוט ג	<u>piayeu</u> as	: Nullibe	er or ic	ols / Total s	<u>ampie size</u>	<u>/ 10tai</u> 1a	illeu	
Туре	#	Test Spec	Min Lot	SS /	Test Name	Condition	Duration	Qual Device:	QBS Package Reference:	QBS Package Reference:	QBS Process Reference:	QBS Product Reference:
			Qty	Lot				ISO6721RBQDRQ1	ISO6721BQDRQ1	TLV9022QDRQ1	UCC23513QDWYQ1	ISO1640QDWRQ1
Test Group	A - Acc	elerated Enviror	ment Si	tress Te	sts							
PC	A1	JEDEC J- STD-020 JESD22- A113	3	77	Preconditioning	MSL1 260C	-	-	No Fails	No Fails	-	
HAST	A2	JEDEC JESD22- A110	3	77	Biased HAST	130C/85%RH	96 Hours	-	3/231/0	3/231/0	-	
AC/UHAST	А3	JEDEC JESD22- A102/JEDEC JESD22- A118	3	77	Autoclave	121C/15psig	96 Hours	-	3/231/0		-	
AC/UHAST	А3	JEDEC JESD22- A102/JEDEC JESD22- A118	3	77	Unbiased HAST	130C/85%RH	96 Hours		-	3/231/0		
TC-SAM	A4		3	3	Post TC SAM	<50% delamination	-	-	1/12/0	-	-	
HTSL	A6	JEDEC JESD22- A103	1	45	High Temperature Storage Life	150C	1000 Hours	-		3/135/0	-	
HTSL	A6	JEDEC JESD22- A103	1	45	High Temperature Storage Life	175C	500 Hours	-	3/135/0	-	-	
Test Group	B - Acc	elerated Lifetime	e Simula	tion Tes	ts	No.	3		702		30	
HTOL	B1	JEDEC JESD22- A108	3	77	Life Test	125C	1000 Hours	-	3/231/0	3/231/0	3/231/0	
ELFR	B2	AEC Q100- 008	3	800	Early Life Failure Rate	125C	48 Hours		-	-	3/2400/0	-
Test Group	C - Pac	kage Assembly	Integrity	Tests								
WBS	C1	AEC Q100- 001	1	30	Wire Bond Shear	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	1/30/0	3/228/0	3/90/0	-	1/30/0
WBP	C2	MIL-STD883 Method 2011	1	30	Wire Bond Pull	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	1/30/0	3/228/0	3/90/0	-	1/30/0

Туре	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device:	QBS Package Reference: ISO6721BQDRQ1	QBS Package Reference: TLV9022QDRQ1	QBS Process Reference: UCC23513QDWYQ1	QBS Product Reference: ISO1640QDWRQ1
SD	СЗ	JEDEC J- STD-002	1	15	PB Solderability	>95% Lead Coverage	-	-	1/15/0	-	-	-
SD	СЗ	JEDEC J- STD-002	1	15	PB-Free Solderability	>95% Lead Coverage	-	-	1/15/0	-	-	-
PD	C4	JEDEC JESD22- B100 and B108	3	10	Physical Dimensions	Cpk>1.67	-	1/10/0	3/30/0	3/30/0	-	
Test Group	D - Die F	abrication Relia	ability Te	sts								
ЕМ	D1	JESD61			Electromigration		-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
TDDB	D2	JESD35		-	Time Dependent Dielectric Breakdown		-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
HCI	D3	JESD60 & 28		-	Hot Carrier Injection		-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
ВТІ	D4	-	-		Bias Temperature Instability		-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
SM	D5	-		-	Stress Migration		-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
Test Group	E - Elect	rical Verificatio	n Tests									
ESD	E2	AEC Q100- 002	1	3	ESD HBM		2000 Volts	1/3/0	1/3/0	1/3/0	1/3/0	1/3/0
ESD	E3	AEC Q100- 011	1	3	ESD CDM	-	500 Volts	1/3/0	1/3/0	1/3/0	1/3/0	1/3/0
LU	E4	AEC Q100- 004	1	6	Latch-Up	Per AEC Q100-004	-	1/3/0	1/6/0	1/6/0	1/6/0	1/6/0
ED	E5	AEC Q100- 009	3	30	Electrical Distributions	Cpk>1.67 Room, hot, and cold	-	1/30/0	3/90/0	3/90/0	3/90/0	1/30/0

Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable

The following are equivalent HTOL options based on an activation energy of 0.7eV: 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours

The following are equivalent HTSL options based on an activation energy of 0.7eV:150C/1k Hours, and 170C/420 Hours

The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles

Ambient Operating Temperature by Automotive Grade Level:

Grade 0 (or E): -40C to +150C Grade 1 (or Q): -40C to +125C Grade 2 (or T): -40C to +105C Grade 3 (or I): -40C to +85C

E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):

Room/Hot/Cold: HTOL, ED

Room/Hot: THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU

Room: AC/uHAST

Quality and Environmental data is available at TI's external Web site: http://www.ti.com

Automotive Qualification Summary (As per AEC-Q100 and JEDEC Guidelines) Approve Date 05-April-2024

Product Attributes

Attributes	Qual Device:	Qual Device:	QBS Package Reference:	QBS Process Reference:	QBS Package Reference:	QBS Product Reference:	QBS Product Reference:	QBS Package Reference:	QBS Package Reference:	QBS Package, Process, Product Reference:	QBS Package Reference:
	UCC5350MCQDRQ1	UCC5350MCQDRQ1	IS06721BQDRQ1	UCC23513QDWYQ1	AMC22C12QDRQ1	UCC5390ECQDWVQ1	UCC5350MCQDRQ1	UCC21520QDWRQ1	ISO5452DWR	UCC5350SBQDRQ1	UCC21540QDWKRQ1
Automotive Grade Level	Grade 1	Grade 1	Grade 1	Grade 1	Grade 1	Grade 1	Grade 1	Grade 1	Grade 1	Grade 1	Grade 1
Operating Temp Range (C)	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125
Product Function	Signal Chain	Signal Chain	Interface	Power Management	Signal Chain	Interface	Interface	Power Management	Power Management	Signal Chain	Power Management
Wafer Fab Supplier	RFAB, RFAB	RFAB, RFAB	MH8, MH8	RFAB, RFAB	MH8, DMOS6	DP1DM5, DP1DM5	DP1DM5, DP1DM5	DP1DM5, DP1DM5, DP1DM5	DP1DM5, DP1DM5, MH8	RFAB, RFAB	MH8, MH8, MH8
Assembly Site	TAI	MLA	MLA	TAI	MLA	TAI	TAI	TAI	MLA	MLA	TAI
Package Group	SOIC	SOIC	SOIC	SOIC	SOIC	SOIC	SOIC	SOIC	SOIC	SOIC	SOIC
Package Designator	D	D	D	DWY	D	DWV	D	DW	DW	D	DWK
Pin Count	8	8	8	6	8	8	8	16	16	8	14

QBS: Qual By Similarity

Qual Device UCC5350MCQDRQ1 is qualified at MSL2 260C Qual Device UCC5350MCQDRQ1 is qualified at MSL2 260C

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

						ta Di	Spic	iycu as			003 / 10							
Туре		Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: UCC5350MCQDRQ1	Qual Device: UCC5350MCQDRQ1	QBS Package Reference: ISO6721BQDRQ1	QBS Process Reference: UCC23513QDWYQ1	QBS Package Reference: AMC22C12QDRQ1	QBS Product Reference: UCC5390ECQDWVQ1	QBS Product Reference: UCC5350MCQDRQ1	QBS Package Reference: UCC21520QDWRQ1	QBS Package Reference:	QBS Package, Process, Product Reference: UCC5350SBODRO1	QBS Package Reference: UCC21540QDWKRO
Test Group	A - Acce	lerated Environ	ment Stre	ss Tes	ts													
rest Group	n nocc	JEDEC J-	incin ou c	.55 105				-						0.				
PC	A1	STD-020 JESD22- A113	3	77	Preconditioning	MSL1 260C	n .	tik	8	3/0/0	5	•		es.			•	
PC	A1	JEDEC J- STD-020 JESD22- A113	3	77	Preconditioning	MSL2 260C			1/0/0			3/0/0			3/0/0	1/0/0		1/0/0
HAST	A2	JEDEC JESD22- A110	3	77	Biased HAST	130C/85%RH	96 Hours	-	5	-		-	-			1/77/0	-	2/154/0
AC/UHAST	A3	JEDEC JESD22- A102/JEDEC JESD22- A118	3	77	Autoclave	121C/15psig	96 Hours	21	-	3/231/0	-	-	(2)			1/77/0	-	3/231/0
AC/UHAST	A3	JEDEC JESD22- A102/JEDEC JESD22- A118	3	77	Unbiased HAST	130C/85%RH	96 Hours	•				3/231/0						
тс	A4	JEDEC JESD22- A104 and Appendix 3	3	77	Temperature Cycle	-65C/150C	500 Cycles	-	-	-		-	-		1/77/0	-		2/154/0
TC-BP	A4	MIL-STD883 Method 2011	1 !	5	Post Temp Cycle Bond Pull	-	21	-	-		-		-		1/5/0		-	-
TC-SAM	A4		3	3	Post TC SAM	<50% delamination			-	1/12/0							-	
HTSL	A6	JEDEC JESD22- A103	1 .	45	High Temperature Storage Life	150C	1000 Hours		-		-	3/135/0			-	1/45/0	-	1/45/0
HTSL	A6	JEDEC JESD22- A103	1	45	High Temperature Storage Life	175C	500 Hours	-	-	3/135/0	-	-	-	-	-	-	-	-
Test Group	B - Acce	lerated Lifetime	Simulation	on Test	s													
HTOL	B1	A108	3		Life Test	125C	1000 Hours	-	1/77/0	-	3/231/0		1/77/0	-			-	
ELFR	B2	AEC Q100- 008	3 1	800	Early Life Failure Rate	125C	48 Hours	-	-	-	3/2400/0	-	-	-	-		-	-
Test Group	C - Pack	age Assembly I	integrity T	ests														
WBS	C1	AEC Q100- 001		30	Wire Bond Shear	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	1/30/0	1/30/0	3/228/0	-	3/90/0	-				1/30/0	3/90/0
WBP	C2	MIL-STD883 Method 2011	1 :	30	Wire Bond Pull	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	1/30/0	1/30/0	3/228/0	-	3/90/0					1/30/0	3/90/0
SD	СЗ	JEDEC J- STD-002	1	15	PB Solderability	>95% Lead Coverage				1/15/0								
SD	СЗ	JEDEC J-										1/15/0		-		-		
PD		STD-002	1	15	PB-Free Solderability	>95% Lead Coverage				1/15/0	-	1/15/0						
	C4	JEDEC JESD22- B100 and B108		15	PB-Free Solderability Physical Dimensions	>95% Lead		1/10/0	1/10/0	1/15/0							- 1/10/0	
Test Group		JEDEC JESD22- B100 and	3	10	Solderability	>95% Lead Coverage	-	1/10/0	1/10/0			1/15/0					1/10/0	
Test Group		JEDEC JESD22- B100 and B108	3	10	Solderability	>95% Lead Coverage	-	. 1/10/0 Completed Per Process Technology Requirements	2/10/0 Completed Per Process Technology Requirements		Completed Per Process Technology Requirements	1/15/0	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	- Completed Per Process Technology Requirements		- Completed Per Process Technology Requirements
	D - Die Fi	JEDEC JESD22- B100 and B108 abrication Relia	3	10	Solderability Physical Dimensions	>95% Lead Coverage		Completed Per Process Technology	Completed Per Process Technology	3/30/0 Completed Per Process Technology	Process Technology	1/15/0 2/30/0 Completed Per Process Technology	Process Technology	Process Technology	Process Technology	Per Process Technology	Completed Per Process Technology	Process Technology
ЕМ	D - Die Fi	JEDEC JESD22- B100 and B108 abrication Relia	3	10	Solderability Physical Dimensions Electromigration Time Dependent Dielectric	>95% Lead Coverage	-	Completed Per Process Technology Requirements Completed Per Process Technology	Completed Per Process Technology Requirements Completed Per Process Technology	3/30/0 Completed Per Process Technology Requirements Completed Per Process Technology	Process Technology Requirements Completed Per Process Technology	2/15/0 3/30/0 Completed Per Process Technology Requirements Completed Per Process Technology	Process Technology Requirements Completed Per Process Technology	Process Technology Requirements Completed Per Process Technology	Process Technology Requirements Completed Per Process Technology	Per Process Technology Requirements Completed Per Process Technology	Completed Per Process Technology Requirements Completed Per Process Technology	Process Technology Requirements Completed Per Process Technology
EM	D - Die Fi	JESD61 JESD61 JESD61 JESD60 &	3	10	Physical Dimensions Electromigration Time Dependent Dielectric Breakdown Hot Carrier	>95% Lead Coverage	-	Completed Per Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Technology	Completed Per Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Technology Requirements	3/30/0 Completed Per Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Technology	Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Technology	1/15/0 3/30/0 Completed Per Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Technology Requirements	Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Technology	Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Technology	Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Technology	Per Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Technology	Completed Per Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Technology	Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Technology
TDDB	D - Die Fi	JESD61 JESD61 JESD61 JESD60 &	3	10	Physical Dimensions Electromigration Time Dependent Delectric Breakfown Hot Carrier Injection Bias Temperature	>95% Lead Coverage	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements Completed Per Process Technology	3/30/0 Completed Per Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Completed Per Process Completed Per Process Technology Requirements Technology Requirements Technology Requirements	Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Technology Completed Per Process Technology Requirements	2/15/0 3/30/0 Completed Per Process Technology Requirements Completed Per Process Technology Tech	Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Technology Completed Per Process Technology	Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Technology Requirements	Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Technology Completed Per Process Technology	Per Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Technology	Completed Per Process Technology Requirements Completed Per Process Technology	Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Technology
TDDB HCI BTI SM	D - Die Fi D1 D2 D3	JEDEC JESD22 JESD22 BIJ00 and BIJ00 and BIJ00 and BIJ00 and BIJ00 abrication Relia JESD61 JESD61 JESD60 &	3	10	Physical Dimensions Electromigration Time Dependent Delectric Breakform Hot Carrier Injection Bias Temperature Instability	>95% Lead Coverage	-	Completed Per Process Technology Requirements Completed Per Process Technology Requirements	Completed Per Process Technology Requirements Completed Per Process Technology Requirements	Completed Per Process Technology Requirements Completed Per Process Completed Per	Process Technology Requirements Completed Per Process Technology Requirements	3/30/0 Completed Per Process Process Process Requirements Completed Per Process Rectanglements Completed Per Process Rectanglements Rectanglements Rectanglements Completed Per Process Rectanglements Rectanglements Completed Per Process Rectanglements	Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Technology	Process Technology Requirements Completed Per Process Technology Requirements	Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Technology Requirements	Per Process Technology Requirements Completed Per Process Technology Technology	Completed Per Process Technology Requirements	Process Technology Requirements Completed Per Process Technology Requirements
TDDB HCI BTI SM	D - Die Fi D1 D2 D3 D4 D5 E - Electr	JEDEC JESD22- JESD22- JESD23- B100 and B100 B100 B100 B100 B100 B100 B100 B10	3 ibility Test	-	Physical Directions Bias Temperature Instability Bias Temperature Instability Bias Temperature Instability Stress Migration	>95% Lead Coverage	-	Completed Per Process Technology Requirements Completed Per Process Technology Requirements	Completed Per Process Technology Requirements Completed Per Process Technology Requirements	Completed Per Process Technology Requirements Completed Per Process Completed Per	Process Technology Requirements Completed Per Process Technology Requirements	3/30/0 Completed Per Process Process Process Requirements Completed Per Process Rectanglements Completed Per Process Rectanglements Rectanglements Rectanglements Completed Per Process Rectanglements Rectanglements Completed Per Process Rectanglements	Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Technology Requirements	Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Technology Requirements	Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Technology Requirements	Per Process Technology Requirements Completed Per Process Technology Technology	Completed Per Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Technology Requirements Completed Per Requirements Completed Per Requirements Completed Per Requirements Completed Per Requirements Requirements Requirements Requirements Requirements Requirements Requirements Requirements Requirements	Process Technology Requirements Completed Per Process Technology Requirements
TDDB HCI BTI SM	D - Die Fi D1 D2 D3 D4	JEDEC JESD2- JESD2- JESD2- BLOG and JESD61 JESD60 & 28	3 shifty Test		Physical Dimensions Electromigration Time Dependent Delectric Breakform Hot Carrier Injection Bias Temperature Instability	>95% Lead Coverage	Volts 500	Completed Per Process Technology Requirements Completed Per Process Technology Requirements	Completed Per Process Technology Requirements Completed Per Process Technology Requirements	Completed Per Process Technology Requirements Completed Per Process Completed Per	Process Technology Requirements Completed Per Process Technology Requirements	3/30/0 Completed Per Process Process Process Requirements Completed Per Process Rectanglements Completed Per Process Rectanglements Rectanglements Rectanglements Completed Per Process Rectanglements Rectanglements Completed Per Process Rectanglements	Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Technology	Process Technology Requirements Completed Per Process Technology Requirements	Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Technology Requirements	Per Process Technology Requirements Completed Per Process Technology Technology	Completed Per Process Technology Requirements	Process Technology Requirements Completed Per Process Technology Requirements
TDDB HCI BTI SM Test Group	D - Die Fi D1 D2 D3 D4 D5 E - Electr	JEDEC JESD22- BID0 and BID0 an	3 : Ibility Tests 1 : I		Solderability Physical Dimensions Electromigration Time Dependent Dependent Breakdown Hot Carrier Injection Blass Temperature Instability ESD HBM	>95% Lead Coverage	Volts	Completed Per Process Technology Requirements Completed Per Process Technology Requirements	Completed Per Process Technology Requirements Completed Per Process Technology Requirements	Completed Per Process Technology Requirements Completed Per Process Completed Per	Process Technology Requirements Completed Per Process Technology Requirements	3/30/0 Completed Per Process Process Process Requirements Completed Per Process Rectanglements Completed Per Process Rectanglements Rectanglements Rectanglements Completed Per Process Rectanglements Rectanglements Completed Per Process Rectanglements	Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Technology Requirements	Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Technology Requirements	Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Technology Requirements	Per Process Technology Requirements Completed Per Process Technology Technology	Completed Per Process Technology Requirements	Process Technology Requirements Completed Per Process Technology Requirements

Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable

The following are equivalent HTOL options based on an activation energy of 0.7eV: 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours

The following are equivalent HTSL options based on an activation energy of 0.7eV : 150C/1k Hours, and 170C/420 Hours

The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycle Ambient Operating Temperature by Automotive Grade Level:

Grade 0 (or E): -40C to +150C Grade 1 (or Q): -40C to +125C Grade 2 (or T): -40C to +105C Grade 3 (or I): -40C to +85C

E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):

Room/Hot/Cold: HTOL, ED

Room/Hot: THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU

Room: AC/uHAST

Quality and Environmental data is available at TI's external Web site: http://www.ti.com/

Qualification Report

Automotive Qualification Summary
(As per AEC-Q100 and JEDEC Guidelines)
Approve Date 19-October-2023

Product Attributes

Attributes	Qual Device:	Qual Device:	QBS Process Reference:	QBS Process Reference:	QBS Product Reference:
Attributes	ISO6763QDWRQ1	UCC21540QDWKRQ1	UCC23513QDWYQ1	IS07741FQDWQ1	ISO6763QDWRQ1
Automotive Grade Level	Grade 1	Grade 1	Grade 1	Grade 1	Grade 1
Operating Temp Range (C)	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125
Product Function	Interface	Power Management	Power Management	Interface	Interface
Wafer Fab Supplier	RFAB, RFAB	MH8, MH8, MH8	RFAB, RFAB	MH8, MH8	RFAB, RFAB
Assembly Site	MLA	TAI	TAI	TAI	MLA
Package Group	SOIC	SOIC	SOIC	SOIC	SOIC
Package Designator	DW	DWK	DWY	DW	DW
Pin Count	16	14	6	16	16

QBS: Qual By Similarity

Qual Device ISO6763QDWRQ1 is qualified at MSL2 260C Qual Device UCC21540QDWKRQ1 is qualified at MSL3 260C

Qualification Results

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Туре		Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: ISO6763QDWRQ1	Qual Device: UCC21540QDWKRQ1	QBS Process Reference: UCC23513QDWYQ1	QBS Process Reference: ISO7741FQDWQ1	QBS Product Reference: ISO6763QDWRQ1
Test Group	A - Acc	elerated Enviror	nment S	tress Te	sts				61	***	'	22
PC	A1	JEDEC J- STD-020 JESD22- A113	3	77	Preconditioning	MSL2 260C		No Fails	No Fails		-	No Fails
HAST	A2	JEDEC JESD22- A110	3	77	Biased HAST	130C/85%RH	96 Hours	3/231/0	3/231/0	-	-	1/77/0
AC/UHAST	A3	JEDEC JESD22- A102/JEDEC JESD22- A118	3	77	Autoclave	121C/15psig	96 Hours	3/231/0	3/231/0	-	-	1/77/0
тс	A4	JEDEC JESD22- A104 and Appendix 3	3	77	Temperature Cycle	-65C/150C	500 Cycles	3/231/0	3/231/0		-	1/77/0
TC-BP	A4	MIL-STD883 Method 2011	1	5	Post Temp Cycle Bond Pull	-	-	1/5/0	1/5/0	-	-	1/5/0
HTSL	A6	JEDEC JESD22- A103	1	45	High Temperature Storage Life	150C	1000 Hours	3/135/0	3/135/0	-	-	-
HTSL	A6	JEDEC JESD22- A103	1	45	High Temperature Storage Life	175C	500 Hours	-	-	-	-	1/45/0

Test Group	B - Acc	elerated Lifetim	e Simula	tion Tes	ts		20					
HTOL	B1	JEDEC JESD22- A108	3	77	Life Test	125C	1000 Hours	-		3/231/0	3/231/0	-
ELFR	B2	AEC Q100- 008	3	800	Early Life Failure Rate	125C	48 Hours	-	-	3/2400/0	3/2400/0	- 1
Test Group	C - Paci	kage Assembly	Integrity	Tests							·	Li-
WBS	C1	AEC Q100- 001	1	30	Wire Bond Shear	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	3/90/0	3/90/0	3/90/0	3/90/0	-
WBP	C2	MIL-STD883 Method 2011	1	30	Wire Bond Pull	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	3/90/0	3/90/0	3/90/0	3/90/0	-
SD	C3	JEDEC J- STD-002	1	15	PB Solderability	>95% Lead Coverage	-	-	-	1/15/0	-	1/15/0
SD	СЗ	JEDEC J- STD-002	1	15	PB-Free Solderability	>95% Lead Coverage	-	-	-	1/15/0	-	1/15/0
PD	C4	JEDEC JESD22- B100 and B108	3	10	Physical Dimensions	Cpk>1.67	-	-	-	3/30/0	-	-
Test Group	D - Die I	Fabrication Relia	ability Te	ests				·				
EM	D1	JESD61	-	-	Electromigration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
TDDB	D2	JESD35	-		Time Dependent Dielectric Breakdown	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
HCI	D3	JESD60 & 28	-	-	Hot Carrier Injection	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
NBTI	D4	-	-	-	Negative Bias Temperature Instability	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
SM	D5	-	-	-	Stress Migration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
Test Group	E - Elec	trical Verificatio	n Tests									
ESD	E2	AEC Q100- 002	1	3	ESD HBM	-	2000 Volts	Device specific data [1]	Device specific data [1]	-	-	1/3/0
ESD	E3	AEC Q100- 011	1	3	ESD CDM	-	1500 Volts	Device specific data [1]	Device specific data [1]	-	-	1/3/0
LU	E4	AEC Q100- 004	1	6	Latch-Up	Per AEC Q100-004	-	Device specific data [1]	Device specific data [1]	-	-	1/6/0
ED	E5	AEC Q100- 009	3	30	Electrical Distributions	Cpk>1.67 Room, hot, and cold	-	3/90/0	3/90/0	3/90/0	3/90/0	-

Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable

The following are equivalent HTOL options based on an activation energy of 0.7eV: 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours

The following are equivalent HTSL options based on an activation energy of 0.7eV : 150C/1k Hours, and 170C/420 Hours

The following are equivalent Temp Cycle options per JESD47: -55C/125C/700 Cycles and -65C/150C/500 Cycles Ambient Operating Temperature by Automotive Grade Level:

Grade 0 (or E): -40C to +150C Grade 1 (or Q): -40C to +125C Grade 2 (or T): -40C to +105C Grade 3 (or I): -40C to +85C

E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):

Room/Hot/Cold: HTOL, ED

Room/Hot: THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU

Room: AC/uHAST

Quality and Environmental data is available at TI's external Web site: http://www.ti.com/

[1] Change from hybrid Au and Cu wires to full Cu wire in assembly will not impact HBM, CDM, and LU result.

Automotive Qualification Summary (As per AEC-Q100 and JEDEC Guidelines) Approve Date 16-June-2023

Product Attributes

Attributes	Qual Device:	Qual Device:	QBS Reference:	QBS Reference:	QBS Reference:	QBS Reference:	QBS Reference:
Attributes	UCC21520QDWRQ1	ISO5452DWR	UCC21520QDWQ1	IS05851QDWQ1	TMP451AQDQERQ1	AMC1305M25QDWQ1	AMC1305M25QDWQ1
Automotive Grade Level	Grade 1	Grade 1	Grade 1	Grade 1	Grade 1	Grade 1	Grade 1
Operating Temp Range (C)	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125
Product Function	Power Management	Power Management	Power Management	Interface	Power Management	Signal Chain	Signal Chain
Wafer Fab Supplier	DP1DM5, DP1DM5, DP1DM5	DP1DM5, DP1DM5, MH8	DP1DM5, DP1DM5, DP1DM5	MH8, DP1DM5, DP1DM5	DP1DM5	DP1DM5, DP1DM5, AIZU	DP1DM5, DP1DM5, AIZU
Assembly Site	TAI	MLA	TAI	TAI	UTL1	MLA	TAI
Package Group	SOIC	SOIC	SOIC	SOIC	QFN	SOIC	SOIC
Package Designator	DW	DW	DW	DW	DQF	DW	DW
Pin Count	16	16	16	16	8	16	16

QBS: Qual By Similarity

Qual Device UCC21520QDWRQ1 is qualified at MSL2 260C Qual Device ISO5452DWR is qualified at MSL2 260C

Qualification Results

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Туре	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: UCC21520QDWRQ1	Qual Device: ISO5452DWR	QBS Reference: UCC21520QDWQ1	QBS Reference: ISO5851QDWQ1	QBS Reference: TMP451AQDQFRQ1	QBS Reference: AMC1305M25QDWQ1	QBS Reference: AMC1305M25QDWC
Test Group	A - Acce	elerated Environ	ment Si	tress Te	sts			·						
PC	A1	JEDEC J- STD-020 JESD22- A113	3	77	Preconditioning	MSL1 260C	-	-	-	-	-	No Fails	-	-
PC	A1	JEDEC J- STD-020 JESD22- A113	3	77	Preconditioning	MSL2 260C	-	No Fails	No Fails	No Fails	No Fails	-	-	-
PC	A1	JEDEC J- STD-020 JESD22- A113	3	77	Preconditioning	MSL3 260C	-			ā		=	3/0/0	3/0/0
HAST	A2	JEDEC JESD22- A110	3	77	Biased HAST	130C/85%RH	96 Hours	-	1/77/0	-	3/231/0	3/231/0	3/231/0	3/231/0
AC/UHAST	A3	JEDEC JESD22- A102/JEDEC JESD22- A118	3	77	Autoclave	121C/15psig	96 Hours	-	1/77/0	1/77/0	1/77/0	3/231/0	3/231/0	3/231/0
тс	A4	JEDEC JESD22- A104 and Appendix 3	3	77	Temperature Cycle	-65C/150C	500 Cycles	1/77/0	1/77/0	1/77/0	1/77/0	3/231/0	3/231/0	3/231/0
TC-BP	A4	MIL-STD883 Method 2011	1	5	Post Temp Cycle Bond Pull			1/5/0	1/5/0		-	1/5/0	1/5/0	1/5/0
HTSL	A6	JEDEC JESD22- A103	1	45	High Temperature Storage Life	150C	1000 Hours		1/45/0	-	-		3/135/0	3/135/0
HTSL	A6	JEDEC JESD22- A103	1	45	High Temperature Storage Life	175C	500 Hours	-	-	2	1/45/0	1/45/0	-	-
Test Group	B - Acc	elerated Lifetime	e Simula	tion Tes	ts			*			•			
HTOL	B1	JEDEC JESD22- A108	1	77	Life Test	125C	1000 Hours	2	-	2	3/231/0	-	-	-
HTOL	B1	JEDEC JESD22- A108	1	77	Life Test	150C	408 Hours	-			-	3/231/0	-	
ELFR	B2	AEC Q100- 008	1	77	Early Life Failure Rate	125C	48 Hours	-	-	-	3/2400/0			
ELFR	B2	AEC Q100- 008	1	77	Early Life Failure Rate	150C	24 Hours	-				3/2400/0	-	
Test Group	C - Paci	kage Assembly	Integrity	Tests										
WBS	C1	AEC Q100- 001	1	30	Wire Bond Shear	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	1/30/0	1/30/0		1/30/0	3/90/0	3/90/0	3/90/0
WBP	C2	MIL-STD883 Method 2011	1	30	Wire Bond Pull	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	1/30/0	1/30/0	ō	1/30/0	3/90/0	3/90/0	3/90/0
SD	C3	JEDEC J- STD-002	1	15	PB Solderability	>95% Lead Coverage		-		-	-	-	-	2)
SD	C3	JEDEC J- STD-002	1	15	PB-Free Solderability	>95% Lead Coverage		-				-	-	
PD	C4	JEDEC JESD22- B100 and B108	1	10	Physical Dimensions	Cplc>1.67		ā	-	ō	1/10/0	3/30/0	ī.	5.0
est Group	D - Die I	Fabrication Relia	ability Te	sts										

ЕМ	D1	JESD61			Electromigration		-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
TDDB	D2	JESD35			Time Dependent Dielectric Breakdown		-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
HCI	D3	JESD60 & 28			Hot Carrier Injection	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
NBTI	D4	-			Negative Bias Temperature Instability	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
SM	D5				Stress Migration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
Test Group	E - Elect	rical Verification	n Tests											
ESD	E2	AEC Q100- 002	1	3	ESD HBM	-	2000 Volts	Device specific data [1]	Device specific data [1]	1/3/0	1/3/0	1/3/0	-	-
ESD	E3	AEC Q100- 011	1	3	ESD CDM	-	500 Volts	Device specific data [1]	Device specific data [1]	1/3/0	1/3/0	1/3/0	-	-
LU	E4	AEC Q100- 004	1	6	Latch-Up	Per AEC Q100-004	-	Device specific data [1]	Device specific data [1]	1/6/0	1/6/0	1/6/0	-	-
ED	E5	AEC Q100- 009	3	30	Electrical Distributions	Cpk>1.67 Room, hot, and cold	-	1/30/0	1/30/0	1/30/0	1/30/0	3/90/0	3/90/0	3/90/0

Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable

The following are equivalent HTOL options based on an activation energy of 0.7eV: 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours

The following are equivalent HTSL options based on an activation energy of 0.7eV: 150C/1k Hours, and 170C/420 Hours

The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles Ambient Operating Temperature by Automotive Grade Level:

Grade 0 (or E): -40C to +150C Grade 1 (or Q): -40C to +125C Grade 2 (or T): -40C to +105C Grade 3 (or I): -40C to +85C

E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):

Room/Hot/Cold: HTOL, ED

Room/Hot: THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU

Room: AC/uHAST

Quality and Environmental data is available at TI's external Web site: http://www.ti.com/

TI Qualification ID: R-CHG-2203-108

[1] Qual Device: UCC21520QDWRQ1 and QBS Reference: UCC21520QDWQ1 use the same silicon die and bondout. Qual Device: ISO5452DWR and QBS Reference: ISO5851QDWQ1 use the same silicon die and bondout.

Qualification Report

Automotive Qualification Summary (As per AEC-Q100, AEC-Q006, and JEDEC Guidelines) Approve Date 28-April-2023

Qualification Results

			. ,				- 1				
	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: AMC1305M25QDWQ1	Qual Device: AMC1305M25QDWQ1			
Test Group A - Accelerated Environment Stress Tests											
A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	MSL3 260C	1 Step	No Fails	No Fails			
A1.1	-	3	22	SAM Precon Pre	Review for delamination	1 Step	3/66/0	3/66/0			
A1.2	-	3	22	SAM Precon Post	Review for delamination	1 Step	3/66/0	3/66/0			
A2.1	JEDEC JESD22- A110	3	77	Biased HAST	130C/85%RH	96 Hours	-	-			
	Oup A - A A1 A1.1 A1.2	# Test Spec oup A - Accelerated Environme A1	# Test Spec Min Lot Qty oup A - Accelerated Environment Stres A1 JEDEC J-STD-020 3 A1.1 - 3 A1.2 - 3 JEDEC JESD22- 3	# Test Spec	# Test Spec Min Lot Qty SS / Lot Test Name oup A - Accelerated Environment Stress Tests A1	# Test Spec Min Lot Qty SS / Lot Test Name Condition oup A - Accelerated Environment Stress Tests A1	# Test Spec Min Lot Qty SS / Lot Test Name Condition Duration oup A - Accelerated Environment Stress Tests A1	# Test Spec Min Lot Qty SS / Lot Test Name Condition Duration Qual Device: AMC1305M25QDWQ1 oup A - Accelerated Environment Stress Tests A1			

HAST	A2.1.2	-	3	1	Cross Section, post bHAST, 1X	Post stress cross section	Completed	-	-
HAST	A2.1.3	-	3	30	Wire Bond Shear, post bHAST, 1X	Post stress	Wires	-	-
HAST	A2.1.4	-	3	30	Bond Pull over Stitch, post bHAST, 1X	Post stress	Wires	-	-
HAST	A2.1.5	-	3	30	Bond Pull over Ball, post bHAST, 1X	Post stress	Wires	-	-
HAST	A2.2	JEDEC JESD22- A110	3	77	Biased HAST	130C/85%RH	192 Hours	3/231/0	3/231/0
HAST	A2.2.1	-	3	22	SAM Analysis, post bHAST 2X	Review for delamination	Completed	3/66/0	3/66/0
HAST	A2.2.2	-	3	1	Cross Section, post bHAST, 2X	Post stress cross section	Completed	3/3/0	3/3/0
HAST	A2.2.3	-	3	30	Wire Bond Shear, post bHAST, 2X	Post stress	Wires	3/9/0	3/9/0
HAST	A2.2.4	-	3	30	Bond Pull over Stitch, post bHAST, 2X	Post stress	Wires	3/9/0	3/9/0
HAST	A2.2.5	-	3	30	Bond Pull over Ball, post bHAST, 2X	Post stress	Wires	3/9/0	3/9/0
тс	A4.1	JEDEC JESD22- A104 and Appendix 3	3	77	Temperature Cycle	-65C/150C	500 Cycles	3/231/0	3/231/0
тс	A4.1.1	-	3	22	SAM Analysis, post TC 1X	Review for delamination	Completed	-	-
тс	A4.1.2	-	3	1	Cross Section, post TC, 1X	Post stress cross section	Completed	-	-
тс	A4.1.3	-	3	30	Wire Bond Shear, post TC, 1X	Post stress	Wires	-	-
тс	A4.1.4	-	3	30	Bond Pull over Stitch, post TC, 1X	Post stress	Wires	-	-
тс	A4.1.5	-	3	30	Bond Pull over Ball, post TC, 1X	Post stress	Wires	-	-
тс	A4.2	JEDEC JESD22- A104 and Appendix 3	3	77	Temperature Cycle	-65C/150C	1000 Cycles	3/210/0	3/210/0
тс	A4.2.1	-	3	22	SAM Analysis, post TC, 2X	Review for delamination	Completed	3/66/0	3/66/0
тс	A4.2.2	-	3	1	Cross Section, post TC, 2X	Post stress cross section	Completed	3/3/0	3/3/0
тс	A4.2.3	-	3	30	Wire Bond Shear, post TC, 2X	Post stress	Wires	3/9/0	3/9/0
тс	A4.2.4	-	3	30	Bond Pull over Stitch, post TC, 2X	Post stress	Wires	3/9/0	3/9/0
тс	A4.2.5	-	3	30	Bond Pull over Ball, post TC, 2X	Post stress	Wires	3/9/0	3/9/0
HTSL	A6.1	JEDEC JESD22- A103	3	45	High Temperature Storage Life	150C	1000 Hours	3/135/0	3/135/0
HTSL	A6.1.1	-	3	1	Cross Section, post HTSL, 1X	Post stress cross section	Completed	-	-
HTSL	A6.2	JEDEC JESD22- A103	3	45	High Temperature Storage Life	150C	2000 Hours	3/132/0	3/132/0
HTSL	A6.2.1	-	3	1	Cross Section, post HTSL, 2X	Post stress cross section	Completed	3/3/0	3/3/0

Test G	Test Group B - Accelerated Lifetime Simulation Tests											
Test G	roup C - F	Package Assembly Inte	grity Te	sts								
WBS	C1	AEC Q100-001	1	30	Wire Bond Shear	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	3/90/0	3/90/0			
WBP	C2	MIL-STD883 Method 2011	1	30	Wire Bond Pull	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	3/90/0	3/90/0			
SD	СЗ	JEDEC J-STD-002	1	15	PB Solderability	>95% Lead Coverage	-	-	-			
SD	C3	JEDEC J-STD-002	1	15	PB-Free Solderability	>95% Lead Coverage	-	-	-			
PD	C4	JEDEC JESD22- B100 and B108	1	10	Physical Dimensions	Cpk>1.67	-	-	-			
Test G	roup D - [Die Fabrication Reliabili	ty Tests									
EM	D1	JESD61	-	-	Electromigration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements			
TDDB	D2	JESD35	-	-	Time Dependent Dielectric Breakdown	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements			
нсі	D3	JESD60 & 28	-	-	Hot Carrier Injection	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements			
NBTI	D4	-	-	-	Negative Bias Temperature Instability	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements			
SM	D5	-	-	-	Stress Migration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements			

QBS: Qual By Similarity

Qual Device AMC1305M25QDWQ1 is qualified at MSL3 260C

Qual Device AMC1305M25QDWQ1 is qualified at MSL3 260C

Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable

The following are equivalent HTOL options based on an activation energy of 0.7eV: 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours

The following are equivalent HTSL options based on an activation energy of 0.7eV : 150C/1k Hours, and 170C/420 Hours

The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles Ambient Operating Temperature by Automotive Grade Level:

Grade 0 (or E): -40C to +150C Grade 1 (or Q): -40C to +125C Grade 2 (or T): -40C to +105C Grade 3 (or I): -40C to +85C

E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):

Room/Hot/Cold: HTOL, ED

Room/Hot: THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU

Room: AC/uHAST

Quality and Environmental data is available at TI's external Web site: http://www.ti.com/

Automotive Qualification Summary (As per AEC-Q100 and JEDEC Guidelines) (Q100, Q006, Grade 1, -40/125C) Approved 21-Dec-2023

Qualification Results

			Data L)ispla	ıl sample size ,	/ Total failed				
	Туре	#	Test Spec	Min Lot Qty	\$\$/Lot	Test Name / Condition	Duration	Qual Device: UCC21330BQDRQ1	QB\$ Reference Device: TLV9022QDRQ1	QBS Reference Device: ISO6721BQDRQ1
		Test (Group A – A	cceler	ated Envi	ronment Stress Tes	its			
	PC	A1	-	3	22	SAM Analysis, Pre Stress	Completed	3/66/0	3/86/0	-
	PC	A1	JEDEC J- STD-020 JESD22- A113	3	77	Preconditioning	Level 2- 260C	No fails	No fails	No fails
П	PC	A1	-	3	22	SAM Analysis, Post Stress	Completed	3/86/0	3/86/0	2/44/0
	HAST	A2	JEDEC JESD22- A110	3	77	Biased HAST, 130C/85%RH	96 Hours	-	3/231/0	3/231/0
	HAST	A2	-	3	1	Cross Section, Post bHAST 96 Hours	Completed	-	-	-
	HAST	A2	-	3	30	Wire Bond Shear, Post bHast 98 Hours	Wires	-	-	-
	HAST	A2	-	3	30	Bond Pull over Stitch, post bHAST, 96 Hours	Wires	-	-	-
	HAST	A2	-	3	30	Bond Pull over Ball, Post bHAST, 96 Hours	Wires	-	-	-
	HAST	A2	JEDEC JESD22- A110	3	77	Biased HAST, 130C/85%RH	192 Hours	-	3/210/0	3/210/0
	HAST	A2	-	3	1	Cross Section, Post bHAST 192 Hours	Completed	-	3/3/0	3/3/0
	HAST	A2	-	3	22	SAM Analysis, Post bHAST, 192 Hours	Completed	-	3/66/0	3/66/0
	HAST	A2	-	3	30	Wire Bond Shear, Post bHast, 192 Hours	Wires	-	3/9/0	3/9/0
	HAST	A2	-	3	30	Bond Pull over Stitch, post bHAST, 192 Hours	Wires	-	3/9/0	3/9/0
	HAST	A2	-	3	30	Bond Pull over Ball, Post bHAST, 192 Hours	Wires	-	3/9/0	3/9/0
	тс	A4	JEDEC JESD22- A104 and Appendix 3	3	77	Temperature Cycle, -65/150C	500 Cycles	3/231/0	3/231/0	3/231/0
	TC	A4	-	3	1	Cross Section, Post T/C 500 Cycles	Completed	-	-	-
	TC	Α4	-	3	22	SAM Analysis, Post T/C, 500 Cycles	Completed	-	-	-

Туре	#	Test Spec	Min Lot Qty	SS/Lot	Test Name / Condition	Duration	Qual Device: UCC21330BQDRQ1	QBS Reference Device: TLV9022QDRQ1	QBS Reference Device: ISO6721BQDRQ1
TC	A4	,	3	30	Wire Bond Shear, Post T/C 500 Cycles	Wires	-	-	-
TC	A4	1	3	30	Bond Pull over Stitch Post T/C 500 Cycles	Wires	-	-	-
TC	A4	,	3	30	Bond Pull over Ball Post T/C 500 Cycles	Wires	-	•	-
тс	A4	JEDEC JESD22- A104 and Appendix 3	3	77	Temperature Cycle, -65/150C	1000 Cycles	3/210/0	3/210/0	3/210/0
TC	A4	,	3	1	Cross Section, Post T/C 1000 Cycles	Completed	3/3/0	3/3/0	3/3/0
TC	A4	,	3	22	SAM Analysis, Post T/C, 1000 Cycles	Completed	3/66/0	3/66/0	3/66/0
TC	A4	,	3	30	Wire Bond Shear, Post T/C 1000 Cycles	Wires	3/9/0	3/9/0	3/9/0
TC	A4	-	3	30	Bond Pull over Stitch, Post T/C, 1000 Cycles	Wires	3/9/0	3/9/0	3/9/0
TC	A4	-	3	30	Bond Pull over Ball, Post T/C, 1000 Cycles	Wires	3/9/0	3/9/0	3/9/0
PTC	A5	JEDEC JESD22- A105	1	45	Power Temperature Cycle -40/125C	1000 Cycles	N/A	N/A	N/A
PTC	A5	JEDEC JESD22- A105	1	45	Power Temperature Cycle -40/125C	2000 Cycles	N/A	N/A	N/A
HTSL	A6	JEDEC JESD22- A103	3	45	High Temp Storage Bake 175C	500 Hours	-	3/231/0	3/135/0
HTSL	A6	,	3	1	Cross Section, Post HTSL 1000 Hours	Completed	-	•	-
HTSL	A6	JEDEC JESD22- A103	3	44	High Temp Storage Bake 150C	2000 Hours	-	3/210/0	3/132/0
HTSL	A6	,	3	1	Cross Section, Post HTSL 2000 Hours	Completed	-	3/3/0	3/3/0
	Tes	st Group C –	Packa	ge Assen	nbly Integrity Tests				
WBS	C1	AEC Q100-001	3	30	Wire Bond Shear, Cpk>1.67	Wires	3/90/0	3/90/0	3/90/0
WBP	C2	MIL- STD883 Method 2011	3	30	Bond Pull over Ball, Cpk >1.67	Wires	3/90/0	3/90/0	3/90/0

⁻ QBS: Qual By Similarity

A1 (PC): Preconditioning:

Performed for THB, Biased HAST, AC, uHAST & TC samples, as applicable.

Ambient Operating Temperature by Automotive Grade Level:

Grade 0 (or E): -40C to +150C Grade 1 (or Q): -40C to +125C Grade 2 (or T): -40C to +105C Grade 3 (or I): -40C to +85C

⁻ Qual Device UCC21330BQDRQ1 is qualified at LEVEL2-260C

E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):

Room/Hot/Cold: HTOL, ED

Room/Hot: THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU

Room : AC/uHAST Green/Pb-free Status:

Qualified Pb-Free(SMT) and Green

ZVEI ID: SEM-PA-08

For questions regarding this notice, e-mails can be sent to the Change Management team or your local Field Sales Representative.

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PCN# 20240605000.2