PRODUCT / PROCESS CHANGE INFORMATION

1. PCI basic data	
1.1 Company	STMicroelectronics International N.V
1.2 PCI No.	MICROCONTROLLERS/24/14682
1.3 Title of PCI	SR5E1x (FT70): Technical Note Update (IO Definition)
1.4 Product Category	see list
1.5 Issue date	2024-05-09

2. PCI Team	
2.1 Contact supplier	
2.1.1 Name	ROBERTSON HEATHER
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2.2 Change responsibility	
2.2.1 Product Manager	Luca RODESCHINI
2.1.2 Marketing Manager	Matteo MOIOLI
2.1.3 Quality Manager	Alberto MERVIC

3. Change		
3.1 Category	3.2 Type of change	3.3 Manufacturing Location
General Product & Design	Modification of datasheet : Errata/error fix	NA

4. Description of change		
	Old	New
4.1 Description	TN Revision 3	TN Revision 4
4.2 Anticipated Impact on form,fit, function, quality, reliability or processability?	No Impact	

5. Reason / motivation for change	
5.1 Motivation	Document Update
5.2 Customer Benefit	SERVICE CONTINUITY

6. Marking of parts / traceability of change	
6.1 Description	Available on www.st.com and included in this notification

7. Timing / schedule	
7.1 Date of qualification results	2024-05-02
7.2 Intended start of delivery	2024-06-14
7.3 Qualification sample available?	Not Applicable

8. Qualification / Validation			
8.1 Description	14682 TN1404_4_0.pdf		
8.2 Qualification report and qualification results	Available (see attachment)	Issue Date	2024-05-09

9. Attachments (additional documentations)
14682 Public product.pdf 14682 TN1404_4_0.pdf

10. Affected parts		
10. 1 Current		10.2 New (if applicable)
10.1.1 Customer Part No	10.1.2 Supplier Part No	10.1.2 Supplier Part No
	SR5E1E770C30F00X	

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SR5E1E3, SR5E1E5, SR5E1E7 IO definition (signal description and input multiplexing tables) and device identification registers

Overview

This technical note provides information on the pinout and device identification registers of the SR5E1E3, SR5E1E5, SR5E1E7 microcontrollers to be used by software and hardware developers.

The table below lists all part numbers available in the device family:

Table 1. Device summary

Product status link	
Part number	**Package**
SR5E1E3	eTQFP100
SR5E1E5	eTQFP144
SR5E1E7	eLQFP176

1 IO definition

The IO definition is contained in a Microsoft® Excel® workbook file attached to this document. Locate the paperclip symbol on the left side of the PDF window, and click it. To open it, double-click on the Excel file.

This file includes the following information:

- Package pinouts
- Pin descriptions
  - Power supply and reference voltage pins
  - System pins
  - Functional pins and associated alternate functions

2 Device identification registers

The identification information about the device is accessible after enabling the clock of the system configuration (SYSCFG) module.

Set the RCC.APB2LENR.SYSCFG bit to one.

2.1 SYSCFG_MIDR1 register description

The device part number and package settings are defined in the SYSCFG_MIDR1 register (refer to the following table).

Note: For more details about this register, refer to the device Reference manual.

Table 2. SYSCFG_MIDR1 field descriptions

Field	Description
31:16 PARTNUM	MCU part number These digits identify the part number of the chip. 0x2511 for: • Production samples of SR5E1x devices
15	0 Reserved
14:10 PKG	Package settings 0x11 eLQFP176 0x09 eTQFP100 0x0D eTQFP144 Other values are reserved.
9:8	00 Reserved
7:4 MAJOR_MASK	Major mask revision *Note: Value is set at factory and varies for each revision of device.*
3:0 MINOR_MASK	Minor mask revision *Note: Value is set at factory and varies for each revision of device.*

2.2 SYSCFG_MIDR2 register description

The manufacturer, NVM memory size and family number settings are defined in the SYSCFG_MIDR2 register (refer to the following table).

Note: For more details about this register, refer to the device Reference manual.

Table 3. SYSCFG_MIDR2 field descriptions

Field	Description
31 SF	Manufacturer 0 Reserved 1 STMicroelectronics
30:23 NVM_SIZE	NVM memory size 0x70 2 Mbytes All other values are reserved.
15:8 FAMILYNUM	ASCII character in MCU part number 0x45 (hexadecimal ASCII value for “E”) for production parts of SR5E1x devices All other values are reserved.

Revision history

Table 4. **Document revision history**

Date	Revision	Changes
11-Mar-2022	1	Initial release based on device pinout Microsoft Excel® files v1.
05-May-2022	2	This release is based on device pinout Microsoft Excel® files v2. Updated Analog Comparator mapping in "IO Signal Table" worksheet in columns "Function" and "Description": • COMP3_INM removed from PAD_PB8 and mapped on PAD_PB13 • COMP5_INM removed from PAD_PB13 and mapped on PAD_PAD_PC4 • COMP7_INM removed from PAD_PC4 and mapped on PAD_PB8 Updated Analog Comparator mapping in "IO Muxing Table" worksheet in column "Direct Analog Function": • COMP3_INM removed from PAD_PB8 and mapped on PAD_PB13 • COMP5_INM removed from PAD_PB13 and mapped on PAD_PAD_PC4 • COMP7_INM removed from PAD_PC4 and mapped on PAD_PB8
26-Sep-2023	3	This release is based on device pinout Microsoft Excel® files v3. Updated "IO Signal Table" worksheet: • Added PA[13] SDADC1_IN0/SAR1_IN16 function description • Row 196: added B-DAC in "Module" column • Row 544, port PC[14]: corrected function description to ADC SAR 3 Analog Channel 6 (was incorrectly labelled ADC SAR 5 Analog Channel 6) • Added slow/fast ADC channel type in "Description" column • Row 566, port PC[15]: corrected function description to ADC SAR 3 Analog Channel 7 (was incorrectly labelled ADC SAR x Analog Channel 7) • Row 569, port PD[0]: corrected function description to ADC SAR 3 Analog Channel 8 (was incorrectly labelled ADC SAR 5 Analog Channel 8) • Row 641, port PD[6]: added missing channel number in Description • Port PB2 to PB15 : changed "Module" and "Description" columns as GPI instead of GPIO Updated Supply / QFP100: renamed pin 87 as VDD_HV_IO_PMU (was VDD_LV). Added new package QFP144 information in various worksheets. QFP1xx and Supply worksheets: added exposed pad ground in the package drawings. Section "Overview": removed text "cut1.0". Section "Device summary": added new RPN "SR5E1E5" for eTQFP144 package. Section "SYSCFG_MIDR1 field descriptions": added new package, 0x0D eTQFP144 to "PKG" field.
27-Mar-2024	4	Updated the confidentiality level of this version of the technical note from "ST restricted" to "Public". Replaced "SR5E1x" with RPNs "SR5E1E3, SR5E1E5, SR5E1E7" in the document. Section 2: Device identification registers: Added text "The identification information..." This release is based on device pinout Microsoft Excel® files v4. Updated "IO Signal Table" worksheet: Row 598, PD2 - TIM1 Break Input: corrected direction to I (Input) in column G Updated "IO Muxing Table" worksheet:

Date	Revision	Changes

		• Changed alternate function description to show the global user function name adding in parenthesis the direction (I, O or I/O) as for GPIO: Example: pad PA[0]
		– before: TIM16_CH1_ti1[0] (I) // TIM16_CH1_oc[1] (O)
		– after: TIM16_CH1 (I/O)
		• Changed SDADC CLKEXT for AF8 into bidirectional and renamed: Example: pad PF[12]
		– before: SDADC1_CLKEXT (I) // RCC_sd_adc1_clk (O)
		– after: RCC SDADC1_CLKEXT (IO)
		Updated all worksheets: Renamed VDD_HV_IOx and VDD_HV_PMU to VDD_HV_IO
		Signal direction convention: I for input; O for output; IO for bidirectional function (example I2C handled in the IP); I/O input or output depending on user configuration (example SPI MISO signal).