PCN Number:	20240424000.1	**PCN Date:**	April 24, 2024
Title:	Datasheet for TPS5410, TPS5420, TPS543x		
Customer Contact:	Change Management team	**Dept:**	Quality Services
Proposed 1st Ship Date:	July 23, 2024		
Change Type:			

☐	Assembly Site	☐	Design	☐	Wafer Bump Material
☐	Assembly Process	☒	Data Sheet	☐	Wafer Bump Process
☐	Assembly Materials	☐	Part number change	☐	Wafer Fab Site
☐	Mechanical Specification	☐	Test Site	☐	Wafer Fab Materials
☐	Packing/Shipping/Labeling	☐	Test Process	☐	Wafer Fab Process

PCN Details

Description of Change:

The product datasheet(s) is being updated as summarized below.
The following change history provides further details.

TEXAS INSTRUMENTS — **TPS5410**
SLVS675E – AUGUST 2006 – REVISED JANUARY 2024

Changes from Revision D (November 2014) to Revision E (January 2024) — **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document 1
- Updated to new format which does not include specific parameter names and does include min and max columns; TJ called out in header Pin names are used rather than signal names; BOOT and PH voltages now marked as output voltage; Footnotes updated and Note 2 removed 3
- Changed BOOT to PH Absolute Maximum to 6 V maximum 3
- Changed CDM ESD to ±750 V 4
- Added Recommended operating V_I input voltage 4
- Updated footnotes to match current TI standards, replaced custom board specifications with EVM information and JEDEC standard information 4
- Changed $R_{\theta JC(top)}$, $R_{\theta JB}$, Ψ_{JT}, Ψ_{JB} 4
- Added condition for typical specifications EC table's header, added parameter names, and used pin names in parameter descriptions. Footnote added 4
- Updated the following test conditions: V_{FB}, D_{MAX}, and $R_{DSON(HS)}$ 4
- Updated the following typical specifications in the EC table: $I_{Q(VIN)}$, $I_{SD(VIN)}$, $VIN_{UVLO(H)}$, $V_{EN(H)}$, and $R_{DSON(HS)}$ 4
- Updated typical and maximum ISH(OC) in the EC table 4

TEXAS INSTRUMENTS — **TPS5420**
SLVS642F – APRIL 2006 – REVISED JANUARY 2024

Changes from Revision E (September 2013) to Revision F (January 2024) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document..... 1
- Updated to new format which does not include specific parameter names and does include min and max columns. TJ called out in header. Pin names are used rather than signal names. BOOT and PH voltages now marked as output voltage. Footnotes updated and Note 2 removed..... 5
- Changed BOOT to PH Absolute Maximum to 6 V maximum..... 5
- Deleted Absolute Maximum BOOT to GND maximum voltage..... 5
- Added ESD table..... 5
- Added Recommended operating V_I input voltage..... 5
- Updated footnotes to match current TI standards, replaced custom board specifications with EVM information and JEDEC standard information..... 5
- Changed $R_{\theta JC(top)}$, $R_{\theta JB}$, ψ_{JT}, ψ_{JB} 5
- Added condition for typical specifications EC table's header, added parameter names, and used pin names in parameter descriptions. Footnote added..... 6
- Updated the following test conditions: V_{FB}, D_{MAX}, and $R_{DSON(HS)}$..... 6
- Updated the following typical specifications in the EC table: $I_{Q(VIN)}$, $I_{SD(VIN)}$, $VIN_{UVLO(H)}$, $V_{EN(H)}$, and $R_{DSON(HS)}$..... 6

Changes from Revision J (July 2022) to Revision K (January 2024) **Page**

- Updated WEBENCH® links throughout the data sheet. Added "integrated circuit" when the PowerPAD™ package is mentioned. Changed MOSFET resistance 110mΩ to100mΩ. Changed I_Q from 18µA to 15µA..... 1
- Changed Pin Configuration figure title to "DDA Package 8-Pin SOIC with Thermal Pad Top View" and repositioned the title to the correct position. Changed "PowerPAD" to "DAP". 3
- Updated Absolute Maximum Ratings table to new format which does not include specific parameter names and does include min and max columns. T_J called out in header. Pin names are used rather than signal names. BOOT and PH voltages now marked as output voltage. Updated footnotes and removed Note 2..... 4
- Changed BOOT to PH Absolute Maximum from 10 V to 6 V..... 4
- Changed PH to GND Absolute Maximum (transient < 10 ns) from -4 V to -1.2 V..... 4
- Changed CDM ESD from ±1500 V to ±750 V..... 4
- Changed recommended operating "V_I" to "input voltage"..... 4
- Updated thermal information footnotes to match current TI standards which include JEDEC standard information. Changed custom board information to EVM $R_{\theta JA}$ information..... 4
- Changed $R_{\theta JC(top)}$ from 46.4 to 46, $R_{\theta JB}$ from 20.8 to 15, ψ_{JT} from 4.9 to 5.2, ψ_{JB} from 20.7 to 15.3, and $R_{\theta JC(bot)}$ from 0.8 to 6..... 4
- Added condition for typical specifications EC table's header, added parameter names, and used pin names in parameter descriptions. Footnote added..... 5
- Changed test condition for V_{FB} from "I_O = 0 A to 3 A" to "T_J = –40°C to 125°C", Changed $r_{DS(ON)}$ to $R_{DSON(HS)}$ and test condition to for $R_{DSON(HS)}$ from "VIN = 5.5 V" to "V_{IN} = 5.5 V, $V_{BOOT-SW}$ = 4.0 V"..... 5
- Changed the name of I_Q to $I_{SD(VIN)}$ if ENA is low and $I_{Q(VIN)}$ if the chip is active..... 5
- Added test condition for D_{MAX}, "f_{SW} = 500 kHz" and for second $R_{DSON(HS)}$ spec "V_{IN} = 12 V, $V_{BOOT-SW}$ = 4.5 V"..... 5
- Changed $I_{Q(VIN)}$ typical from 3 mA to 2 mA, $I_{SD(VIN)}$ typical from 18 µA to 15 µA, $VIN_{UVLO(H)}$ from 330 mV to 0.35 V, and $V_{EN(H)}$ from 450 mV to 325 mV..... 5
- Changed $R_{DS(ON)}$ with VIN = 5 V typical from 150 mΩ to 125 mΩ and with VIN = 12 V from 110 mΩ to 100 mΩ..... 5
- Changed "110-mΩ high-side MOSFET" to "100-mΩ high-side MOSFET" and 18 µA to 15 µA in *Overview* 8
- Changed shutdown current from 18 µA to 15 µA in *Enable (ENA) and Internal Slow Start* section..... 9
- Changed UVLO hysteresis from 330 mV to 350 mV in UVLO description..... 9
- Changed "PwPd" to "DAP" on the TPS5430DDA package drawing in Figure 7-1 and "exposed PowerPAD™" to DAP in circuit description 13
- Changed "PwPd" to "DAP" on the TPS5430DDA package drawing in Figure 7-9..... 21
- Changed "PwPd" to "DAP" on the TPS5431DDA package drawing in Figure 7-10..... 22
- Changed "PwPd" to "DAP" on the TPS5430DDA package drawing in Figure 7-11..... 23
- Changed "PowerPAD" to "DAP" in *Layout Guidelines* 25

The datasheet number will be changing.

Device Family	Change From:	Change To:
TPS5410	SLVS675D	**SLVS675E**
TPS5420	SLVS642E	**SLVS642F**
TPS543x	SLVS632J	**SLVS632K**

These changes may be reviewed at the datasheet links provided.
http://www.ti.com/product/TPS5410
http://www.ti.com/product/TPS5420
http://www.ti.com/product/TPS5430

Reason for Change:

To more accurately reflect device characteristics.

Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):

Electrical specification performance changes as indicated above.

Changes to product identification resulting from this PCN:

None.

Product Affected:

TPS5410DRG4	TPS5410D	TPS5410DG4	TPS5410DR
TPS5420DR	TPS5420DRG4	TPS5420D	TPS5420DG4
TPS5430DDAG4	TPS5430DDAR	TPS5430DDARG4	TPS5430DDA
TPS5431DDAG4	TPS5431DDAR	TPS5431DDARG4	TPS5431DDA

For questions regarding this notice, e-mails can be sent to the Change Management team or your local Field Sales Representative.

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