PCN Number: 202			240320001.2A						CN		April 16, 2024			
Titl	e:	Qualific	ation	of T	I CDAT	as	an addi	tional A	ssembly 8	ķΤ	est	site f	or select devices	
Customer					anagement team <b>Dept:</b>			(	Quality Services					
Proposed 1 <sup>st</sup> Ship Octob Date: 2024				Octob 2024	er 1	3,	Sample requests accepted until:					May 16, 2024*		
*Sa	mple	request	s rec	eived	after	May	16, 20	24 will r	not be sup	эрс	orte	ed.		
Cha	ange	Type:												
$\square$	Assembly Site						Design					Wafer Bump Material		
Assembly Process						Data Sheet					Wafer Bump Process			
Assembly Materials						Part number change					Wafer Fab Site			
Mechanical Specification						Test Site					Wafer Fab Material			
	Pack	king/Ship	ping	/Lab	eling		Test Process			Wafer Fab Process				
	DCN Detaile													

# **PCN Details**

### **Description of Change:**

**Revision A** is to announce the <u>addition</u> of lead finish & Pin 1 ID marking change that was not included on the original PCN notification.

Texas Instruments is pleased to announce the qualification of TI CDAT as an additional Assembly & test site for the devices listed below.

#### Construction differences are as follows:

	UTAC	TI CDAT
Wire diam/type	1.0mil Au	0.96mil Cu
Mount compound	PZ0068	4229877
Mold compound	CZ0096	4222198
Lead finish	<mark>NiPdAu</mark>	Matte Sn
Pin 1 ID marking	<mark>Stripe</mark>	Dot

Upon expiry of this PCN, there will be a transition period where TI will combine lead free solutions in a single <u>standard part number</u>. For example; <u>LM74700QDBVRQ1</u> – can ship with both Matte Sn and NiPdAu.

#### Example:

- Customer order for 7500 units of LM74700QDBVRQ1 with 2500 units SPQ (Standard Pack Quantity per Reel).
- TI can satisfy the above order in one of the following ways.
  - 3 Reels of NiPdAu finish.
  - II. 3 Reels of Matte Sn finish
  - III. 2 Reels of Matte Sn and 1 reel of NiPdAu finish.
  - IV. 2 Reels of NiPdAu and 1 reel of Matte Sn finish.

Qual details are provided in the Qual Data Section.

#### **Reason for Change:**

Continuity of Supply

- 1) To align with world technology trends and use wiring with enhanced mechanical and electrical properties
- 2) Maximize flexibility within our Assembly/Test production sites.
- 3) Cu is easier to obtain and stock

Anticipated impact on Form, Fit, Function, Quality or Reliability (positive / negative):

None

# **Impact on Environmental Ratings**

Checked boxes indicate the status of environmental ratings following implementation of this change. If below boxes are checked, there are no changes to the associated environmental ratings.

RoHS	REACH	Green Status	IEC 62474
No Change	No Change	No Change	No Change

#### Changes to product identification resulting from this PCN:

Assembly Site

UTAC	Assembly Site Origin (22L)	ASO: NSE
TI CDAT	Assembly Site Origin (22L)	ASO: CDA

Sample product shipping label (not actual product label)





(1P) \$N74L\$07N\$R (Q) 2000 (D) 0336 (31T)LOT: 3959047MLA (4W) TKY(1T) 7523483\$I2 (P) (2P) REV: (V) 0033317 (20L) C\$0: SHE (21L) CCO: USA (22L) A\$0: MLA (23L) ACO: MY\$

# LBL: 5A (L)TO

LM74700QDBVRQ1 LM74700QDBVTQ1

# **Qualification Report**

Automotive Qualification Summary (As per AEC-Q100 Rev. H and JEDEC Guidelines) Approve Date 05-March-2024

#### **Product Attributes**

1 Todati Attibutes								
Attributes	Qual Device:	QBS Process, Product Reference:						
Attibutes	LM74700QDBVRQ1	<u>LM74700QDBVRQ1</u>						
Automotive Grade Level	Grade 1	Grade 1						
Operating Temp Range (C)	-40 to 125	-40 to 125						
Product Function	Power Management	Power Management						
Wafer Fab Supplier	RFAB	RFAB						
Assembly Site	CDAT	UTL2						
Package Group	SOT	SOT						
Package Designator	DBV	DBV						
Pin Count	6	6						

QBS: Qual By Similarity

Qual Device LM74700QDBVRQ1 is qualified at MSL2 260C

# **Qualification Results**

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Spec	Min Lot	SSI	Test Name	Condition	Duration	Qual Device:	QBS Process, Product Reference:
			Qty	Lot	iest Hame	Condition		LM74700QDBVRQ1	LM74700QDBVRQ1
Test Group	A - Acc	elerated Environment Str	ess Test	s			100		
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	MSL2 260C	-	0 Fails	0 Fails
HAST	A2	JEDEC JESD22-A110	3	77	Biased HAST	130C/85%RH	96 Hours	3/231/0	3/231/0
AC/UHAST	A3	JEDEC JESD22- A102/JEDEC JESD22- A118	3	77	Autoclave	121C/15psig	96 Hours	• /	3/231/0
AC/UHAST	АЗ	JEDEC JESD22- A102/JEDEC JESD22- A118	3	77	Unbiased HAST	130C/85%RH	96 Hours	3/231/0	-
тс	A4	JEDEC JESD22-A104 and Appendix 3	3	77	Temperature Cycle	-65C/150C	500 Cycles	3/231/0	3/231/0
TC-BP	A4	MIL-STD883 Method 2011	1	5	Post Temp Cycle Bond Pull	-	-	1/5/0	1/5/0
HTSL	A6	JEDEC JESD22-A103	1	45	High Temperature Storage Life	150C	1000 Hours	3/135/0	-
HTSL	A6	JEDEC JESD22-A103	1	45	High Temperature Storage Life	175C	500 Hours	-	1/45/0
Test Group	B - Acc	elerated Lifetime Simulati	on Tests					:o:	
HTOL	B1	JEDEC JESD22-A108	3	77	Life Test	150C	300 Hours	1/77/0	3/231/0
ELFR	B2	AEC Q100-008	3	800	Early Life Failure Rate	150C	24 Hours	-	3/2400/0
Test Group	C - Pac	kage Assembly Integrity 1	ests	10				·	
WBS	C1	AEC Q100-001	1	30	Wire Bond Shear	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	3/90/0	3/90/0

WBP	C2	MIL-STD883 Method 2011	1	30	Wire Bond Pull	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	3/90/0	3/90/0
SD	СЗ	JEDEC J-STD-002	1	15	PB Solderability	>95% Lead Coverage	-	1/15/0	1/15/0
SD	СЗ	JEDEC J-STD-002	1	15	PB-Free Solderability	>95% Lead Coverage	-	1/15/0	1/15/0
PD	C4	JEDEC JESD22-B100 and B108	3	10	Physical Dimensions	Cpk>1.67	-	3/30/0	3/30/0
Test Grou	p D - Die	Fabrication Reliability Tes	ts						
ЕМ	D1	JESD61	-	-	Electromigration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
TDDB	D2	JESD35	-	-	Time Dependent Dielectric Breakdown	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
HCI	D3	JESD60 & 28	-	-	Hot Carrier Injection	-	2	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
ВТІ	D4	-		-	Bias Temperature Instability	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
SM	D5	-	-	-	Stress Migration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
Test Grou	p E - Elec	trical Verification Tests	100		20	edi.			
ESD	E2	AEC Q100-002	1	3	ESD HBM		2000 Volts	•	1/3/0
ESD	E3	AEC Q100-011	1	3	ESD CDM	-	500 Volts		1/3/0
LU	E4	AEC Q100-004	1	6	Latch-Up	Per AEC Q100-004	-	•	1/6/0
ED	E5	AEC Q100-009	3	30	Electrical Distributions	Cpk>1.67 Room, hot, and cold	-	1/30/0	3/90/0

Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable

The following are equivalent HTOL options based on an activation energy of 0.7eV: 125C/1k

Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours

The following are equivalent HTSL options based on an activation energy of 0.7 eV: 150 C/1 k Hours, and 170 C/420 Hours

The following are equivalent Temp Cycle options per JESD47: -55C/125C/700 Cycles and -65C/150C/500 Cycles

#### **Ambient Operating Temperature by Automotive Grade Level:**

Grade 0 (or E): -40C to +150C Grade 1 (or Q): -40C to +125C Grade 2 (or T): -40C to +105C Grade 3 (or I): -40C to +85C

# E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):

Room/Hot/Cold: HTOL, ED

Room/Hot: THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU

Room: AC/uHAST

Quality and Environmental data is available at TI's external Web site: http://www.ti.com/

# **Qualification Report**

Automotive Qualification Summary (As per AEC-Q006 and JEDEC Guidelines) Approve Date 05-March-2024

#### **Product Attributes**

Attributes	Qual Device:
Attributes	<u>LM74700QDBVRQ1</u>
Automotive Grade Level	Grade 1
Operating Temp Range (C)	-40 to 125
Product Function	Power Management
Wafer Fab Supplier	RFAB
Assembly Site	CDAT
Package Group	SOT
Package Designator	DBV
Pin Count	6

QBS: Qual By Similarity

Qual Device LM74700QDBVRQ1 is qualified at MSL2 260C

# **Qualification Results**

Data Displayed as: Number of lots / Total sample size / Total failed

Туре	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: LM74700QDBVRQ1
Test Gr	oup A - A	Accelerated Environment Stres	ss Tests					
PC	A1	JEDEC J-STD-020 JESD22- A113	3	77	Preconditioning	MSL2 260C	-	3/639/0
PC	A1.1	2	3	22	SAM Precon Pre	on Pre Review for delamination		3/66/0
PC	A1.2	-	- 3 22 SAM Precon Post Review for delamination		-	3/66/0		
HAST	A2.1	JEDEC JESD22-A110	3	77	Biased HAST	130C/85%RH	96 Hours	3/231/0
HAST	A2.1.2	-	3	1	Cross Section, post bHAST, 1X	Post stress cross section	Completed	3/3/0
HAST	A2.1.3	-	3	3	Wire Bond Shear, post bHAST, 1X	Post stress	-	3/9/0
HAST	A2.1.4		3	3	Bond Pull over Stitch, post bHAST, 1X	Post stress	-	3/9/0
HAST	A2.1.5	-	3	3	Bond Pull over Ball, post bHAST, 1X	Post stress	-	3/9/0
HAST	A2.2	JEDEC JESD22-A110	3	70	Biased HAST	130C/85%RH	192 Hours	3/231/0
HAST	A2.2.1	-	3	22	SAM Analysis, post bHAST 2X	Review for delamination	Completed	3/66/0
HAST	A2.2.2		3	1	Cross Section, post bHAST, 2X	Post stress cross section	Completed	3/3/0
HAST	A2.2.3	-	3	3	Wire Bond Shear, post bHAST, 2X	Post stress	-	3/9/0
HAST	A2.2.4	-	3	3	Bond Pull over Stitch, post bHAST, 2X	Post stress	-	3/9/0
HAST	A2.2.5	-	3	3	Bond Pull over Ball, post bHAST, 2X	Post stress	-	3/9/0
тс	A4.1	JEDEC JESD22-A104 and Appendix 3	3	77	Temperature Cycle	-65C/150C	500 Cycles	3/231/0
TC	A4.1.1	-	3	22	SAM Analysis, post TC 1X	Review for delamination	Completed	3/66/0
TC	A4.1.2	-	3	1	Cross Section, post TC, 1X	Post stress cross section	Completed	3/3/0
тс	A4.1.3	-	3	3	Wire Bond Shear, post TC, 1X	Post stress	-	3/9/0
тс	A4.1.4		3	3	Bond Pull over Stitch, post TC, 1X	Post stress	<u>-</u>	3/9/0
TC	A4.1.5	-	3	3	Bond Pull over Ball, post TC, 1X	Post stress	-	3/9/0
TC	A4.2	JEDEC JESD22-A104 and Appendix 3	3	70	Temperature Cycle	-65C/150C	1000 Cycles	3/231/0
тс	A4.2.1	-	3	22	SAM Analysis, post TC, 2X	Review for delamination	Completed	3/66/0
тс	A4.2.2	-	3	1	Cross Section, post TC, 2X	Post stress cross section	Completed	3/3/0
тс	A4.2.3	-	3	3	Wire Bond Shear, post TC, 2X	Post stress	-	3/9/0
TC	A4.2.4	-	3	3	Bond Pull over Stitch, post TC, 2X	Post stress	-	3/9/0
тс	A4.2.5	-	3	3	Bond Pull over Ball, post TC, 2X	Post stress	-	3/9/0
HTSL	A6.1	JEDEC JESD22-A103	3	45	High Temperature Storage Life	150C	1000 Hours	3/135/0
HTSL	A6.1.1		3	1	Cross Section, post HTSL, 1X	Post stress cross section	Completed	3/3/0
HTSL	A6.2	JEDEC JESD22-A103	3	44	High Temperature Storage Life	150C	2000 Hours	3/135/0
HTSL	A6.2.1	-	3	1	Cross Section, post HTSL, 2X	Post stress cross section	Completed	3/3/0
Test Gr	roup C - F	Package Assembly Integrity Te	sts					
WBS	C1	AEC Q100-001	1	30	Wire Bond Shear	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	3/90/0
WBP	C2	MIL-STD883 Method 2011	1	30	Wire Bond Pull	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	3/90/0

Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable

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The following are equivalent Temp Cycle options per JESD47: -55C/125C/700 Cycles and -65C/150C/500 Cycles Ambient Operating Temperature by Automotive Grade Level:

Grade 0 (or E): -40C to +150C Grade 1 (or Q): -40C to +125C Grade 2 (or T): -40C to +105C Grade 3 (or I): -40C to +85C

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Room/Hot: THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU

Room: AC/uHAST

Quality and Environmental data is available at TI's external Web site: http://www.ti.com/

ZVEI ID reference: SEM-PA-11, SEM-PA-07, SEM-PA-08, SEM-PA-18, SEM-PA-13, SEM-PA-05, SEM-TF-01

For questions regarding this notice, e-mails can be sent to Change Management team or your local Field Sales Representative.

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