



PCN Number:	20240313001.2		PCN Date:	March 14, 2024	
Title:	Qualification of RFAB using qualified Process Technology, Die Revision, CDAT as wafer probe site and additional Assembly site/BOM options for select devices				
Customer Contact:	Change Management team		Dept:	Quality Services	
Proposed 1st Ship Date:	September 10, 2024		Sample requests accepted until:	April 13, 2024*	
*Sample requests received after April 13, 2024 will not be supported.					
Change Type:					
<input checked="" type="checkbox"/>	Assembly Site	<input checked="" type="checkbox"/>	Design	<input type="checkbox"/>	Wafer Bump Material
<input checked="" type="checkbox"/>	Assembly Process	<input type="checkbox"/>	Data Sheet	<input type="checkbox"/>	Wafer Bump Process
<input checked="" type="checkbox"/>	Assembly Materials	<input type="checkbox"/>	Part number change	<input checked="" type="checkbox"/>	Wafer Fab Site
<input type="checkbox"/>	Mechanical Specification	<input checked="" type="checkbox"/>	Test Site	<input checked="" type="checkbox"/>	Wafer Fab Material
<input checked="" type="checkbox"/>	Packing/Shipping/Labeling	<input type="checkbox"/>	Test Process	<input type="checkbox"/>	Wafer Fab Process
PCN Details					
Description of Change:					
Texas Instruments is pleased to announce the qualification of its RFAB fabrication facility as an additional Wafer Fab option in addition to an Assembly site/BOM option for the devices listed below.					
Current Fab Site			Additional Fab Site		
Current Fab Site	Process	Wafer Diameter	Additional Fab Site	Process	Wafer Diameter
MIHO8	LBC8LVISO	200 mm	RFAB	LBC8LVISO	300 mm
The die was also changed as a result of the process change.					
	Current	Proposed			
Probe site (EWS)	No Probe	CDAT (CD-PR)			
Construction differences are as follows:					
Group 1 Device:					
	TI Taiwan	TI Malaysia			
Wire diam/type	0.96mil Au, 1.0mil Cu	0.80mil Cu			
Test coverage, insertions, conditions will remain consistent with current testing					
Group 2 Device:					
	Current	Proposed			
Bond wire type, diam	0.96mil Au	0.8mil Cu			
Package Marking	 (with Q)	 (Without Q)			
Qual details are provided in the Qual Data Section.					
Reason for Change:					
Continuity of Supply					
1) To align with world technology trends and use wiring with enhanced mechanical and electrical properties					
2) Maximize flexibility within our Assembly/Test production sites.					

3) Cu is easier to obtain and stock			
Anticipated impact on Form, Fit, Function, Quality or Reliability (positive / negative):			
None			
Impact on Environmental Ratings			
Checked boxes indicate the status of environmental ratings following implementation of this change. If below boxes are checked, there are no changes to the associated environmental ratings.			
RoHS	REACH	Green Status	IEC 62474
<input checked="" type="checkbox"/> No Change	<input checked="" type="checkbox"/> No Change	<input checked="" type="checkbox"/> No Change	<input checked="" type="checkbox"/> No Change
Changes to product identification resulting from this PCN:			
Fab Site Information:			
Chip Site	Chip Site Origin Code (20L)	Chip Site Country Code (21L)	Chip Site City
MIHO8	MH8	JPN	Ibaraki
RFAB	RFB	USA	Richardson
Die Rev:			
Current	New		
Die Rev [2P]	Die Rev [2P]		
A	A		
Assembly Site Information:			
Assembly Site	Assembly Site Origin (22L)	Assembly Country Code (23L)	Assembly City
TI Taiwan	TAI	TWN	Chung Ho, New Taipei City
TI Malaysia	MLA	MYS	Kuala Lumpur
Sample product shipping label (not actual product label):			
Group 1 Product Affected: Wafer Fab, Probe site, A/T			
ISO6720FQDWVRQ1	ISO6720QDWVRQ1	ISO6721FQDWVRQ1	ISO6721QDWVRQ1
Group 2 Product Affected: Wafer FAB, Probe site, BOM			
ISO7710FQDRQ1	ISO7710QDRQ1	ISO7720FQDWRQ1	ISO7721FQDWRQ1
ISO7710FQDWRQ1	ISO7710QDWRQ1	ISO7720QDWRQ1	ISO7721QDWRQ1

Group 1 Qualification Report

Automotive Qualification Summary
(As per AEC-Q100 Rev. H and JEDEC Guidelines)
Approve Date 21-February-2024

Product Attributes

Attributes	Qual Device: <u>ISO6721QDWVRQ1</u>	QBS Process Reference: <u>UCC23513QDWYQ1</u>	QBS Package Reference: <u>ISO6763QDWVRQ1</u>	QBS Package Reference: <u>AMC1311CQDWVRQ1</u>
Automotive Grade Level	Grade 1	Grade 1	Grade 1	Grade 1
Operating Temp Range (C)	-40 to 125	-40 to 125	-40 to 125	-40 to 125
Product Function	Interface	Power Management	Interface	Signal Chain
Wafer Fab Supplier	RFAB, RFAB	RFAB, RFAB	RFAB, RFAB	AIZU, AIZU, MH8, MH8
Assembly Site	MLA	TAI	MLA	MLA
Package Group	SOIC	SOIC	SOIC	SOIC
Package Designator	DWV	DWY	DW	DWV
Pin Count	8	6	16	8

QBS: Qual By Similarity

Qual Device ISO6721QDWVRQ1 is qualified at MSL2 260C

Qual Device ISO6721FQDWVRQ1 is qualified at MSL2 260C

Qual Device ISO6720QDWVRQ1 is qualified at MSL2 260C

Qual Device ISO6720FQDWVRQ1 is qualified at MSL2 260C

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: <u>ISO6721QDWVRQ1</u>	QBS Process Reference: <u>UCC23513QDWYQ1</u>	QBS Package Reference: <u>ISO6763QDWVRQ1</u>	QBS Package Reference: <u>AMC1311CQDWVRQ1</u>
Test Group A - Accelerated Environment Stress Tests											
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	MSL2 260C	-	1/154/0	-	3/828/0	-
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	MSL3 260C	-	-	-	-	3/828/0
HAST	A2	JEDEC JESD22-A110	3	77	Biased HAST	130C/85%RH	96 Hours	-	-	3/231/0	3/231/0
AC/UHAST	A3	JEDEC JESD22-A102/JEDEC JESD22-A118	3	77	Autoclave	121C/15psig	96 Hours	1/77/0	-	3/231/0	-
AC/UHAST	A3	JEDEC JESD22-A102/JEDEC JESD22-A118	3	77	Unbiased HAST	130C/85%RH	96 Hours	-	-	-	3/231/0
TC	A4	JEDEC JESD22-A104 and Appendix 3	3	77	Temperature Cycle	-65C/150C	500 Cycles	1/77/0	-	3/231/0	3/231/0
TC-BP	A4	MIL-STD883 Method 2011	1	5	Post Temp Cycle Bond Pull	-	-	1/5/0	-	1/5/0	1/5/0
HTSL	A6	JEDEC JESD22-A103	1	45	High Temperature Storage Life	150C	1000 Hours	-	-	3/135/0	-
HTSL	A6	JEDEC JESD22-A103	1	45	High Temperature Storage Life	175C	500 Hours	-	-	-	3/135/0
Test Group B - Accelerated Lifetime Simulation Tests											

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: ISO6721QDWVRQ1	QBS Process Reference: UCC23513QDWYQ1	QBS Package Reference: ISO6763QDWRQ1	QBS Package Reference: AMC1311CQDWVRQ1
HTOL	B1	JEDEC JESD22-A108	3	77	Life Test	125C	1000 Hours	-	3/231/0	-	-
ELFR	B2	AEC Q100-008	3	800	Early Life Failure Rate	125C	48 Hours	-	3/2400/0	-	-
Test Group C - Package Assembly Integrity Tests											
WBS	C1	AEC Q100-001	1	30	Wire Bond Shear	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	1/30/0	-	3/90/0	3/90/0
WBP	C2	MIL-STD883 Method 2011	1	30	Wire Bond Pull	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	1/30/0	-	3/90/0	3/90/0
SD	C3	JEDEC J-STD-002	1	15	PB Solderability	>95% Lead Coverage	-	-	-	-	1/15/0
SD	C3	JEDEC J-STD-002	1	15	PB-Free Solderability	>95% Lead Coverage	-	-	-	-	1/15/0
PD	C4	JEDEC JESD22-B100 and B108	3	10	Physical Dimensions	Cpk>1.67	-	-	-	-	3/30/0
Test Group D - Die Fabrication Reliability Tests											
EM	D1	JESD61	-	-	Electromigration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
Tddb	D2	JESD35	-	-	Time Dependent Dielectric Breakdown	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
HCI	D3	JESD60 & 28	-	-	Hot Carrier Injection	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
BTI	D4	-	-	-	Bias Temperature Instability	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
SM	D5	-	-	-	Stress Migration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
Test Group E - Electrical Verification Tests											
ESD	E2	AEC Q100-002	1	3	ESD HBM	-	2000 Volts	1/3/0	1/3/0	-	1/3/0
ESD	E3	AEC Q100-011	1	3	ESD CDM	-	750 Volts	1/3/0	1/3/0	-	1/3/0
LU	E4	AEC Q100-004	1	6	Latch-Up	Per AEC Q100-004	-	1/6/0	1/6/0	-	1/6/0
ED	E5	AEC Q100-009	3	30	Electrical Distributions	Cpk>1.67 Room, hot, and cold	-	1/30/0	3/90/0	3/90/0	1/30/0

Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable

The following are equivalent HTOL options based on an activation energy of 0.7eV : 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours

The following are equivalent HTSL options based on an activation energy of 0.7eV : 150C/1k Hours, and 170C/420 Hours

The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles

Ambient Operating Temperature by Automotive Grade Level:

Grade 0 (or E): -40C to +150C

Grade 1 (or Q): -40C to +125C

Grade 2 (or T): -40C to +105C

Grade 3 (or I) : -40C to +85C

E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):

Room/Hot/Cold : HTOL, ED

Room/Hot : THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU

Room : AC/uHAST

Quality and Environmental data is available at TI's external Web site: <http://www.ti.com/>

Group 2 Qualification Report
Automotive Qualification Summary
(As per AEC-Q100 Rev. J and JEDEC Guidelines)
Approve Date 01-March-2024

Product Attributes

Attributes	Qual Device: ISO7710QDRQ1	QBS Package Reference: ISO6721BQDRQ1	QBS Process Reference: UCC23513QDWYQ1	QBS Package Reference: ISO6763QDWRQ1	QBS Package Reference: ISO5452DWR	QBS Package Reference: ISO7721QDRQ1	QBS Package Reference: UCC21330BQDRQ1
Automotive Grade Level	Grade 1	Grade 1	Grade 1	Grade 1	Grade 1	Grade 1	Grade 1
Operating Temp Range (C)	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125
Product Function	Interface	Interface	Power Management	Interface	Power Management	Signal Chain,Interface	Power Management
Wafer Fab Supplier	RFAB, RFAB	MH8, MH8	RFAB, RFAB	RFAB, RFAB	DP1DM5, DP1DM5, MH8	RFAB, RFAB	RFAB, RFAB, RFAB
Assembly Site	MLA	MLA	TAI	MLA	MLA	MLA	MLA
Package Group	SOIC	SOIC	SOIC	SOIC	SOIC	SOIC	SOIC
Package Designator	D	D	DWY	DW	DW	D	D
Pin Count	8	8	6	16	16	8	16

QBS: Qual By Similarity

Qual Device ISO7710QDRQ1 is qualified at MSL2 260C

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: ISO7710QDRQ1	QBS Package Reference: ISO6721BQDRQ1	QBS Process Reference: UCC23513QDWYQ1	QBS Package Reference: ISO6763QDWRQ1	QBS Package Reference: ISO5452DWR	QBS Package Reference: ISO7721QDRQ1	QBS Package Reference: UCC21330BQDRQ1
Test Group A - Accelerated Environment Stress Tests														
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	MSL1 260C	-	-	No Fails	-	-	-	-	-
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	MSL2 260C	-	-	-	-	No Fails	No Fails	No Fails	No Fails
HAST	A2	JEDEC JESD22-A110	3	77	Biased HAST	130C/85%RH	96 Hours	-	3/231/0	-	3/231/0	1/77/0	-	-
AC/HAST	A3	JEDEC JESD22-A102/JEDEC JESD22-A118	3	77	Autoclave	121C/15psig	96 Hours	-	3/231/0	-	3/231/0	1/77/0	-	-
TC	A4	JEDEC JESD22-A104 and Appendix 3	3	77	Temperature Cycle	-65C/150C	500 Cycles	-	3/231/0	-	3/231/0	1/77/0	1/77/0	3/231/0
TC-SAM	A4	-	3	3	Post TC SAM	<50% delamination	-	-	1/12/0	-	1/12/0	-	1/12/0	1/12/0
HTSL	A6	JEDEC JESD22-A103	1	45	High Temperature Storage Life	150C	1000 Hours	-	-	-	3/135/0	1/45/0	-	-
HTSL	A6	JEDEC JESD22-A103	1	45	High Temperature Storage Life	175C	500 Hours	-	3/135/0	-	-	-	-	-
Test Group B - Accelerated Lifetime Simulation Tests														
HTOL	B1	JEDEC JESD22-A108	3	77	Life Test	125C	1000 Hours	-	3/231/0	3/231/0	-	-	-	-
ELFR	B2	AEC Q100-006	3	800	Early Life Failure Rate	125C	48 Hours	-	-	3/2400/0	-	-	-	-
Test Group C - Package Assembly Integrity Tests														
WBS	C1	AEC Q100-001	1	30	Wire Bond Shear	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	-	3/228/0	-	3/90/0	-	1/30/0	3/90/0
WBP	C2	MIL-STD883 Method 2011	1	30	Wire Bond Pull	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	-	3/228/0	-	3/90/0	-	1/30/0	3/90/0
SD	C3	JEDEC J-STD-002	1	15	PB Solderability	>95% Lead Coverage	-	-	1/15/0	-	-	-	-	-
SD	C3	JEDEC J-STD-002	1	15	PB-Free Solderability	>95% Lead Coverage	-	-	1/15/0	-	-	-	-	-
PD	C4	JEDEC JESD22-B100 and B108	3	10	Physical Dimensions	Cpk>1.67	-	-	3/30/0	-	-	-	1/10/0	3/30/0
Test Group D - Die Fabrication Reliability Tests														

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: ISO7710QDWRQ1	QBS Package Reference: ISO6721BQDWRQ1	QBS Process Reference: UCC23513QDWRQ1	QBS Package Reference: ISO6763QDWRQ1	QBS Package Reference: ISO6452DWR	QBS Package Reference: ISO7721QDWRQ1	QBS Package Reference: UCC21330BQDWRQ1
EM	D1	JESD61	-	-	Electromigration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
TDD8	D2	JESD35	-	-	Time Dependent Dielectric Breakdown	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
HCI	D3	JESD60 & 28	-	-	Hot Carrier Injection	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
BTI	D4	-	-	-	Bias Temperature Instability	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
SM	D5	-	-	-	Stress Migration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
Test Group E - Electrical Verification Tests														
ESD	E2	AEC Q100-002	1	3	ESD HBM	-	2000 Volts	1/3/0	1/3/0	1/3/0	-	-	1/3/0	1/3/0
ESD	E3	AEC Q100-011	1	3	ESD CDM	-	500 Volts	1/3/0	1/3/0	1/3/0	-	-	1/3/0	1/3/0
LU	E4	AEC Q100-004	1	6	Latch-Up	Per AEC Q100-004	-	1/6/0	1/6/0	1/6/0	-	-	1/6/0	1/6/0
ED	E5	AEC Q100-009	3	30	Electrical Distributions	Cpk>1.67 Room, hot, and cold	-	1/30/0	3/90/0	3/90/0	3/90/0	1/30/0	1/30/0	1/30/0

Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable

The following are equivalent HTOL options based on an activation energy of 0.7eV : 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours

The following are equivalent HTSL options based on an activation energy of 0.7eV : 150C/1k Hours, and 170C/420 Hours

The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles

Ambient Operating Temperature by Automotive Grade Level:

Grade 0 (or E): -40C to +150C

Grade 1 (or Q): -40C to +125C

Grade 2 (or T): -40C to +105C

Grade 3 (or I) : -40C to +85C

E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):

Room/Hot/Cold : HTOL, ED

Room/Hot : THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU

Room : AC/uHAST

Quality and Environmental data is available at TI's external Web site: <http://www.ti.com/>

Qualification Report

Automotive Qualification Summary

(As per AEC-Q100 Rev. J and JEDEC Guidelines)

Approve Date 01-MARCH -2024

Product Attributes

Attributes	Qual Device: ISO7710QDWRQ1	QBS Process Reference: UCC23513QDWRQ1	QBS Package Reference: ISO6763QDWRQ1	QBS Package Reference: ISO7721QDWRQ1	QBS Product Reference: ISO7710QDWRQ1
Automotive Grade Level	Grade 1	Grade 1	Grade 1	Grade 1	Grade 1
Operating Temp Range (C)	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125
Product Function	Interface	Power Management	Interface	Interface	Interface
Wafer Fab Supplier	RFAB, RFAB	RFAB, RFAB	RFAB, RFAB	RFAB, RFAB	RFAB, RFAB
Assembly Site	MLA	TAI	MLA	MLA	MLA
Package Group	SOIC	SOIC	SOIC	SOIC	SOIC
Package Designator	DW	DWY	DW	DW	D
Pin Count	16	6	16	16	8

QBS: Qual By Similarity

Qual Device ISO7710QDWRQ1 is qualified at MSL2 260C

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: ISO7710QDWRQ1	QBS Process Reference: UCC23513QDWYQ1	QBS Package Reference: ISO6763QDWRQ1	QBS Package Reference: ISO7721QDWRQ1	QBS Product Reference: ISO7710QDRQ1
Test Group A - Accelerated Environment Stress Tests												
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	MSL2 260C	-	-	-	No Fails	-	-
HAST	A2	JEDEC JESD22-A110	3	77	Biased HAST	130C/85%RH	96 Hours	-	-	3/231/0	-	-
AC/UHAST	A3	JEDEC JESD22-A102/JEDEC JESD22-A118	3	77	Autoclave	121C/15psig	96 Hours	-	-	3/231/0	-	-
TC	A4	JEDEC JESD22-A104 and Appendix 3	3	77	Temperature Cycle	-65C/150C	500 Cycles	-	-	3/231/0	-	-
HTSL	A6	JEDEC JESD22-A103	1	45	High Temperature Storage Life	150C	1000 Hours	-	-	3/135/0	-	-
Test Group B - Accelerated Lifetime Simulation Tests												
HTOL	B1	JEDEC JESD22-A108	3	77	Life Test	125C	1000 Hours	-	3/231/0	-	-	-
ELFR	B2	AEC Q100-008	3	800	Early Life Failure Rate	125C	48 Hours	-	3/2400/0	-	-	-
Test Group C - Package Assembly Integrity Tests												
WBS	C1	AEC Q100-001	1	30	Wire Bond Shear	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	-	-	3/90/0	1/30/0	-
WBP	C2	MIL-STD883 Method 2011	1	30	Wire Bond Pull	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	-	-	3/90/0	1/30/0	-
SD	C3	JEDEC J-STD-002	1	15	PB Solderability	>95% Lead Coverage	-	-	-	-	-	-
SD	C3	JEDEC J-STD-002	1	15	PB-Free Solderability	>95% Lead Coverage	-	-	-	-	-	-
PD	C4	JEDEC JESD22-B100 and B108	3	10	Physical Dimensions	Cpk>1.67	-	-	-	-	1/10/0	-
Test Group D - Die Fabrication Reliability Tests												
EM	D1	JESD61	-	-	Electromigration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
Tddb	D2	JESD35	-	-	Time Dependent Dielectric Breakdown	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
HCI	D3	JESD60 & 28	-	-	Hot Carrier Injection	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
BTI	D4	-	-	-	Bias Temperature Instability	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
SM	D5	-	-	-	Stress Migration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
Test Group E - Electrical Verification Tests												
ESD	E2	AEC Q100-002	1	3	ESD HBM	-	2000 Volts	Device specific data [1]	1/3/0	-	-	1/3/0
ESD	E3	AEC Q100-011	1	3	ESD CDM	-	500 Volts	Device specific data [1]	1/3/0	-	1/3/0	1/3/0
LU	E4	AEC Q100-004	1	6	Latch-Up	Per AEC Q100-004	-	Device specific data [1]	1/6/0	-	-	1/6/0
ED	E5	AEC Q100-009	3	30	Electrical Distributions	Cpk>1.67 Room, hot, and cold	-	Device specific data [1]	3/90/0	3/90/0	-	1/30/0

Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable

The following are equivalent HTOL options based on an activation energy of 0.7eV : 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours

The following are equivalent HTSL options based on an activation energy of 0.7eV : 150C/1k Hours, and 170C/420 Hours

The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles

Ambient Operating Temperature by Automotive Grade Level:

Grade 0 (or E): -40C to +150C

Grade 1 (or Q): -40C to +125C

Grade 2 (or T): -40C to +105C

Grade 3 (or I) : -40C to +85C

E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):

Room/Hot/Cold : HTOL, ED

Room/Hot : THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU

Room : AC/Uhast

[1] Qual Device: ISO7710QDWRQ1 and QBS Reference: ISO7710QDRQ1 use the same silicon die.

Quality and Environmental data is available at TI's external Web site: <http://www.ti.com/>

Qualification Report

(Automotive Qualification Summary

(As per AEC-Q100 Rev. H and JEDEC Guidelines)

Approve Date 30-January-2024

Product Attributes

Attributes	Qual Device: ISO7721QDWRQ1	Qual Device: ISO7720QDWRQ1	QBS Process Reference: UCC23513QDWYQ1	QBS Package Reference: ISO6763QDWRQ1	QBS Product Reference: ISO7721QDRQ1	QBS Product Reference: ISO7720QDRQ1
Automotive Grade Level	Grade 1	Grade 1	Grade 1	Grade 1	Grade 1	Grade 1
Operating Temp Range (C)	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125
Product Function	Interface	Interface	Power Management	Interface	Signal Chain,Interface	Signal Chain,Interface
Wafer Fab Supplier	RFAB, RFAB	RFAB, RFAB	RFAB, RFAB	RFAB, RFAB	RFAB, RFAB	RFAB, RFAB
Assembly Site	MLA	MLA	TAI	MLA	MLA	MLA
Package Group	SOIC	SOIC	SOIC	SOIC	SOIC	SOIC
Package Designator	DW	DW	DWY	DW	D	D
Pin Count	16	16	6	16	8	8

QBS: Qual By Similarity

Qual Device ISO7721QDWRQ1 is qualified at MSL2 260C

Qual Device ISO7720QDWRQ1 is qualified at MSL2 260C

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: ISO7721QDWRQ1	Qual Device: ISO7720QDWRQ1	QBS Process Reference: UCC23513QDWYQ1	QBS Package Reference: ISO6763QDWRQ1	QBS Product Reference: ISO7721QDRQ1	QBS Product Reference: ISO7720QDRQ1
Test Group A - Accelerated Environment Stress Tests													
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	MSL2 260C	-	-	-	-	-	No Fails	No Fails
HAST	A2	JEDEC JESD22-A110	3	77	Biased HAST	130C/85%RH	96 Hours	-	-	-	-	3/231/0	-
AC/UHAST	A3	JEDEC JESD22-A102/JEDEC JESD22-A118	3	77	Autoclave	121C/15psig	96 Hours	-	-	-	-	3/231/0	-
TC	A4	JEDEC JESD22-A104 and Appendix 3	3	77	Temperature Cycle	-65C/150C	500 Cycles	-	-	-	-	3/231/0	1/77/0
HTSL	A6	JEDEC JESD22-A103	1	45	High Temperature Storage Life	150C	1000 Hours	-	-	-	-	3/135/0	-
Test Group B - Accelerated Lifetime Simulation Tests													
HTOL	B1	JEDEC JESD22-A108	3	77	Life Test	125C	1000 Hours	-	-	3/231/0	-	-	-
ELFR	B2	AEC Q100-008	3	800	Early Life Failure Rate	125C	48 Hours	-	-	3/2400/0	-	-	-
Test Group C - Package Assembly Integrity Tests													

WBS	C1	AEC Q100-001	1	30	Wire Bond Shear	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	1/30/0	-	3/90/0	3/90/0	1/30/0	-
WBP	C2	MIL-STD883 Method 2011	1	30	Wire Bond Pull	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	1/30/0	-	3/90/0	3/90/0	1/30/0	-
SD	C3	JEDEC J-STD-002	1	15	PB Solderability	>95% Lead Coverage	-	-	-	1/15/0	-	-	-
SD	C3	JEDEC J-STD-002	1	15	PB-Free Solderability	>95% Lead Coverage	-	-	-	1/15/0	-	-	-
PD	C4	JEDEC JESD22-B100 and B108	3	10	Physical Dimensions	Cpk>1.67	-	1/10/0	-	3/30/0	-	1/10/0	-
Test Group D - Die Fabrication Reliability Tests													
EM	D1	JESD61	-	-	Electromigration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
TDDb	D2	JESD35	-	-	Time Dependent Dielectric Breakdown	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
HCI	D3	JESD60 & 28	-	-	Hot Carrier Injection	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
BTI	D4	-	-	-	Bias Temperature Instability	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
SM	D5	-	-	-	Stress Migration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
Test Group E - Electrical Verification Tests													
ESD	E2	AEC Q100-002	1	3	ESD HBM	-	2000 Volts	Device specific data [1]	Device specific data [1]	1/3/0	-	1/3/0	1/3/0
ESD	E3	AEC Q100-011	1	3	ESD CDM	-	500 Volts	1/3/0	1/3/0	1/3/0	-	1/3/0	1/3/0
LU	E4	AEC Q100-004	1	6	Latch-Up	Per AEC Q100-004	-	Device specific data [1]	Device specific data [1]	1/6/0	-	1/6/0	1/6/0
ED	E5	AEC Q100-009	3	30	Electrical Distributions	Cpk>1.67 Room, hot, and cold	-	Device specific data [1]	Device specific data [1]	3/90/0	3/90/0	1/30/0	1/30/0

Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable

The following are equivalent HTOL options based on an activation energy of 0.7eV : 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours

The following are equivalent HTSL options based on an activation energy of 0.7eV : 150C/1k Hours, and 170C/420 Hours

The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles

Ambient Operating Temperature by Automotive Grade Level:

Grade 0 (or E): -40C to +150C

Grade 1 (or Q): -40C to +125C

Grade 2 (or T): -40C to +105C

Grade 3 (or I) : -40C to +85C

E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):

Room/Hot/Cold : HTOL, ED

Room/Hot : THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU

Room : AC/uHAST

[1] Data collected for same silicon die in D package

Quality and Environmental data is available at TI's external Web site: <http://www.ti.com/>

Qualification Report

Automotive Qualification Summary
(As per AEC-Q100 Rev. H, AEC-Q006 and JEDEC Guidelines)
Approve Date 19-OCTOBER -2023

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: <u>ISO6763QDWRQ1</u>	Qual Device: <u>UCC21540QDWKRQ1</u>	QBS Reference: <u>PUCC21550ADWKR</u>
Test Group A - Accelerated Environment Stress Tests										
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	MSL2 260C	-	3/597/0	1/199/0	-
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	MSL3 260C	-	-	-	3/693/0
PC	A1.1	-	3	22	SAM Precon Pre	Review for delamination	-	3/66/0	1/22/0	3/66/0
PC	A1.2	-	3	22	SAM Precon Post	Review for delamination	-	3/66/0	1/22/0	3/66/0
HAST	A2.1	JEDEC JESD22-A110	3	77	Biased HAST	130C/85%RH	96 Hours	3/231/0	1/77/0	3/231/0
HAST	A2.1.2	-	3	1	Cross Section, post bHAST, 1X	Post stress cross section	Completed	3/3/0	1/1/0	-
HAST	A2.1.3	-	3	3	Wire Bond Shear, post bHAST, 1X	Post stress	-	3/9/0	1/3/0	3/9/0
HAST	A2.1.4	-	3	3	Bond Pull over Stitch, post bHAST, 1X	Post stress	-	3/9/0	1/3/0	3/9/0
HAST	A2.1.5	-	3	3	Bond Pull over Ball, post bHAST, 1X	Post stress	-	3/9/0	1/3/0	3/9/0
HAST	A2.2	JEDEC JESD22-A110	3	70	Biased HAST	130C/85%RH	192 Hours	3/210/0	1/70/0	3/210/0
HAST	A2.2.1	-	3	22	SAM Analysis, post bHAST, 2X	Review for delamination	Completed	3/66/0	1/22/0	3/66/0
HAST	A2.2.2	-	3	1	Cross Section, post bHAST, 2X	Post stress cross section	Completed	3/3/0	1/1/0	3/3/0
HAST	A2.2.3	-	3	3	Wire Bond Shear, post bHAST, 2X	Post stress	-	3/9/0	1/3/0	3/9/0
HAST	A2.2.4	-	3	3	Bond Pull over Stitch, post bHAST, 2X	Post stress	-	3/9/0	1/3/0	3/9/0
HAST	A2.2.5	-	3	3	Bond Pull over Ball, post bHAST, 2X	Post stress	-	3/9/0	1/3/0	3/9/0
TC	A4.1	JEDEC JESD22-A104 and Appendix 3	3	77	Temperature Cycle	-55C/150C	1000 Cycles	-	-	3/231/0
TC	A4.1	JEDEC JESD22-A104 and Appendix 3	3	77	Temperature Cycle	-65C/150C	500 Cycles	3/231/0	1/77/0	-

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: ISO6763QDWRQ1	Qual Device: UCC21540QDWKRQ1	QBS Reference: PUCC21550ADWKR
TC	A4.1.1	-	3	22	SAM Analysis, post TC 1X	Review for delamination	Completed	3/66/0	1/22/0	3/66/0
TC	A4.1.2	-	3	1	Cross Section, post TC, 1X	Post stress cross section	Completed	3/3/0	1/1/0	-
TC	A4.1.3	-	3	3	Wire Bond Shear, post TC, 1X	Post stress	-	3/9/0	1/3/0	3/9/0
TC	A4.1.4	-	3	3	Bond Pull over Stitch, post TC, 1X	Post stress	-	3/9/0	1/3/0	3/9/0
TC	A4.1.5	-	3	3	Bond Pull over Ball, post TC, 1X	Post stress	-	3/9/0	1/3/0	3/9/0
TC	A4.2	JEDEC JESD22-A104 and Appendix 3	3	70	Temperature Cycle	-55C/150C	2000 Cycles	-	-	3/210/0
TC	A4.2	JEDEC JESD22-A104 and Appendix 3	3	70	Temperature Cycle	-65C/150C	1000 Cycles	3/210/0	1/70/0	-
TC	A4.2.1	-	3	22	SAM Analysis, post TC, 2X	Review for delamination	Completed	3/66/0	1/22/0	3/66/0
TC	A4.2.2	-	3	1	Cross Section, post TC, 2X	Post stress cross section	Completed	3/3/0	1/1/0	3/3/0
TC	A4.2.3	-	3	3	Wire Bond Shear, post TC, 2X	Post stress	-	3/9/0	1/3/0	3/9/0
TC	A4.2.4	-	3	3	Bond Pull over Stitch, post TC, 2X	Post stress	-	3/9/0	1/3/0	3/9/0
TC	A4.2.5	-	3	3	Bond Pull over Ball, post TC, 2X	Post stress	-	3/9/0	1/3/0	3/9/0
HTSL	A6.1	JEDEC JESD22-A103	3	45	High Temperature Storage Life	150C	1000 Hours	3/135/0	1/45/0	-
HTSL	A6.1	JEDEC JESD22-A103	3	45	High Temperature Storage Life	175C	500 Hours	-	-	3/231/0
HTSL	A6.1.1	-	3	1	Cross Section, post HTSL, 1X	Post stress cross section	Completed	3/3/0	1/1/0	3/3/0
HTSL	A6.2	JEDEC JESD22-A103	3	44	High Temperature Storage Life	150C	2000 Hours	3/132/0	1/44/0	-
HTSL	A6.2	JEDEC JESD22-A103	3	44	High Temperature Storage Life	175C	1000 Hours	-	-	3/228/0
HTSL	A6.2.1	-	3	1	Cross Section, post HTSL, 2X	Post stress cross section	Completed	3/3/0	1/1/0	3/3/0
Test Group C - Package Assembly Integrity Tests										
WBS	C1	AEC Q100-001	1	30	Wire Bond Shear	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	3/90/0	3/90/0	3/90/0
WBP	C2	MIL-STD883 Method 2011	1	30	Wire Bond Pull	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	3/90/0	3/90/0	3/90/0

QBS: Qual By Similarity

Qual Device ISO6763QDWRQ1 is qualified at MSL2 260C

Qual Device UCC21540QDWKRQ1 is qualified at MSL3 260C

Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable

The following are equivalent HTOL options based on an activation energy of 0.7eV : 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours

The following are equivalent HTSL options based on an activation energy of 0.7eV : 150C/1k Hours, and 170C/420 Hours

The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles

Ambient Operating Temperature by Automotive Grade Level:

Grade 0 (or E): -40C to +150C

Grade 1 (or Q): -40C to +125C

Grade 2 (or T): -40C to +105C
Grade 3 (or I) : -40C to +85C
E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):
Room/Hot/Cold : HTOL, ED
Room/Hot : THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU
Room : AC/uHAST
Quality and Environmental data is available at TI's external Web site: <http://www.ti.com/>

ZVEI ID reference: SEM-DE-03, SEM-PA-08, SEM-PA-13, SEM-PA-18, SEM-TF-01, SEM-PW-13, SEM-PW-02

For questions regarding this notice, e-mails can be sent to Change Management team or your local Field Sales Representative.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.