

PCN Number:	20240125001.0	PCN Date:	January 26, 2024
Title:	Datasheet for DLPC900		
Customer Contact:	Change Management team	Dept:	Quality Services
Change Type:	Electrical Specification		

PCN Details

Description of Change:

Texas Instruments Incorporated is announcing an information only notification. The product datasheet(s) is being updated as summarized below. The following change history provides further details.



DLPC900
DLPS037G – OCTOBER 2014 – REVISED NOVEMBER 2023

Changes from Revision F (June 2021) to Revision G (November 2023)

Page

• Rearranged list and added DLP5500 DMD to list of supported devices.....	1
• Edited wording of high speed pattern rates, and added clarifying information regarding the DLP500YX.....	1
• Removed number of patterns that Flash memory can hold.....	1
• Corrected SVGA to XGA in Video mode section.....	1
• Added the DLP5500 DMD to the list of devices supported by DLPC900 controller.....	1
• Removed links to pages that are no longer on TI.com	1
• Removed the fan block from Simplified Application	1
• Enumerated the number of 1-bit patterns available for the DLP5500 and all other DMDs.....	1
• Moved placement of footnote 3 in the Trigger Control Pin Function table	3
• Moved pins H23 and G23 from the Reserved Pin Functions table to Port1 and Port2 Channel Data and Control Pin Functions table.....	3
• Moved pins E8, B4, C4, E7, D5, E6, D3, C2, A4, B5, C6, A5, and D7 from Reserved Pin Functions table to Board-Level Test and Debug Pin Functions table.....	3
• Moved pins AD8, AE8, AF9, G24, D26, F23, F22, E24, and D25 from the Reserved Pin Functions table to the Peripheral Interface Pin Functions table.....	3
• Removed extraneous YCbCr reference.....	3
• Added the t_{SB} parameter to Table 5-1 table.....	25
• Removed t_{EW} from Table 5-1 table - duplicates t_{PH}	25
• Added DLPA200 to Figure 5-3	26
• PWRGOOD cannot be used as an early warning signal for an anticipated power down.....	26
• Changed Power Mode = 1 "Standby" instructions for anticipated power down.....	26
• Changed Anticipated Power Down Sequence and Unanticipated Power Down Sequence diagrams to match the behavior of the DLPC900 controller.....	26

• Added DLP5500 DMD to list of supported devices.....	36
• Added XGA resolution to single DLPC900 controller systems for the DLP5500.....	36
• Changed phrasing from 'normal' to 'default'.....	38
• Changed the section name from DLPC900 Memory Space to DLPC900 External Memory Space.....	40
• Updated GPIO signal names.....	44
• Updated GPIO signal names.....	45
• Removed lists of flash memory components and added links to the appropriate BOMs on TI.com	46
• Added information about the number of 1-bit patterns the DLP5500 can pre-load and corrected the 1-bit depth of the DLP670S DMD.....	47
• Added information to the tables about minimum exposure times for the DLP5500.....	47
• Added table listing the number of 1-bit prestored patterns for each DMD.....	47
• Updated Section to include DLP5500 DMD and reordered the DMD names.....	50
• Updated block diagram and added Table 7-1	50
• Updated DMD interface lists to include support for the DLP5500.....	52
• Corrected P1_ bits to [0:9].....	54
• Added information about optional GPIOs for extended external memory access.....	56
• Updated the schematic to reflect the DLP5500.....	58
• Updated Related Documents Table (added DLPLCR55EVM).....	78

The datasheet number will be changing.

Device Family	Change From:	Change To:
DLPC900	DLPS037F	DLPS037G

These changes may be reviewed at the datasheet links provided.

<http://www.ti.com/product/DLPC900>

Reason for Change:

To accurately reflect device characteristics.

Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):

No anticipated impact. This is a specification change announcement only. There are no changes to the actual device

Changes to product identification resulting from this PCN:

None.

Product Affected:

DLPC900AZPC			
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For questions regarding this notice, e-mails can be sent to the Change Management team or your local Field Sales Representative.

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