

PCN Number:	20240117000.2		PCN Date:	January 17, 2024	
Title:	Qualification of LFAB as an additional Wafer Fab site option for select devices				
Customer Contact:	Change Management team		Dept:	Quality Services	
Proposed 1st Ship Date:	Jul 17, 2024		Sample requests accepted until:	Feb 17, 2024*	
*Sample requests received after February 17, 2024 will not be supported.					
Change Type:					
<input type="checkbox"/>	Assembly Site	<input type="checkbox"/>	Design	<input type="checkbox"/>	Wafer Bump Material
<input type="checkbox"/>	Assembly Process	<input type="checkbox"/>	Data Sheet	<input type="checkbox"/>	Wafer Bump Process
<input type="checkbox"/>	Assembly Materials	<input type="checkbox"/>	Part number change	<input checked="" type="checkbox"/>	Wafer Fab Site
<input type="checkbox"/>	Mechanical Specification	<input type="checkbox"/>	Test Site	<input type="checkbox"/>	Wafer Fab Material
<input checked="" type="checkbox"/>	Packing/Shipping/Labeling	<input type="checkbox"/>	Test Process	<input type="checkbox"/>	Wafer Fab Process

PCN Details					
Description of Change:					
Texas Instruments is pleased to announce the addition of LFAB as an additional Wafer Fab site option for the products listed in the "Product Affected" section of this document.					
Current Fab Site			Additional Fab Site		
Current Fab Site	Process	Wafer Diameter	New Fab Site	Process	Wafer Diameter
TSMC-F14	F021	300mm	LFAB	F65	300mm
UMC12i / DM6	F65	300mm			

Qual details are provided in the Qual Data Section.

Reason for Change:
Continuity of supply
Anticipated impact on Form, Fit, Function, Quality or Reliability (positive / negative):
None
Changes to product identification resulting from this PCN:

Device Symbol:

2.3 Package Symbolization and Revision Identification

Figure 2-1 and Table 2-1 describe package symbolization and the device revision code.

Figure 2-1. Package Symbolization for Silicon Revision E

DEVICE REVISION CODE	SILICON REVISION
E	PG2.1 (see following NOTE)
F	PG3.0 (see following NOTE)

Note

- PG2.1 and PG3.0 are functionally equivalent and share the same data sheet specifications.
- PG3.0 was introduced to support the release into additional wafer fab sites.

Current Fab Site Information:

Chip Site	Chip Site Origin Code (20L)	Chip Site Country Code (21L)	Chip Site City
TSMC-F14	T14	TWN	Tainan City
UMC 12i	UMI	SGP	Singapore
DMOS6	DM6	USA	Dallas

Additional Fab Site Information:

New Chip Site	Chip Site Origin Code (20L)	Chip Site Country Code (21L)	Chip Site City
LFAB	LHI	USA	Lehi

Sample product shipping label (not actual product label)

**Product Affected:**

CC2642R1FTWRGZRQ1	CC2662R1FTWRGZRQ1
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Automotive New Product Qualification Summary
(As per AEC-Q100 Rev. H and JEDEC Guidelines)**Product Attributes**

Attributes	Qual Device: CC2642R1FTWRGZRQ1	QBS Process Reference: TMS320F28379SPTPQ	QBS Package Reference: CC2642R1FTWRGZRQ1
Automotive Grade Level	Grade 2	Grade 1	Grade 2
Operating Temp Range (C)	-40 to 105	-40 to 125	-40 to 105
Product Function	Microprocessor	Microprocessor	Microprocessor
Wafer Fab Supplier	LFAB	LFAB	UMCI
Assembly Site	CDAT / CLARK-AT	PHI	CDAT / CLARK-AT
Package Group	QFN	QFP	QFN
Package Designator	RGZ	PTP	RGZ
Pin Count	48	176	48

- QBS: Qual By Similarity
- Qual Device CC2642R1FTWRGZRQ1 is qualified at MSL3 260C

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: CC2642R1TWRGZRQ1	QBS Process Reference: TMS320F28379SPTPQ	QBS Package Reference: CC2642R1TWRGZRQ1
Test Group A - Accelerated Environment Stress Tests										
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	MSL3 260C	-	3/828/0	-	3/828/0
HAST	A2	JEDEC JESD22-A110	3	77	Biased HAST	110C/85%RH	264 Hours	3/231/0	-	3/231/0
ACUHA	A3	JEDEC JESD22-A102/JEDEC JESD22-A118	3	77	Unbiased HAST	110C/85%RH	264 Hours	3/231/0	-	3/231/0
TC	A4	JEDEC JESD22-A104 and Appendix 3	3	77	Temperature Cycle	-55C/125C	1000 Cycles	3/231/0	-	3/231/0
HTSL	A6	JEDEC JESD22-A103	1	45	High Temperature Storage Life	150C	1000 Hours	3/135/0	-	3/135/0
Test Group B - Accelerated Lifetime Simulation Tests										
HTOL	B1	JEDEC JESD22-A108	3	77	Life Test*	105C	1000 Hours	-	-	3/231/0
HTOL	B1	JEDEC JESD22-A108	3	77	Life Test*	125C	1000 Hours	3/231/0	3/231/0	-
ELFR	B2	AEC Q100-008	3	800	Early Life Failure Rate	105C	48 Hours	-	-	2/1600/0
ELFR	B2	AEC Q100-008	3	800	Early Life Failure Rate	125C	24 Hours	3/2400/0	-	1/800/0
ELFR	B2	AEC Q100-008	3	800	Early Life Failure Rate	125C	48 Hours	-	3/2400/0	-
Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: CC2642R1TWRGZRQ1	QBS Process Reference: TMS320F28379SPTPQ	QBS Package Reference: CC2642R1TWRGZRQ1
EDR	B3	AEC Q100-005	3	77	NVM Endurance, Data Retention*	150C	1000 Hours	3/231/0	3/231/0	3/231/0
Test Group C - Package Assembly Integrity Tests										
WBS	C1	AEC Q100-001	1	30	Wire Bond Shear	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	-	-	3/90/0
WBP	C2	MIL-STD883 Method 2011	1	30	Wire Bond Pull	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	-	-	3/90/0
SD	C3	JEDEC J-STD-002	1	15	PB Solderability	>95% Lead Coverage	-	-	-	1/15/0
SD	C3	JEDEC J-STD-002	1	15	PB-Free Solderability	>95% Lead Coverage	-	-	-	1/15/0
PD	C4	JEDEC JESD22-B100 and B108	3	10	Physical Dimensions	Cpk>1.67	-	-	-	3/30/0
Test Group D - Die Fabrication Reliability Tests										
EM	D1	JESD61	-	-	Electromigration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
TDD	D2	JESD35	-	-	Time Dependent Dielectric Breakdown	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
HCI	D3	JESD60 & 28	-	-	Hot Carrier Injection	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
BTI	D4	-	-	-	Bias Temperature Instability	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: CC2642R1TWRGZRQ1	QBS Process Reference: TMS320F28379SPTPO	QBS Package Reference: CC2642R1TWRGZRQ1
SM	D5	-	-	-	Stress Migration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
Test Group E - Electrical Verification Tests										
ESD	E2	AEC Q100-002	1	3	ESD HBM	-	2000 Volts	1/3/0	1/3/0	1/3/0
ESD	E3	AEC Q100-011	1	3	ESD CDM	-	500 Volts	1/3/0	1/3/0	1/3/0
LU	E4	AEC Q100-004	1	6	Latch-Up	Per AEC Q100-004	-	1/6/0	1/6/0	1/6/0
ED	E5	AEC Q100-009	3	30	Electrical Distributions	Cpk>1.67 Room, hot, and cold	-	3/90/0	3/90/0	3/90/0

- Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable
- The following are equivalent HTOL options based on an activation energy of 0.7eV : 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours
- The following are equivalent HTSL options based on an activation energy of 0.7eV : 150C/1k Hours, and 170C/420 Hours
- The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles
- *HTOL/Life Test and EDR/NVM Data Retention units were W/E precycled prior to these stress tests.
- 1 unit of EIPD was discounted on HTOL.

Ambient Operating Temperature by Automotive Grade Level:

- Grade 0 (or E): -40C to +150C
- Grade 1 (or Q): -40C to +125C
- Grade 2 (or T): -40C to +105C
- Grade 3 (or I) : -40C to +85C

E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):

- Room/Hot/Cold : HTOL, ED
- Room/Hot : THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU
- Room : AC/uHAST

Quality and Environmental data is available at TI's external Web site: <http://www.ti.com/>

TI Qualification ID: R-CHG-2206-036

Automotive New Product Qualification Summary (As per AEC-Q100, AEC-Q006, and JEDEC Guidelines)

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: CC2642R1FTWRGZRQ1	QBS Reference: CC2642R1FTWRGZRQ1
Test Group A - Accelerated Environment Stress Tests									
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	MSL3 260C	-	3/828/0	3/828/0
PC	A1.1	-	3	22	SAM Precon Pre	Review for delamination	-	3/66/0	3/66/0
PC	A1.2	-	3	22	SAM Precon Post	Review for delamination	-	3/66/0	3/66/0
HAST	A2.1	JEDEC JESD22-A110	3	77	Biased HAST	110C/85%RH	264 Hours	3/231/0	3/231/0
HAST	A2.1.2	-	3	1	Cross Section, post bHAST, 1X	Post stress cross section	Completed	3/3/0	3/3/0
HAST	A2.1.3	-	3	3	Wire Bond Shear, post bHAST, 1X	Post stress	-	3/9/0	3/9/0

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: CC2642R1FTWRGZRQ1	QBS Reference: CC2642R1FTWRGZRQ1
HAST	A2.1.4	-	3	30	Bond Pull over Stitch, post bHAST, 1X	Post stress	Wires	3/9/0	3/9/0
HAST	A2.1.5	-	3	3	Bond Pull over Ball, post bHAST, 1X	Post stress	-	3/9/0	3/9/0
HAST	A2.2	JEDEC JESD22-A110	3	70	Biased HAST	110C/85%RH	528 Hours	3/210/0	3/210/0
HAST	A2.2.1	-	3	22	SAM Analysis, post bHAST 2X	Review for delamination	Completed	3/66/0	3/66/0
HAST	A2.2.2	-	3	1	Cross Section, post bHAST, 2X	Post stress cross section	Completed	3/3/0	3/3/0
HAST	A2.2.3	-	3	3	Wire Bond Shear, post bHAST, 2X	Post stress	-	3/9/0	3/9/0
HAST	A2.2.4	-	3	30	Bond Pull over Stitch, post bHAST, 2X	Post stress	Wires	3/9/0	3/9/0
HAST	A2.2.5	-	3	3	Bond Pull over Ball, post bHAST, 2X	Post stress	-	3/9/0	3/9/0
TC	A4.1	JEDEC JESD22-A104 and Appendix 3	3	77	Temperature Cycle	-55C/125C	1000 Cycles	3/231/0	3/231/0
TC	A4.1.1	-	3	22	SAM Analysis, post TC 1X	Review for delamination	Completed	3/66/0	3/66/0
TC	A4.1.2	-	3	1	Cross Section, post TC, 1X	Post stress cross section	Completed	3/3/0	3/3/0
TC	A4.1.3	-	3	3	Wire Bond Shear, post TC, 1X	Post stress	-	3/9/0	3/9/0
TC	A4.1.4	-	3	30	Bond Pull over Stitch, post TC, 1X	Post stress	Wires	3/9/0	3/9/0
TC	A4.1.5	-	3	3	Bond Pull over Ball, post TC, 1X	Post stress	-	3/9/0	3/9/0

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: CC2642R1FTWRGZRQ1	QBS Reference: CC2642R1FTWRGZRQ1
TC	A4.2	JEDEC JESD22-A104 and Appendix 3	3	70	Temperature Cycle	-55C/125C	2000 Cycles	3/210/0	3/210/0
TC	A4.2.1	-	3	22	SAM Analysis, post TC, 2X	Review for delamination	Completed	3/66/0	3/66/0
TC	A4.2.2	-	3	1	Cross Section, post TC, 2X	Post stress cross section	Completed	3/3/0	3/3/0
TC	A4.2.3	-	3	3	Wire Bond Shear, post TC, 2X	Post stress	-	3/9/0	3/9/0
TC	A4.2.4	-	3	30	Bond Pull over Stitch, post TC, 2X	Post stress	Wires	3/9/0	3/9/0
TC	A4.2.5	-	3	3	Bond Pull over Ball, post TC, 2X	Post stress	-	3/9/0	3/9/0
HTSL	A6.1	JEDEC JESD22-A103	3	45	High Temperature Storage Life	150C	500 Hours	3/135/0	3/135/0
HTSL	A6.1.1	-	3	1	Cross Section, post HTSL, 1X	Post stress cross section	Completed	3/3/0	3/3/0
HTSL	A6.2	JEDEC JESD22-A103	3	44	High Temperature Storage Life	150C	1000 Hours	3/132/0	3/132/0
HTSL	A6.2.1	-	3	1	Cross Section, post HTSL, 2X	Post stress cross section	Completed	3/3/0	3/3/0
Test Group C - Package Assembly Integrity Tests									
WBS	C1	AEC Q100-001	1	30	Wire Bond Shear	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	-	3/90/0
WBP	C2	MIL-STD883 Method 2011	1	30	Wire Bond Pull	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	-	3/90/0

- QBS: Qual By Similarity
- Qual Device CC2642R1FTWRGZRQ1 is qualified at MSL3 260C
- Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable
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- Room : AC/uHAST

Quality and Environmental data is available at TI's external Web site: <http://www.ti.com/>

TI Qualification ID: R-CHG-2206-036

ZVEI ID: SEM-PW-13, SEM-PS-04

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