PCN Number:		2	20231	0231212000.1				PCN	PCN Date: December 13, 202			
Title:		•						dditional Fab site option, Die Revision, and MLA as an				
		additiona	Il Assembly Site options for select devices									
Custo	omer (Contact:		С	Change Management Team				Dept:			Quality Services
Proposed 1 st Ship Date:				М					nple requests ccepted until:			Jan 13, 2024*
*Sam	iple r	equests r	eceiv	ed af	fter J	a n	13, 2024 wil	l not b	e sup	por	ted.	
Chan	ge Ty	pe:										
\boxtimes	Asse	mbly Site				\boxtimes	Design				Wafer Bump Material	
	Asse	mbly Proce	ess				Data Sheet			Wafer Bump Process		
\boxtimes	Asse	mbly Mate	ria Is				Part number change			X	Wafer Fab Site	
☐ Mechanical Specification				tion			Test Site			X	Wafer Fab Material	
□ Packing/Shipping/Labeli			beling			Test Process				Wafer Fab Process		
	PCN Details											
Desci	rintio	Description of Change:										

Texas Instruments is pleased to announce the qualification of its RFAB fabrication facility as an additional Wafer Fab option & MLA as an additional Assembly site option for the devices listed below.

Cui	rrent Fab Site		Additional Fab site				
Current Fab Site	Process	Wafer Diameter	Additional Fab site	Process	Wafer Diameter		
MIHO8	LBC8LVISO	200mm	RFAB	LBC8LVISO	300mm		

The die was also changed as a result of the process change to accommodate the change in Assembly technology

Construction differences are as follows:

	TAI	MLA
Bond wire composition, diameter	Au, 0.96 mil	Cu, 0.8 mil

Reason for Change:

Supply Continuity

Anticipated impact on Form, Fit, Function, Quality or Reliability (positive / negative):

None

Impact on Environmental Ratings

Checked boxes indicate the status of environmental ratings following implementation of this change. If below boxes are checked, there are no changes to the associated environmental ratings.

RoHS	REACH	Green Status	IEC 62474
	⊠ No Change	⊠ No Change	⊠ No Change

Changes to product identification resulting from this PCN:

Fab Site Information:

Chip Site	Chip Site Origin Code (20L)	Chip Site Country Code (21L)	Chip Site City		
MIHO8	MH8	JPN	Iba ra ki		
RFAB	RFB	USA	Richardson		

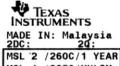
Die Rev:

Current	New
Die Rev [2P]	Die Rev [2P]
۸	^

Assembly Site Information:

Assembly Site	Assembly Site Origin (22L)	Assembly Country Code (23L)	Assembly City	
TI Taiwan	TAI	TWN	Chung Ho, New Taipei City	
TI Malaysia	MLA	MYS	Kuala Lumpur	

Sample product shipping label (not actual product label):



MSL '2 /260C/1 YEAR SEAL DT MSL 1 /235C/UNLIM 03/29/04

OPT: LBL: 5A (L)T0:1750

(1P) \$N74L\$07N\$R (Q) 2000 (D) 0336 (31T)LOT: 3959047MLA (4W) TKY(1T) 7523483812

(2P) REV: (V) 9933317 (20L) CSO: SHE (Z1L) CCO:USA (22L) ASO: MLA (23L) ACO: MYS

Product Affected:

		T	
ISO7760DWR	ISO7761DWR	ISO7762DWR	ISO7763DWR
ISO7760FDWR	ISO7761FDWR	ISO7762FDWR	ISO7763FDWR

Qualification Report Automotive New Product Qualification Summary (As per AEC-Q100 and JEDEC Guidelines)

Approve Date 21-November-2023

Product Attributes

11000011001										
Attributes	Qual Device:	Qual Device:	Qual Device:	Qual Device:	QBS Process Reference:	QBS Package Reference:				
Attributes	ISO7763QDWRQ1	<u>IS07761QDWRQ1</u>	ISO7762QDWRQ1	ISO7760QDWRQ1	UCC23513QDWYQ1	ISO6763QDWRQ1				
Automotive Grade Level	Grade 1	Grade 1	Grade 1	Grade 1	Grade 1	Grade 1				
Operating Temp Range (C)	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125				
Product Function	Interface	Interface	Interface	Interface	Power Management	Interface				
Wafer Fab Supplier	RFAB, RFAB	RFAB, RFAB	RFAB, RFAB	RFAB, RFAB	RFAB, RFAB	RFAB, RFAB				
Assembly Site	MLA	MLA	MLA	MLA	TAI	MLA				
Package Group	SOIC	SOIC	SOIC	SOIC	SOIC	SOIC				
Package Designator	DW	DW	DW	DW	DWY	DW				
Pin Count	16	16	16	16	6	16				

QBS: Qual By Similarity

Qual Device ISO7763QDWRQ1 is qualified at MSL2 260C

Qual Device ISO7761QDWRQ1 is qualified at MSL2 260C

Qual Device ISO7762QDWRQ1 is qualified at MSL2 260C

Qual Device ISO7760QDWRQ1 is qualified at MSL2 260C

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

) is played	401 110		01 1003 /		Tiple Size		QBS Process	QBS Package
Туре	#	Test Spec	Min Lot	SS / Lot	Test Name	Condition	Duration	Qual Device:	Qual Device:	Qual Device:	Qual Device:	Reference:	Reference:
			Qty	200				ISO7763QDWRQ1	ISO7761QDWRQ1	ISO7762QDWRQ1	ISO7760QDWRQ1	UCC23513QDWYQ1	ISO6763QDWRQ1
Test Group	A - Acce	lerated Environ	ment St	ress Te	sts								
PC	A1	JEDEC J- STD-020 JESD22- A113	3	77	Preconditioning	MSL2 260C	-	-	-	-	-	No Fails	No Fails
HAST	A2	JEDEC JESD22- A110	3	77	Biased HAST	130C/85%RH	96 Hours	-	-	-	-	3/231/0	3/231/0
AC/UHAST	A3	JEDEC JESD22- A102/JEDEC JESD22- A118	3	77	Autoclave	121C/15psig	96 Hours	-	-	-	-	3/231/0	3/231/0
тс	A4	JEDEC JESD22- A104 and Appendix 3	3	77	Temperature Cycle	-65C/150C	500 Cycles	-	-	-	-	3/231/0	3/231/0
HTSL	A6	JEDEC JESD22- A103	1	45	High Temperature Storage Life	150C	1000 Hours	-	-	-	-	-	3/135/0
HTSL	A6	JEDEC JESD22- A103	1	45	High Temperature Storage Life	175C	500 Hours	-	-	-	-	3/135/0	-
Test Group I	B - Acce	lerated Lifetime	e Simula	tion Tes	ts								
HTOL	B1	JEDEC JESD22- A108	3	77	Life Test	125C	1000 Hours	-	-	-	-	3/231/0	-
ELFR	B2	AEC Q100- 008	3	800	Early Life Failure Rate	125C	48 Hours	-	-	-	-	3/2400/0	-
Test Group (C - Pack	age Assembly I	Integrity	Tests									
WBS	C1	AEC Q100- 001	1	30	Wire Bond Shear	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	1/30/0	-	-	-	3/90/0	3/90/0
WBP	C2	MIL-STD883 Method 2011	1	30	Wire Bond Pull	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	1/30/0	-	-	-	3/90/0	3/90/0
SD	СЗ	JEDEC J- STD-002	1	15	PB Solderability	>95% Lead Coverage	-	-	-	-	-	1/15/0	-
SD	СЗ	JEDEC J- STD-002	1	15	PB-Free Solderability	>95% Lead Coverage	-	-	-	-	-	1/15/0	-
PD	C4	JEDEC JESD22- B100 and B108	3	10	Physical Dimensions	Cpk>1.67	-	1/10/0	-	-	-	3/30/0	-
Test Group I	D - Die F	abrication Relia	bility Te	sts									
EM	D1	JESD61	-	-	Electromigration			Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
TDDB	D2	JESD35	-	-	Time Dependent Dielectric Breakdown	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
нсі	D3	JESD60 & 28	-	-	Hot Carrier Injection	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
ВТІ	D4	-	-	-	Bias Temperature Instability	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
SM	D5	-	-	-	Stress Migration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
Test Group E	E - Elect	rical Verification	1 Tests										
ESD	E2	AEC Q100- 002	1	3	ESD HBM	-	2000 Volts	1/3/0	1/3/0	1/3/0	1/3/0	1/3/0	-
ESD	E3	AEC Q100- 011	1	3	ESD CDM	-	500 Volts	1/3/0	1/3/0	1/3/0	1/3/0	1/3/0	-
LU	E4	AEC Q100- 004	1	6	Latch-Up	Per AEC Q100-004	-	1/6/0	1/6/0	1/6/0	1/6/0	1/6/0	-
ED	E5	AEC Q100- 009	3	30	Electrical Distributions	Cpk>1.67 Room, hot, and cold	-	1/30/0	1/30/0	1/30/0	1/30/0	3/90/0	3/90/0
	_		_						T D /D:	=	_		—

Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable

The following are equivalent HTOL options based on an activation energy of 0.7eV: 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours

The following are equivalent HTSL options based on an activation energy of $0.7 \, \text{eV}$: $150 \, \text{C/1k}$ Hours, and $170 \, \text{C/420}$ Hours

The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles Ambient Operating Temperature by Automotive Grade Level:

Grade 0 (or E): -40C to +150C Grade 1 (or Q): -40C to +125C Grade 2 (or T): -40C to +105C Grade 3 (or I): -40C to +85C

E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):

Room/Hot/Cold: HTOL, ED

Room/Hot: THB/HAST, TC/PTC, HTSL, ELFR, ESD & LU

Room: AC/uHAST

Quality and Environmental data is available at TI's external Web site: http://www.ti.com/

For questions regarding this notice, e-mails can be sent to the Change Management team or your local Field Sales Representative.

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