October 16, 2023

PCN #	Issue Date	Description
01A-23	July 17, 2023	Initial Release
01B-23	October 16, 2023	Update to all channel 3 usage modes

Subject: PCN# 01A-23 90-Day Notification of Intent to Utilize an Alternate Qualified Mask Set for CertusPro-NX Devices (LFCPNX-50 and LFCPNX-100)

Dear Lattice Customer,

Lattice is providing this notification of our intent to utilize an alternate qualified mask set for the CertusPro-NX Devices (LFCPNX-50 and LFCPNX-100).

Change Descriptions

Lattice is releasing an alternate qualified mask set as a manufacturing enhancement to resolve a SERDES functional capability when channel 3 is used when the PMA clock divider is set to >=2.

If you currently use LFCPNX-50 or LFCPNX-100 and do NOT utilize Channel 3, no further actions are required. If you USE channel 3 (numbering is 0,1,2,3) and do NOT use PMA clock divider >=2, no further actions are required. Continue to order the standard ordering part number. After the PCN implementation date product shipment may utilize either of the qualified mask sets.

If you currently use LFCPNX-50 or LFCPNX-100 AND utilize Channel 3 with PMA clock divider >=2, please ensure that you order from the Alternate Parts Number provided in the Affected Devices list (refer to Appendix A). This will guarantee you receive the latest mask set and the Channel 3 with PMA clock divider >=2 corrected functionality. Additional guidance identifying this usage case in the Radiant tools is outlined in Appendix B.

The use of this alternate qualified mask set will not change form or fit. The alternate qualified mask set will correct Channel 3 with PMA clock divider >=2 functional capability.

Affected Devices

The Ordering Part Numbers (OPNs) affected by this PCN are as follows:

- All LFCPNX-50 and LFCPNX-100 Ordering Part Numbers will utilize the alternate qualified mask set. See table in appendix for complete list.

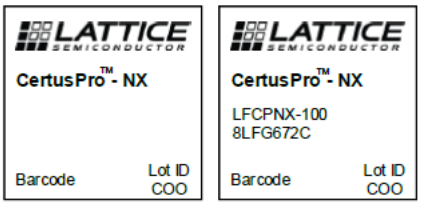
No change in ordering part number is required for customers who are not utilizing Channel 3 and PMA clock divider >=2.

For customers utilizing Channel 3 and PMA clock divider >=2 please use the table in Appendix A for specific ordering part numbers which will guarantee the delivery of the alternate qualified mask set.

This PCN also affects any custom devices (i.e. factory programmed, special test, non-standard speed grade, etc), which are derived from these devices. For any customer utilizing a Custom Device, please contact sales@latticesemi.com for Ordering Information.

Device Identificiation

Devices with this new alternate qualified mask set can be identified by the first alpha character of the Lot ID ("**C**" for the alternative mask product), which is marked on the topside of the device. Inspection lot numbers are also marked on the label on the outside of the inventory box as well as on the anti-static moisture barrier bag within. See device topside marking examples below.



"C" in the first position of Lot ID indicates the alternate mask set
COO = Country Of Origin code

Data Sheet Specifications

This PCN has no impact or change to any data sheet specifications.

Qualification Data

A summary of the qualification and characterization data is available upon request.

Sample Support

Should samples be required to complete evaluation of this PCN, such sample requests must be received no later than August 17, 2023 (30 days after the date of this Notice). Samples will be available based on die/package combination. Please Contact your Sales Person or sales@latticesemi.com for additional information.

PCN Timing

Conversion timing for this PCN is 90 days from the date of this Notice.

- **Sample Request Cut-Off Date: August 17, 2023**
- **PCN Implementation Date: October 17, 2023**

Response

In accordance with J-STD-046, this change is deemed accepted by the customer if no acknowledgement is received within 30 days from this Notice. Lattice PCNs are available on the Lattice website. Please sign up to receive e-mail PCN alerts by registering here. If you already have a Lattice web account and wish to receive PCN alerts, you can do so by logging into your account and making edits to your subscription options.

Contact

If you have any questions or require additional information, please contact sales@latticesemi.com or pcn@latticesemi.com.

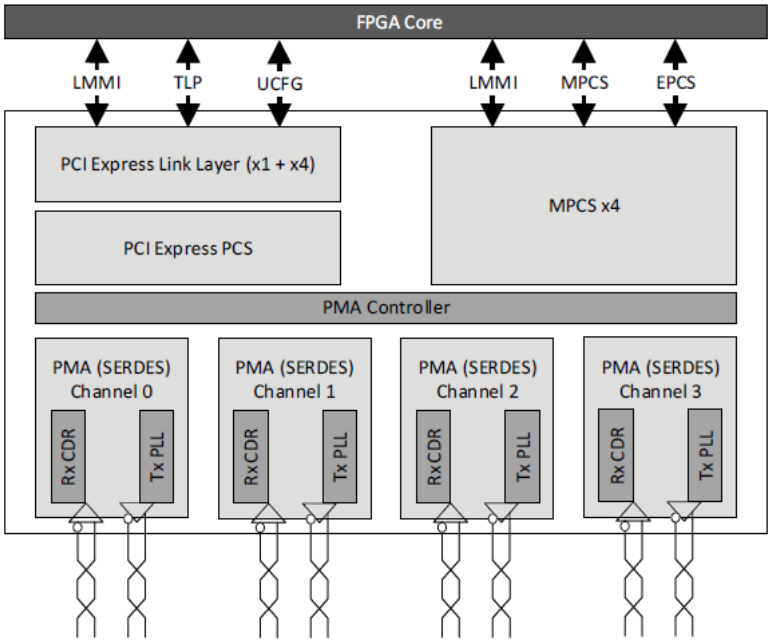
Sincerely,
Lattice Semiconductor PCN Administrator

APPENDIX A - Affected Devices list

Current Part Numbers	Alternate Parts Number
LFCPNX-50-7ASG256C	LFCPNX-50-7ASG256CAPU
LFCPNX-50-7ASG256I	LFCPNX-50-7ASG256IAPU
LFCPNX-50-7BBG484C	LFCPNX-50-7BBG484CAPU
LFCPNX-50-7BBG484I	LFCPNX-50-7BBG484IAPU
LFCPNX-50-7BFG484C	LFCPNX-50-7BFG484CAPU
LFCPNX-50-7BFG484I	LFCPNX-50-7BFG484IAPU
LFCPNX-50-7CBG256C	LFCPNX-50-7CBG256CAPU
LFCPNX-50-7CBG256I	LFCPNX-50-7CBG256IAPU
LFCPNX-50-8ASG256C	LFCPNX-50-8ASG256CAPU
LFCPNX-50-8ASG256I	LFCPNX-50-8ASG256IAPU
LFCPNX-50-8BBG484C	LFCPNX-50-8BBG484CAPU
LFCPNX-50-8BBG484I	LFCPNX-50-8BBG484IAPU
LFCPNX-50-8BFG484C	LFCPNX-50-8BFG484CAPU
LFCPNX-50-8BFG484I	LFCPNX-50-8BFG484IAPU
LFCPNX-50-8CBG256C	LFCPNX-50-8CBG256CAPU
LFCPNX-50-8CBG256I	LFCPNX-50-8CBG256IAPU
LFCPNX-50-9ASG256C	LFCPNX-50-9ASG256CAPU
LFCPNX-50-9ASG256I	LFCPNX-50-9ASG256IAPU
LFCPNX-50-9BBG484C	LFCPNX-50-9BBG484CAPU
LFCPNX-50-9BBG484I	LFCPNX-50-9BBG484IAPU
LFCPNX-50-9BFG484C	LFCPNX-50-9BFG484CAPU
LFCPNX-50-9BFG484I	LFCPNX-50-9BFG484IAPU
LFCPNX-50-9CBG256C	LFCPNX-50-9CBG256CAPU
LFCPNX-50-9CBG256I	LFCPNX-50-9CBG256IAPU
LFCPNX-100-7ASG256A	LFCPNX-100-7ASG256AAPU
LFCPNX-100-7ASG256C	LFCPNX-100-7ASG256CAPU
LFCPNX-100-7ASG256I	LFCPNX-100-7ASG256IAPU
LFCPNX-100-7BBG484A	LFCPNX-100-7BBG484AAPU
LFCPNX-100-7BBG484C	LFCPNX-100-7BBG484CAPU
LFCPNX-100-7BBG484I	LFCPNX-100-7BBG484IAPU
LFCPNX-100-7BFG484C	LFCPNX-100-7BFG484CAPU
LFCPNX-100-7BFG484I	LFCPNX-100-7BFG484IAPU
LFCPNX-100-7CBG256A	LFCPNX-100-7CBG256AAPU
LFCPNX-100-7CBG256C	LFCPNX-100-7CBG256CAPU
LFCPNX-100-7CBG256I	LFCPNX-100-7CBG256IAPU
LFCPNX-100-7LFG672C	LFCPNX-100-7LFG672CAPU
LFCPNX-100-7LFG672I	LFCPNX-100-7LFG672IAPU
LFCPNX-100-8ASG256A	LFCPNX-100-8ASG256AAPU
LFCPNX-100-8ASG256C	LFCPNX-100-8ASG256CAPU
LFCPNX-100-8ASG256I	LFCPNX-100-8ASG256IAPU
LFCPNX-100-8BBG484A	LFCPNX-100-8BBG484AAPU
LFCPNX-100-8BBG484C	LFCPNX-100-8BBG484CAPU
LFCPNX-100-8BBG484I	LFCPNX-100-8BBG484IAPU
LFCPNX-100-8BFG484C	LFCPNX-100-8BFG484CAPU
LFCPNX-100-8BFG484I	LFCPNX-100-8BFG484IAPU
LFCPNX-100-8CBG256A	LFCPNX-100-8CBG256AAPU
LFCPNX-100-8CBG256C	LFCPNX-100-8CBG256CAPU
LFCPNX-100-8CBG256I	LFCPNX-100-8CBG256IAPU
LFCPNX-100-8LFG672C	LFCPNX-100-8LFG672CAPU
LFCPNX-100-8LFG672I	LFCPNX-100-8LFG672IAPU
LFCPNX-100-9ASG256C	LFCPNX-100-9ASG256CAPU
LFCPNX-100-9ASG256I	LFCPNX-100-9ASG256IAPU
LFCPNX-100-9BBG484C	LFCPNX-100-9BBG484CAPU
LFCPNX-100-9BBG484I	LFCPNX-100-9BBG484IAPU
LFCPNX-100-9BFG484C	LFCPNX-100-9BFG484CAPU
LFCPNX-100-9BFG484I	LFCPNX-100-9BFG484IAPU
LFCPNX-100-9CBG256C	LFCPNX-100-9CBG256CAPU
LFCPNX-100-9CBG256I	LFCPNX-100-9CBG256IAPU
LFCPNX-100-9LFG672C	LFCPNX-100-9LFG672CAPU
LFCPNX-100-9LFG672I	LFCPNX-100-9LFG672IAPU

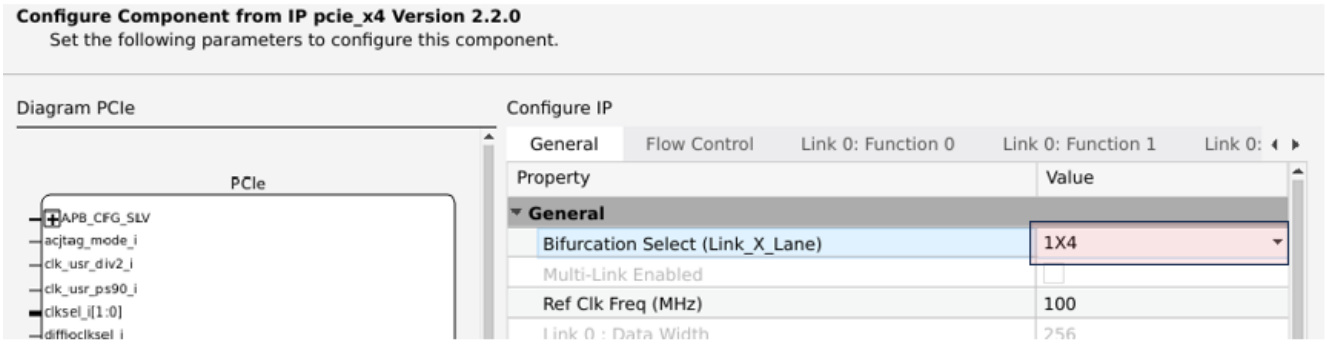
APPENDIX B – Identifying channel 3 and PMA Clk Div >=2

The architecture of the CertusPro-NX SERDES is shown below. The SERDES can be configured for PCI Express, or through the Multiprotocol PCS (MPCS).



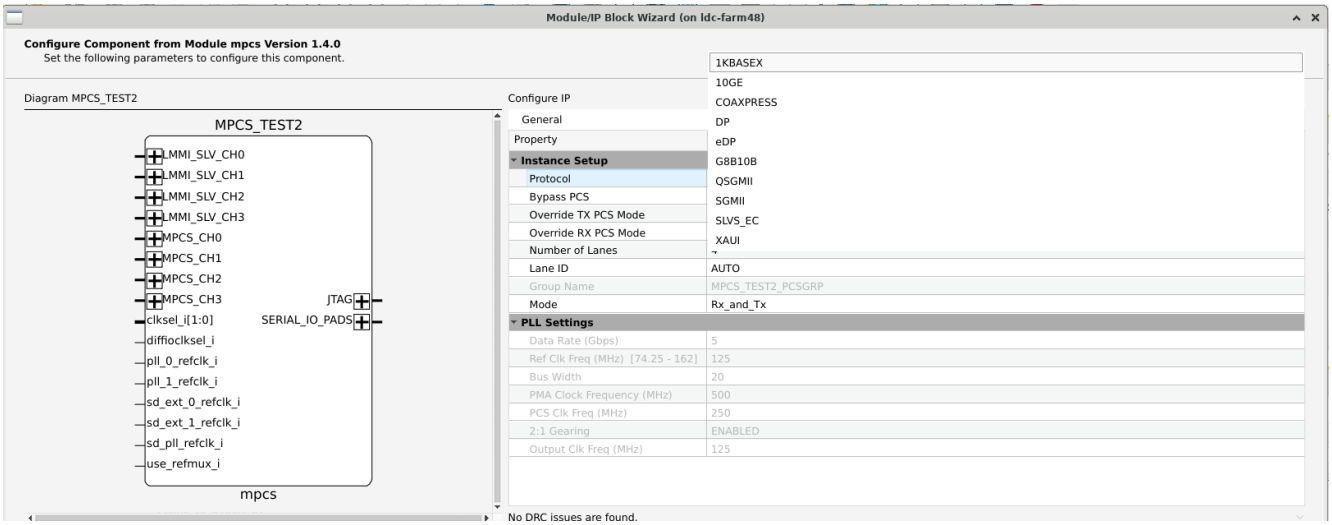
PCIe Express

PCIe is configured to use a clock divider of 2, but you need to confirm use of channel 3. This can be accomplished by double clicking the .ipx file in Radiant and inspect the GUI for x4 mode.



MPCS Protocols

The MPCS block is used to configure all protocols except PCI Express.



Radiant software sets the clock divider to the value shown in the table below:

Protocol		Rate (Gbps)	F_{Ref} (MHz)	PLL Setting			PMA Internal Clock		PMA Output	PMA Clk Div	F_{PCS}[7]	PCS Bus Width	Out Clk Div	F_{OUT}[8]	User Data Bus Width
				M[1]	F[2]	N[3]	F_{VCO}[4]	F_{bit}[5]	F_{PMA}[6]						
Ethernet	10GBASE-R	10.3125	161.1328	1	4	16	10312.5	10312.5	644.53	1	644.53	16	4	161.1328	64
	QSGMII	5	125	2	4	10	10000	5000	500	2	250	20	2	125	40
	XAUI	3.125	156.25	2	2	10	6250	3125	312.5	1	312.5	10	2	156.25	20
	SGMII	1.25	125	8	1	10	10000	1250	125	1	125	10	1	125	10
	1KBASE-X	1.25	125	8	1	10	10000	1250	125	1	125	10	1	125	10
SLVS-EC	Grade 3	5[9]	—	2	4	10	~10000	~5000	~500	2	~250	20	2	~125	40
	Grade 2	2.5[9]	—	4	2	10	~10000	~2500	~250	1	~250	10	2	~125	20
	Grade 1	1.25[9]	—	8	1	10	~10000	~1250	~125	1	~125	10	1	~125	10
CoaXPress	—	6.25	156.25	1	2	20	6250	6250	312.5	1	312.5	20	2	156.25	40
	—	5	125	2	4	10	10000	5000	500	2	250	20	2	125	40
	—	3.125	156.25	2	2	10	6250	3125	312.5	1	312.5	10	2	156.25	20
	—	2.5	125	4	2	10	10000	2500	250	1	250	10	2	125	20
	—	1.25	125	8	1	10	10000	1250	125	1	125	10	1	125	10
DP/eDP	HBR3	8.1	135	1	3	20	8100	8100	405	1	405	20	2	202.5	40
	HBR2	5.4	135	1	2	20	5400	5400	270	1	270	20	2	135	40
	HBR	2.7	135	2	2	10	5400	2700	270	1	270	10	2	135	20
	RBR	1.62	108	4	3	5	6480	1620	324	2	162	10	1	162	10
PCIe	Gen3	8	100	1	5	16	8000	8000	500	N/A	N/A	N/A	N/A	N/A	N/A
	Gen2	5	100	2	5	10	10000	5000	500	N/A	N/A	N/A	N/A	N/A	N/A
	Gen1	2.5	100	4	5	5	10000	2500	500	N/A	N/A	N/A	N/A	N/A	N/A

The G8B10B mode is not listed in the table above and requires manually setting the PMA Clock Divider.

The Radiant design software produces a constraints file for each configured SERDES PHY instance used in the CertusPro-NX design. For instance, if you created an IP instance utilizing the MPCS block named MYPHY, you will find a file called constraints/MYPHY.ldc containing settings. Inspect the variable NUM_LANES for a value of 4 indicating that channel 3 is used (channels are numbered 0, 1, 2 and 3), and the setting TX_RX_DIVMODE_n (where n is 0, 1, or 2) is set to 2 or 4. For example, if you were to inspect your .ldc file and find:

set NUM_LANES 4
set TX_RX_DIVMODE_0 2

then you have a situation where you are using one of the devices in the affected parts list in Appendix A of this PCN.

CertusPro-NX SERDES are constructed as 4 lane quads. Should your protocol utilize an 8 lane mode and PMA clock divider >=2, Radiant will assemble using 2 quads and channels 3 and 7 could experience functionality issues for the affected OPNs shown in Appendix A.

Override Mode

It is possible to manually set the clock divider in user mode through the PMA registers. If you have overwritten the default values, refer to this user guide: CertusPro-NX SerDes/PCS User Guide. Appendix A of this user guide describes the configuration registers to write/read back tx_div_mode0 and rx_div_mode0. Refer to tables A.6 and A.8. Should you have utilized channel 3 and manually set the clock dividers to 2 or 4, follow the instructions for corrective action.