

PCN Number:	20231108002.0	PCN Date:	November 09, 2023
Title:	Datasheet for DS90UB962-Q1, DS90UB960-Q1, and TDES960		
Customer Contact:	Change Management team	Dept:	Quality Services
Change Type:	Electrical Specification		

PCN Details

Description of Change:

Texas Instruments Incorporated is announcing an information only notification. The product datasheet(s) is being updated as summarized below. The following change history provides further details.



DS90UB962-Q1

SNLS573B – AUGUST 2018 – REVISED SEPTEMBER 2023

Changes from Revision A (December 2020) to Revision B (September 2023)	Page
• Fixed spelling errors and minor format issues throughout the document.....	1
• Removed "Port Replication Mode" from the list of device features.....	1
• Updated I2C pull-up resistor recommendations.....	5
• Updated Legend for Pin Functions Table.....	5
• Removed the $t_{CLK-MISS}$ specification from the CSI-2 Timing Specifications table.....	14
• Updated Timing Diagrams section figure titles to align with the figures.....	19
• Removed obstructions in CSI-2 General Frame Format figure to make text clearer.....	19
• Updated the title of the section with timing figures to Timing Diagrams.....	19
• Clarified the clock speed and the configuration settings of non-synchronous clock mode.....	25
• Added information about YUV support.....	26
• Added clarification that MODE pin option 0 straps the device to CSI-2 Non-Synchronous back channel and MODE pin option 4 straps the device to CSI-2 Synchronous back channel.....	26
• Changed I2C terminology to "Controller" and "Target".....	28
• Added a channel requirements section to the datasheet.....	30
• Removed mention of older silicon.....	41
• Removed CSI-2 Transmitter Frequency script example for unsupported CSI-2 port.....	41
• Added cross-links in the CSI-2 Output Bandwidth section to relevant figures in the Timing Diagrams section.....	42
• Added a sentence to clarify that V_{I2C} must match the voltage applied to VDDIO.....	53
• Reworded the Serial Control Bus section to reference V_{I2C} instead of VDDIO.....	53
• Added register addresses for the RX Port ID registers.....	56
• Removed information suggesting that the Rx Port intended for messaging must always be selected with Register 0x4C when communicating with a remote target device.....	56
• Corrected the total number of TargetID and Target Alias pairs of registers for the device.....	57
• Clarified that the write enable bit in register 0x4C needs to be set before configuring remote target addresses.....	57
• Added additional information about how to configure a broadcast write to remote devices.....	57
• Removed unnecessary register writes in the Code Example for Broadcast Write.....	57

• Updated the I2C Controller Proxy description.....	57
• Fixed register address errors in the Typical I2C Timing Register Settings table.....	57
• Removed details about the internal reference clock.....	57
• Corrected typo that mentions two CSI-2 Transmit ports in the Interrupt Support section.....	58
• Replaced CABLE_FAULT with NO_FPD3_CLK in the interrupt readback example script to match the register bit name.....	59
• Clarified instructions for how to configure Pattern Generation on the CSI-2 Port.....	65
• Removed all RESERVED registers from the datasheet.....	69
• Updated description of registers 0x10-0x17 to remove mention of unsupported CSI-2 TX Port.....	69
• RESERVED register bits 0x20[3:0] that have no customer use case.....	69
• RESERVED register bit 0x32[4] that has no customer use case.....	69
• Made register bits 0x34[5:4] public and updated the description of register bit 0x34[1].....	69
• Corrected a bit description typo for bit 4 of register 0x4A.....	69
• Updated the description of register bit 0x4E[1] to clarify functionality.....	69
• Updated the description sections of registers 0x51-0x54.....	69
• Fixed typos in the description for registers 0x90-0x97.....	69
• Removed RESERVED indirect register pages in the description of register bits 0xB0[5:2].....	69
• Made register 0xB6 public.....	69
• Updated the bit description of 0xB9[3:0].....	69
• Updated the name of Indirect Register Page 0 to PATGEN_AND_CSI-2.....	69
• Updated the PoC description.....	154
• Updated all typical connection diagrams to include a reference to App Note SLVA689.....	158
• Added clarification for the recommended ferrite bead characteristics on the power supply rails.....	158
• Removed optional 10 kΩ pull-down resistor on Pin 4 in the Typical Connection Diagram.....	158
• Added clarification for the NC pin connections in the Typical Connection Diagram.....	158
• Updated MIPI CSI-2 D-PHY layout recommendations.....	167



DS90UB960-Q1

SNLS589D – AUGUST 2016 – REVISED SEPTEMBER 2023

Changes from Revision C (December 2020) to Revision D (September 2023)	Page
• Fixed spelling errors and minor format issues throughout the document.....	1
• Updated I2C pull-up resistor recommendations.....	5
• Updated Legend for Pin Functions Table.....	5
• Removed the $t_{CLK-MISS}$ specification from the CSI-2 Timing Specifications table.....	14
• Updated Timing Diagrams section figure titles to align with the figures.....	20
• Removed obstructions in CSI-2 General Frame Format figure to make text clearer.....	20
• Updated the title of the section with timing figures to Timing Diagrams.....	20
• Clarified the clock speed and the configuration settings of non-synchronous clock mode.....	27
• Added information about YUV support.....	28
• Added clarification that MODE pin option 0 straps the device to CSI-2 Non-Synchronous back channel and MODE pin option 4 straps the device to CSI-2 Synchronous back channel.....	28
• Changed I2C terminology to "Controller" and "Target".....	30
• Updated the transmission channel requirements for Coaxial and STP/STQ Cable Applications.....	32
• Removed mention of older silicon.....	44
• Added cross-links in the CSI-2 Output Bandwidth section to relevant figures in the Timing Diagrams section.....	45
• Clarified that CSI-2 forwarding should be disabled before CSI-2 replicate mode is enabled.....	55
• Added a sentence to clarify that V_{I2C} must match the voltage applied to VDDIO.....	56
• Reworded the Serial Control Bus section to reference V_{I2C} instead of VDDIO.....	56
• Added register addresses for the RX Port ID registers.....	59
• Removed information suggesting that the Rx Port intended for messaging must always be selected with Register 0x4C when communicating with a remote target device.....	59
• Corrected the total number of TargetID and TargetAlias pairs of registers for the device.....	60
• Clarified that the write enable bit in register 0x4C needs to be set before configuring remote target addresses.....	60
• Added additional information about how to configure a broadcast write to remote devices.....	60
• Removed unnecessary register writes in the Code Example for Broadcast Write.....	60
• Updated the I2C Controller Proxy description.....	60

• Fixed register address errors in the Typical I2C Timing Register Settings table.....	60
• Removed details about the internal reference clock.....	60
• Replaced CABLE_FAULT with NO_FPD3_CLK in the interrupt readback example script to match the register bit name.....	62
• Clarified instructions for how to configure Pattern Generation on the CSI-2 Ports.....	68
• Removed all RESERVED registers from the datasheet.....	72
• Made register bits 0x34[5:4] public and updated the description of register bit 0x34[1].....	72
• Corrected a bit description typo for bit 4 of register 0x4A.....	72
• Updated the description of register bit 0x4E[1] to clarify functionality.....	72
• Updated the description sections of registers 0x51-0x54.....	72
• Fixed typos in the description for registers 0x90-0x9F.....	72
• Removed RESERVED indirect register pages in the description of register bits 0xB0[5:2].....	72
• Made register 0xB6 public.....	72
• Updated the bit description of 0xB9[3:0].....	72
• Updated the name of Indirect Register Page 0 to PATGEN_AND_CSI-2.....	72
• Updated the PoC description.....	163
• Updated all typical connection diagrams to include a reference to App Note SLVA689.....	167
• Added clarification for the recommended ferrite bead characteristics on the power supply rails.....	167
• Removed optional 10 kΩ pulldown resistor on Pin 4 in the Typical Connection Diagram.....	167
• Updated MIPI CSI-2 D-PHY layout recommendations.....	178



Changes from Revision * (April 2021) to Revision A (September 2023)

	Page
• Fixed spelling errors and minor format issues throughout the document.....	1
• Updated I2C pull-up Resistor Recommendations.....	4
• Updated Legend for Pin Functions Table.....	4
• Removed the t _{CLK-MISS} specification from the CSI-2 Timing Specifications table.....	14
• Removed obstructions in CSI-2 General Frame Format figure to make text clearer.....	20
• Clarified the clock speed and the configuration settings of non-synchronous clock mode	27
• Added clarification that MODE pin option 0 straps the device to CSI-2 Non-Synchronous back channel and MODE pin option 4 straps the device to CSI-2 Synchronous back channel.....	28
• Changed I2C terminology to "Controller" and "Target".....	30
• Updated the transmission channel requirements for Coaxial and STP/STQ Cable Applications.....	31
• Removed mention of older silicon.....	43
• Clarified that CSI-2 forwarding should be disabled before CSI-2 replicate mode is enabled.....	54
• Added a sentence to clarify that V _{I2C} must match the voltage applied to VDDIO.....	56
• Reworded the Serial Control Bus section to reference V _{I2C} instead of VDDIO.....	56
• Added register addresses for the RX Port ID registers.....	58
• Removed information suggesting that the Rx Port intended for messaging must always be selected with Register 0x4C when communicating with a remote target device.....	58
• Corrected the total number of TargetID and TargetAlias pairs of registers for the device.....	59
• Clarified that the write enable bit in register 0x4C needs to be set before configuring remote target addresses.....	59
• Added additional information about how to configure a broadcast write to remote devices.....	59
• Updated the I2C Controller Proxy description	59
• Fixed register address errors in the Typical I2C Timing Register Settings table.....	59
• Removed details about the internal reference clock.....	59
• Clarified instructions for how to configure Pattern Generation on the CSI-2 Ports.....	67
• Removed all RESERVED registers from the datasheet.....	71
• Made register bits 0x34[5:4] public and updated the description of register bit 0x34[1].....	71
• Corrected a bit description typo for bit 4 of register 0x4A.....	71
• Updated description of register 0x4E[1] to clarify functionality.....	71

• Updated the description sections of registers 0x51-0x54.....	71
• Fixed typos in the description for registers 0x90-0x9F.....	71
• Removed RESERVED indirect register pages in the description of register bits 0xB0[5:2].....	71
• Made register 0xB6 public.....	71
• Updated the bit description of 0xB9[3:0].....	71
• Updated the name of Indirect Register Page 0 to PATGEN_AND_CSI-2.....	71
• Updated the PoC description.....	162
• Updated both typical connection diagrams to include a reference to App Note SLVA689.....	166
• Added clarification for the recommended ferrite bead characteristics on the power supply rails.....	166
• Removed optional 10 kΩ pulldown resistor on Pin 4 in the Typical Connection Diagram.....	166
• Fixed part number typo in the Power-Up Sequencing With Non-Synchronous Clocking Mode figure	173
• Updated MIPI CSI-2 D-PHY layout recommendations.....	177

The datasheet number will be changing.

Device Family	Change From:	Change To:
DS90UB962-Q1	SNLS573A	SNLS573B
DS90UB960-Q1	SNLS589C	SNLS589D
TDES960	SNLS698	SNLS698A

These changes may be reviewed at the datasheet links provided.

<http://www.ti.com/product/DS90UB962-Q1>

<http://www.ti.com/product/DS90UB960-Q1>

<http://www.ti.com/product/TDES960>

Reason for Change:

To accurately reflect device characteristics.

Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):

No anticipated impact. This is a specification change announcement only. There are no changes to the actual device

Changes to product identification resulting from this PCN:

None.

Product Affected:

DS90UB962WRTDRQ1	DS90UB962WRTDTQ1	DS90UB960WRTDRQ1	DS90UB960WRTDTQ1	
TDES960RTDR	TDES960RTDT			

For questions regarding this notice, e-mails can be sent to the Change Management team or your local Field Sales Representative.

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