PCN Number:	20231106002.0	PCN Date:	November 09, 2023
Title:	Datasheet for AM64x		
Customer Contact:	Change Management team	Dept:	Quality Services
Change Type:	Electrical Specification		

PCN Details

Description of Change:

Texas Instruments Incorporated is announcing an information only notification.
The product datasheet(s) is being updated as summarized below.
The following change history provides further details.

Changes from September 22, 2022 to October 31, 2023 (from Revision E (SEPTEMBER 2022) to Revision F (OCTOBER 2023)) **Page**

- (Features): Updated the Security features to clarify what is supported....1
- (Package Information): Updated the table to match the new content standard....4
- (Functional Block Diagram): Updated URL for Software Build Sheet....5
- (Device Comparison): Updated URL for Software Build Sheet....10
- (Device Comparison): Corrected the name of the JTAG User ID register....10
- (Device Comparison): Defined the R5F cores enabled in each device and changed the R5F TCM memory size from "256KB" to "4 x 64KB" in the 2 x Dual Core devices, and "2 x 128KB" in the 2 x Single Core devices....10
- (Device Comparison): Added Functional Safety Optional for AM6422....10
- (Device Comparison): Changed General-Purpose Memory Controller (GPMC) address range from 1GB to 128MB....10
- (GPMC0 Signal Descriptions): Moved the GPMC0_FCLK_MUX signal from System Signal Descriptions to GPMC0 Signal Descriptions....59
- (System Signal Descriptions): Moved the GPMC0_FCLK_MUX signal from System Signal Descriptions to GPMC0 Signal Descriptions....59
- (Pin Connectivity Requirements): Updated the second paragraph of the note following the Connectivity Requirements table. The update clarifies the operation of configurable device IOs and includes precautions that must be taken to prevent floating signals from damaging device input buffers....94
- (Specifications): Remove note that says specifications are preliminary....99
- (Power-On Hours): Updated the table to match the new content standard....101
- (Recommended Operating Conditions): Added the Automotive temperature range....102
- (I2C OD FS Electrical Characteristics): Changed the I_{OL} minimum value from 20 to 10 for both 1.8 V and 3.3 V modes....104
- (DDR Electrical Characteristics): Added references to the respective JEDEC standards....109
- (System Timing): Removed the Timing Conditions table from this section and added separate Timing Conditions tables to each of the Reset Timing, Safety Signal Timing, and Clock Timing sections....118
- (Reset Timing): Added Timing Conditions table to define conditions specific to reset inputs and outputs....118
- (MCU_RESETSTATz, and RESETSTATz Switching Characteristics): Changed the minimum value of parameter RST8 from "4040*S" to "966*S" and the minimum value of parameter RST9 from "301200" to "4040*S"....118
- (MCU_RESETSTATz, and RESETSTATz Switching Characteristics): Changed the minimum value of parameter RST13 from "0" to "960"....118
- (RESETSTATz Switching Characteristics): Changed the minimum value of parameter RST16 from "T" to "900*T", the minimum value of parameter RST17 from "W" to "4040*S", and replaced the contents of table note 2....118
- (PORz_OUT Switching Characteristics): Changed the minimum value of parameter RST26 from "0" to "1840"....118
- (Safety Signal Timing): Added Timing Conditions table to define conditions specific to MCU_SAFETY_ERRORn output....123

- (MCU_ERRORn Switching Characteristics): Changed "RST22" to "SFTY3" in table note 5.....123
- (Clock Timing): Added Timing Conditions table to define conditions specific to clock inputs and outputs.....124
- (Clock Timing Requirements): Updated the Timing Requirements figure with a single generic waveform and updated the parameter numbers in the Timing Requirements table to reference the generic clock waveform.....124
- (Clock Switching Characteristics): Updated the Switching Characteristics figure with a single generic waveform and updated the parameter numbers in the Switching Characteristics table to reference the generic clock waveform.....124
- (MCU_OSC0 Crystal Implementation): Changing the crystal oscillator circuit diagram back to the original version used in previous revisions of this document.....127

- (CPSW3G MDIO Timing): Included PCB Connectivity Requirements in the Timing Conditions table, changed the minimum setup time value (parameter MDIO1) from "90" to "45", and changed the minimum and maximum output delay time values (parameter MDIO7) from "-150" and "150" to "-10" and "10" respectively.....133
- (GPMC0 IOSETs): Removed GPMC0_CLKLB since there is no pin with this name 171
- (MCSPI Switching Characteristics - Controller Mode): Replaced previous table notes 2 and 3 with new table notes 2, 3, 4, and 5.....176
- (MMC0 Timing Requirements – Legacy SDR Mode): Changed the minimum values for LSDR1 and LSDR3 from 9.69 to 1.56, and the minimum values for LSDR2 and LSDR4 from 27.97 to 5.44.....183
- (MMC0 Switching Characteristics – Legacy SDR Mode): Changed the minimum values for LSDR8 and LSDR9 from -16.1 to -2.3, and the maximum values for HSSDR8 and HSSDR9 from 16.1 to 2.9.....183
- (MMC0 Timing Requirements – High Speed SDR Mode): Changed the minimum values for HSSDR1 and HSSDR3 from 2.99 to 2.55.....184
- (MMC0 Switching Characteristics – High Speed SDR Mode): Changed the minimum values for HSSDR8 and HSSDR9 from -6.35 to -2.3, and the maximum values for HSSDR8 and HSSDR9 from 6.35 to 2.9.....184
- (MMC0 Timing Requirements – High Speed DDR Mode): Changed the minimum values for HSDDR1 from 3.88 to 1.62, and the minimum values for HSDDR2 from 2.67 to 2.52.....185
- (MMC0 Switching Characteristics – High Speed DDR Mode): Changed the maximum value for HSDDR8 from 16.19 to 7.65.....185
- (MMC1 DLL Delay Mapping for All Timing Modes): Changed the value of OTAPDLYENA from 0x0 to 0x1 for Default Speed and High Speed modes. Also changed UHS-I DR50 to UHS-I DDR50 to correct a typographical error in the mode name.....187
- (Timing Requirements for MMC1 – Default Speed Mode): Changed the minimum values for DS1 and DS3 from 2.55 to 2.15, and the minimum values for DS2 and DS2 from 19.67 to 1.67.....189
- (Switching Characteristics for MMC1 – Default Speed Mode): Changed the minimum values for DS8 and DS9 from -14.1 to -1.8, and the maximum values for DS8 and DS9 from 14.1 to 1.8.....189
- (Timing Requirements for MMC1 – High Speed Mode): Changed the minimum values for HS1 and HS3 from 2.55 to 2.15, and the minimum values for HS2 and HS2 from 2.67 to 1.67.....190
- (Switching Characteristics for MMC1 – High Speed Mode): Changed the minimum values for HS8 and HS9 from -7.35 to -1.8, and the maximum values for HS8 and HS9 from 3.35 to 1.8.....190
- (Timing Requirements for MMC1 – UHS-I SDR12 Mode): Changed the minimum values for SDR121 and SDR123 from 21.65 to 2.35.....191
- (Switching Characteristics for MMC1 – UHS-I SDR12 Mode): Changed the minimum values for SDR128 and SDR129 from -13.6 to 1.2, and the maximum values for SDR128 and SDR129 from 13.6 to 8.....191
- (Timing Requirements for MMC1 – UHS-I SDR25 Mode): Changed the minimum values for SDR251 and SDR253 from 2.15 to 1.95.....192
- (Switching Characteristics for MMC1 – UHS-I SDR25 Mode): Changed the minimum values for SDR258 and SDR259 from -7.1 to 2.4, and the maximum values for SDR258 and SDR259 from 3.1 to 8.....192
- (Timing Requirements for MMC1 – UHS-I DDR50 Mode): Removed Timing Requirements since the UHS-I DDR50 mode requires a tuning algorithm to be used for optimal input timing.....194
- (Switching Characteristics for MMC1 – UHS-I DDR50 Mode): Changed the maximum value for DDR508 from 13.1 to 6.35.....194
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- (OSPI Switching Characteristics – PHY Data Training): Added maximum values to the OSPI0_CLK Cycle Time parameter (O1) to define a minimum operating frequency of 133MHz. Also updated Note 1 and Note 4, where "in ns" was added to the OSPI_CLK cycle time reference in Note 1 and "refclk" was changed to "reference clock" in Note 4 so it matches the clock name used in the TRM..... 199
- (OSPI0 Switching Characteristics – PHY SDR Mode): Updated Note 1 and Note 4, where "in ns" was added to the OSPI_CLK cycle time reference in Note 1 and "refclk" was changed to "reference clock" in Note 4 so it matches the clock name used in the TRM..... 201
- (OSPI0 Switching Characteristics – PHY DDR Mode): Updated Note 1 and Note 4, where "in ns" was added to the OSPI_CLK cycle time reference in Note 1 and "refclk" was changed to "reference clock" in Note 4 so it matches the clock name used in the TRM..... 203

- (OSPI0 Timing Requirements – Tap SDR Mode): Updated the constant values associated with the minimum setup and minimum hold formulas in parameters O19 and O20. Note 2 was also updated to change "refclk" to "reference clock" so it matches the clock name used in the TRM.....205
- (OSPI0 Switching Characteristics – Tap SDR Mode): Updated Note 1 and Note 4, where "in ns" was added to the OSPI_CLK cycle time reference in Note 1 and "refclk" was changed to "reference clock" in Note 4 so it matches the clock name used in the TRM..... 205
- (OSPI0 Timing Requirements – Tap DDR Mode): Updated the constant values associated with the minimum setup and minimum hold formulas in parameters O13 and O14. Note 2 was also updated to change "refclk" to "reference clock" so it matches the clock name used in the TRM.....207
- (OSPI0 Switching Characteristics – Tap DDR Mode): Changed the "OSPI_RD_DATA_CAPTURE_REG" bit field from "DELAY_FLD" to "DDR_READ_DELAY_FLD" in the note associated with parameter O6.....207
- (OSPI0 Switching Characteristics – Tap DDR Mode): Updated the minimum data output delay and maximum data output delay formulas in parameter O6. Also updated Note 1 and Note 5, where "in ns" was added to the OSPI_CLK cycle time reference in Note 1 and "refclk" was changed to "reference clock" in Note 5 so it matches the clock name used in the TRM..... 207
- (PCIe): Updated the "For more details about features and ..." paragraph.....208
- (PRUSS PRU Switching Characteristics – Direct Output Mode): Changed the maximum skew value for the GPO to GPO parameter (PRDO1) from 3ns to 2ns.....209
- (PRU_ICSSG UART Switching Characteristics): Added the TRM UART baud rate settings reference to Note 1.....218
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- (Power Supply Designs): Updated recommended PMIC from LP8733xx to TPS65220 or TPS65219.....243
- (USB VBUS Design Guidelines): Changed the 3.5 kΩ resistor value to 3.48kΩ since 3.5kΩ is not a standard value for 1% resistors.....248
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The datasheet number will be changing.

Device Family	Change From:	Change To:
AM64x	SPRSP56E	**SPRSP56F**

These changes may be reviewed at the datasheet links provided.
http://www.ti.com/product/AM6442

Reason for Change:

To accurately reflect device characteristics.

Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):

No anticipated impact. This is a specification change announcement only. There are no changes to the actual device

Changes to product identification resulting from this PCN:

None.

Product Affected:			
AM6411BKCGHAALV	AM6421BSEFHAALVR	AM6441BSEFGAALV	AM6442BSEFHAALV
AM6411BSCGHAALV	AM6421BSFFHAALV	AM6441BSEFHAALV	AM6442BSEGGAALV
AM6412BKCGHAALVR	AM6421BSFGHAALV	AM6441BSEGHAALVR	AM6442BSEGHAALV
AM6412BSCGHAALV	AM6422BSDFHAALVR	AM6441BSFFHAALV	AM6442BSFFHAALV
AM6421BSDGHAALVR	AM6422BSDGHAALV	AM6442BSDGHAALV	AM6442BSFGHAALV

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