Product Change Notification PCN No: MSS-23-0223-CCB-1112 / MSS-23-1106-CCB-1330

Si55xx/540x New Mold Compound Material and Leadframe surface treatment qualification
Si55xx/540x Datasheet Changes and Updates

Notification Date: 11/10/2023
Qualification Data Availability Date: 07/26/2024
Notification Period: 90 days
Sample Availability Date: 11/10/2023
Proposed First Ship Date for Change: 02/08/2024
Last Date of Manufacture of Unchanged Product: 02/08/2024

Dear Valued Skyworks Customer:
Please be advised that Skyworks Solutions Inc. is introducing the following product change(s):

Description and Scope of Change

Skyworks has qualified Sumitomo A631HT-G mold compound at ASE Chung Li for QFN products requiring a high thermal conductivity bill of materials. Leadframe will change to a roughened copper version. No dimensional or plating changes. Si55xx/540x products assembled in QFN 10x10 mm package will migrate to the new bill of materials.

Datasheet changes are outlined in the revision blocks of the respective documents. Affected Datasheets:

- Si5510/08 Low-Phase-Noise, Jitter-Attenuating Clock for 5G/eCPRI
- Si5512: NetSync™ Low-Phase-Noise, Jitter-Attenuating Clock for 5G/eCPRI/SyncE/IEEE 1588
- Si5518 NetSync™ Low-Phase-Noise Jitter-Attenuating Clock for 5G/eCPRI/SyncE/IEEE 1588
- Si5403, Si5402, and Si5401: NetSync™ Network Synchronizer Clock for 5G, SyncE, and IEEE 1588 Applications

Datasheets attached to PCN letter.

Products Affected

Affected parts defined in the Ordering Guide section of each Datasheet. For the purpose of the PCN letter, these have been consolidated as an addendum.

Method for Identifying Changed Product

Full product change traceability is maintained by: date code

Reason for Change

ASECL is standardizing on Sumitomo A631HT-G for high thermal conductivity mold compound in QFN production.

- Sumitomo is a leading supplier of mold compound for our OSAT base
- Multiple customers are qualifying this material at ASECL
- Material change enhances assurance of supply and lot-to-lot material consistency.

Si55xx/540x datasheet updates encompass content expansions, template modifications, and typo corrections.

Anticipated Impact on Form, Fit Function, Reliability, Durability, Quality or Safety

Impacting form due to mold compound change; no impact to fit, function, realiability, durability, quality or safety.

Qualification Plan Summary

Required package qualification plan has been successfully completed.

Launch Plan

Changes will be implemented at the completion of the PCN effectivity date and upon consumption of existing inventory. Datasheets will be updated in advance of the PCN to allow for customer review of the changes.

Please contact your Skyworks customer service representative with any questions or comments regarding this change. If you are unsure whom to contact, please email Skyworks Change Management at Skyworks.CCB@Skyworksinc.com.

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On the Web: www.skyworksinc.com

Ordering Guides - For Reference

- Si5510/08
- Si5512
- Si5518
- Si5403, Si5402, and Si5401

2. Ordering Guide

Table 1. Si5510/08 Ordering Guide

Ordering Part Number (OPN)[1, 2, 3]	Number of DSPLLs, MultiSynths	Number of Outputs	Serial Interface	Package	Temperature Range
Si5510A-Bxxxxx-GM[4]	1-RFPLL 2-MultiSynths	18	SPI 4-wire or 3-wire	72-Lead QFN 10 x 10 mm	–40 to 95 °C ambient –40 to 105 °C board[5]
Si5510C-Bxxxxx-GM[4]	1-RFPLL 2-MultiSynths	18	I2C	72-Lead QFN 10 x 10 mm	–40 to 95 °C ambient –40 to 105 °C board[5]
Si5510D-Bxxxxx-GM[4]	1-RFPLL 2-MultiSynths	18	I2C	72-Lead QFN 10 x 10 mm	–40 to 95 °C ambient –40 to 105 °C board[5]
Si5510E-Bxxxxx-GM[4]	1-RFPLL 2-MultiSynths	18	SPI 4-wire or 3-wire	72-Lead QFN 10 x 10 mm	–40 to 95 °C ambient –40 to 105 °C board[5]
Si5508A-Bxxxxx-GM[4]	1-RFPLL No-MultiSynths	18	SPI 4-wire or 3-wire	72-Lead QFN 10 x 10 mm	–40 to 95 °C ambient –40 to 105 °C board[5]
Si5508C-Bxxxxx-GM[4]	1-RFPLL No-MultiSynths	18	I2C	72-Lead QFN 10 x 10 mm	–40 to 95 °C ambient –40 to 105 °C board[5]
Si5508D-Bxxxxx-GM[4]	1-RFPLL No-MultiSynths	18	SPI 4-wire or 3-wire	72-Lead QFN 10 x 10 mm	–40 to 95 °C ambient –40 to 105 °C board[5]
Si55xx-A-EVB[6]	—	18	—	Evaluation board	—

1. Add an "R" at the end of the OPN to denote tape and reel ordering options.
2. Custom, factory preprogrammed devices are available. See the figure below for 5-digit numerical sequence nomenclature.
3. Revision B will be the device qualified for mass production and loose samples.
4. Grade D and E are reserved for special applications, see CBPro for details.
5. Si55xx EVB can be configured as either Si5510 or Si5508.
6. Si55xx-A-EVB can be configured as either Si5510 or Si5508.

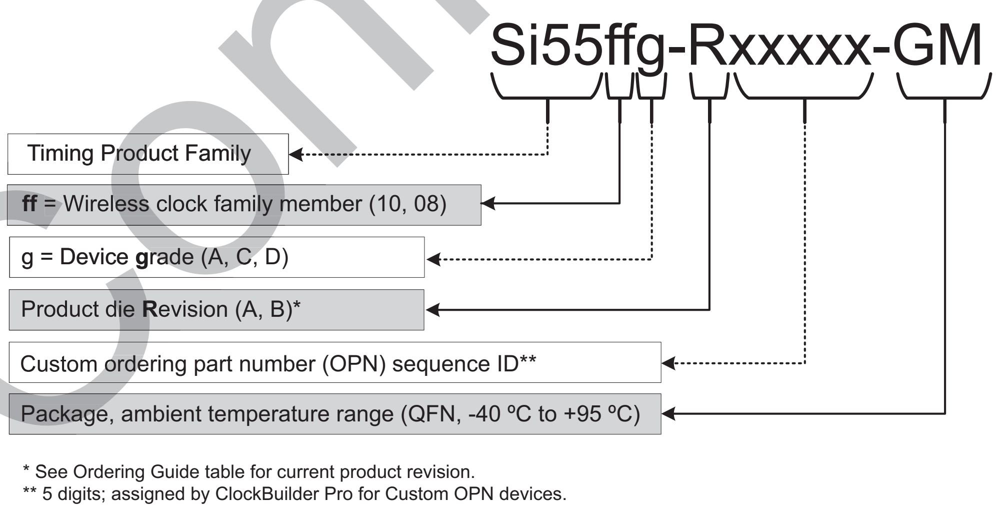

Figure 2. Si5510/08 Ordering Guide Diagram

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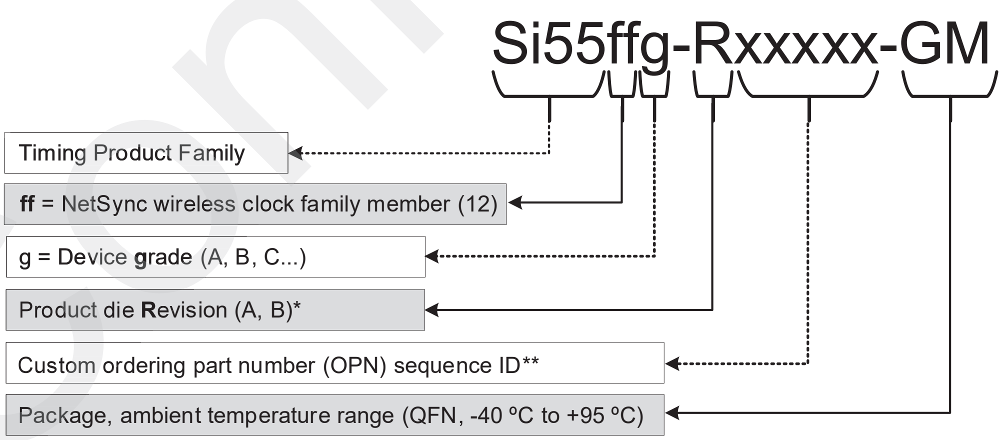
2. Ordering Guide

Table 1. Si5512 Ordering Guide

Ordering Part Number (OPN)[1,2,3]	Number of DSPLLs	Number of Outputs	Serial Interface	AccuTime IEEE 1588 Software Support[4]	Package	Temperature Range
Si5512A-Bxxxxx-GM	1-RFPLL, 2-DSPLL	12	SPI 4–wire or 3–wire	No	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient[5]
Si5512B-Bxxxxx-GM	1-RFPLL, 2-DSPLL	12	SPI 4–wire only	Yes	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient[5]
Si5512C-Bxxxxx-GM	1-RFPLL, 2-DSPLL	12	I^2C	No	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient[5]
Si5512D-Bxxxxx-GM[6]	1-RFPLL, 2-DSPLL	12	SPI 4–wire only	Yes	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient[5]
Si5512E-Bxxxxx-GM[6]	1-RFPLL, 2-DSPLL	12	SPI 4–wire only	Yes	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient[5]
Si5512P-Bxxxxx-GM[6]	1-RFPLL, 2-DSPLL	12	SPI 4–wire or 3–wire	No	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient[5]
Si5512Q-Bxxxxx-GM[6]	1-RFPLL, 2-DSPLL	12	SPI 4–wire or 3–wire	Yes	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient[5]
Si5512R-Bxxxxx-GM[6]	1-RFPLL, 2-DSPLL	12	I^2C	No	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient[5]
Si55xx-A-EVB	1-RFPLL, 2-DSPLL	12	—	No	Evaluation Board	—
Si5518-A-FMC-EVB[7]	—	—	—	Yes	FPGA Mezzanine Card (FMC)	—

1. Add an "R" at the end of the OPN to denote tape and reel ordering options.
2. Custom, factory preprogrammed devices are available as well as unconfigured base devices. See Figure 1 for 5-digit numerical sequence nomenclature.
3. Revision B will be the device qualified for mass production and loose samples.
4. AccuTime IEEE 1588 software is only supported on certain part grades. Use this table to determine which grades support AccuTime.
5. Ambient temperature of 95 °C may not be possible with all configurations. This is dependent on device configuration. Tj cannot exceed a max of 125 °C.
6. Grades D, E, P, Q, and R are reserved for special applications. See ClockBuilder Pro for details.
7. The Si5518-A-FMC ships with 10GBASE-SR SFP+ transceivers, optical cable along with the required software on an SD card. FMC requires a customer-provided AMD ZCU102, ZCU111 or ZCU216 or ZCU670 FPGA evaluation board. FMC is only for AccuTime evaluation. Customers using the Si5512 should use the Si5518-A-FMC to evaluate AccuTime IEEE 1588 software.



* See Ordering Guide table for current product revision.
** 5 digits; assigned by ClockBuilder Pro for Custom OPN devices.

Figure 1. Si5512 Ordering Guide Diagram

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2. Ordering Guide

Table 1. Si5518 Ordering Guide

Ordering Part Number (OPN) [1, 2, 3]	Number of DSPLLs	Number of Outputs	Serial Interface	AccuTime™ IEEE 1588 Software Support [4]	Package	Temperature Range
Si5518A-Bxxxxx-GM	1-RFPLL, PPSPLL, 2-DSPLL	18	SPI 4-wire or 3-wire	No	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient [5] –40 to 105 °C Board
Si5518B-Bxxxxx-GM	1-RFPLL, PPSPLL, 2-DSPLL	18	SPI 4-wire only	Yes	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient [5] –40 to 105 °C Board
Si5518C-Bxxxxx-GM	1-RFPLL, PPSPLL, 2-DSPLL	18	I^2C	No	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient [5] –40 to 105 °C Board
Si5518D-Bxxxxx-GM	1-RFPLL, PPSPLL, 2-DSPLL	18	SPI 4-wire only	Yes	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient [5] –40 to 105 °C Board
Si5518E-Bxxxxx-GM[6]	1-RFPLL, PPSPLL, 2-DSPLL	18	SPI 4-wire only	Yes	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient [5] –40 to 105 °C Board
Si5518F-Bxxxxx-GM [6]	1-RFPLL, PPSPLL, 2-DSPLL	18	SPI 4-wire only	Yes	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient [5] –40 to 105 °C Board
Si5518G-Bxxxxx-GM [6]	1-RFPLL, PPSPLL, 2-DSPLL	18	SPI 4-wire only	Yes	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient [5] –40 to 105 °C Board
Si5518H-Bxxxxx-GM [6]	1-RFPLL, PPSPLL, 2-DSPLL	18	SPI 4-wire only	Yes	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient [5] –40 to 105 °C Board
Si5518I-Bxxxxx-GM [6]	1-RFPLL, PPSPLL, 2-DSPLL	18	SPI 4-wire only	Yes	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient [5] –40 to 105 °C Board
Si5518P-Bxxxxx-GM [6]	1-RFPLL, PPSPLL, 2-DSPLL	18	SPI 4-wire or 3-wire	No	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient [5] –40 to 105 °C Board
Si5518Q-Bxxxxx-GM[6]	1-RFPLL, PPSPLL, 2-DSPLL	18	SPI 4-wire only	Yes	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient [5] –40 to 105 °C Board
Si5518R-Bxxxxx-GM [6]	1-RFPLL, PPSPLL, 2-DSPLL	18	I^2C	No	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient [5] –40 to 105 °C Board
Si55xx-A-EVB	1-RFPLL, PPSPLL, 2-DSPLL	18	—	—	Evaluation Board	—
Si5518-A-FMC-EVB [7]	—	—	—	Yes	FPGA Mezzanine Card (FMC)	—

1. Add an "R" at the end of the OPN to denote tape and reel ordering options.
2. Custom, factory preprogrammed devices are available as well as unconfigured base devices. See the figure below for 5-digit numerical sequence nomenclature.
3. Revision B will be the device qualified for mass production and loose samples.
4. AccuTime IEEE 1588 software is only supported on certain part grades. Use this table to determine which grades support AccuTime.
5. Ambient temperature of 95 °C may not be possible with all configurations. This is dependent on device configuration. Tj cannot exceed a max of 125 °C.
6. Grades D, E, F, G, H, I, P, Q, and R are reserved for special factory use and not for general customer use.
7. The Si5518-A-FMC ships with 10GBASE-SR SFP+ transceivers, optical cable along with the required software on an SD card. FMC requires a customer-provided AMD ZCU102, ZCU111 or ZCU216 FPGA eval board. FMC is only for AccuTime evaluation.

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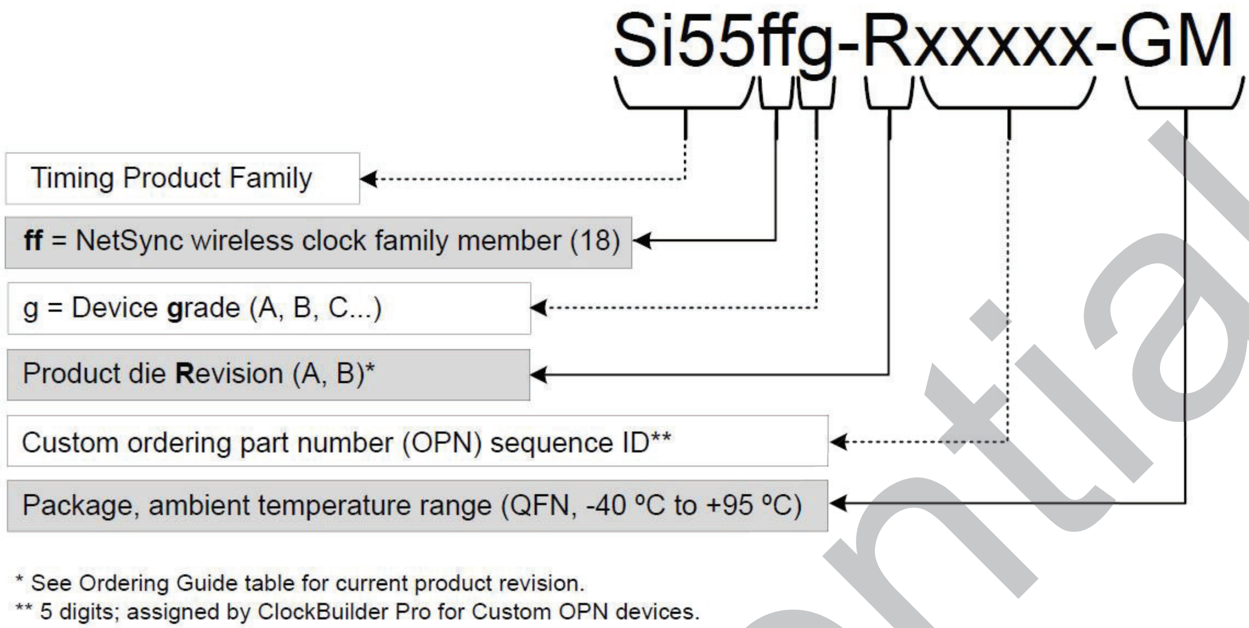

Figure 2. Si5518 Ordering Guide Diagram

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2. Ordering Guide

Table 1. Ordering Guide

Ordering Part Number (OPN)[1,2]	# of PLLs	# of Outputs	Serial Interface	AccuTime™ IEEE 1588 Software Support[3]	Package	Temperature Range
Si5403A-Axxxxx-GM	4 (REFPLL, DSPLL A, DSPLL B and PPSPLL)	18	SPI 4-wire or 3-wire or I^2C	No	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient[4] –40 to 105 °C Board
Si5403B-Axxxxx-GM	4 (REFPLL, DSPLL A, DSPLL B and PPSPLL)	18	SPI 4-wire only or I^2C	Yes	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient[4] –40 to 105 °C Board
Si5403C-Axxxxx-GM[5]	4 (REFPLL, DSPLL A, DSPLL B and PPSPLL)	18	SPI 4-wire only or I^2C	Yes	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient[4] –40 to 105 °C Board
Si5403D-Axxxxx-GM[5]	4 (REFPLL, DSPLL A, DSPLL B and PPSPLL)	18	SPI 4-wire only or I^2C	Yes	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient[4] –40 to 105 °C Board
Si5403E-Axxxxx-GM[5]	4 (REFPLL, DSPLL A, DSPLL B and PPSPLL)	18	SPI 4-wire only or I^2C	Yes	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient[4] –40 to 105 °C Board
Si5403P-Axxxxx-GM[5]	4 (REFPLL, DSPLL A, DSPLL B and PPSPLL)	18	SPI 4-wire or 3-wire or I^2C	No	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient[4] –40 to 105 °C Board
Si5403Q-Axxxxx-GM[5]	4 (REFPLL, DSPLL A, DSPLL B and PPSPLL)	18	SPI 4-wire only or I^2C	Yes	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient[4] –40 to 105 °C Board
Si5402A-Axxxxx-GM[5]	4 (REFPLL, DSPLL A, DSPLL B and PPSPLL)	14	SPI 4-wire only or I^2C	No	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient[4] –40 to 105 °C Board
Si5402B-Axxxxx-GM[5]	4 (REFPLL, DSPLL A, DSPLL B and PPSPLL)	14	SPI 4-wire only or I^2C	Yes	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient[4] –40 to 105 °C Board
Si5402D-Axxxxx-GM[5]	4 (REFPLL, DSPLL A, DSPLL B and PPSPLL)	14	SPI 4-wire only or I^2C	Yes	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient[4] –40 to 105 °C Board
Si5402E-Axxxxx-GM[5]	4 (REFPLL, DSPLL A, DSPLL B and PPSPLL)	14	SPI 4-wire only or I^2C	Yes	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient[4] –40 to 105 °C Board
Si5402P-Axxxxx-GM[5]	4 (REFPLL, DSPLL A, DSPLL B and PPSPLL)	14	SPI 4-wire only or I^2C	No	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient[4] –40 to 105 °C Board
Si5402Q-Axxxxx-GM[5]	4 (REFPLL, DSPLL A, DSPLL B and PPSPLL)	14	SPI 4-wire only or I^2C	Yes	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient[4] –40 to 105 °C Board
Si5401A-Axxxxx-GM[5]	3 (REFPLL, DSPLL A and PPSPLL)	10	SPI 4-wire only or I^2C	No	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient[4] –40 to 105 °C Board
Si5401B-Axxxxx-GM[5]	3 (REFPLL, DSPLL A and PPSPLL)	10	SPI 4-wire only or I^2C	Yes	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient[4] –40 to 105 °C Board
Si5401D-Axxxxx-GM[5]	3 (REFPLL, DSPLL A and PPSPLL)	10	SPI 4-wire only or I^2C	Yes	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient[4] –40 to 105 °C Board
Si5401E-Axxxxx-GM[5]	3 (REFPLL, DSPLL A and PPSPLL)	10	SPI 4-wire only or I^2C	Yes	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient[4] –40 to 105 °C Board
Si5401P-Axxxxx-GM[5]	3 (REFPLL, DSPLL A and PPSPLL)	10	SPI 4-wire only or I^2C	No	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient[4] –40 to 105 °C Board
Si5401Q-Axxxxx-GM[5]	3 (REFPLL, DSPLL A and PPSPLL)	10	SPI 4-wire only or I^2C	Yes	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient[4] –40 to 105 °C Board
Si540X-A-EVB	4 (REFPLL, DSPLL A, DSPLL B and PPSPLL)	18	—	No	Evaluation Board	
Si5403-A-FMC-EVB[6]	—	—	—	Yes	FPGA Mezzanine Card (FMC)	

1. Add an R at the end of the OPN to denote tape and reel ordering options.
2. Custom, factory preprogrammed devices are available as well as unconfigured base devices. See the figure below for 5-digit numerical sequence nomenclature.
3. AccuTime IEEE 1588 software is only supported on certain part grades. Use this table to determine which grades support AccuTime.
4. Ambient temperature of 95 °C may not be possible with all configurations. This is dependent on device configuration. Tj cannot exceed a maximum of 125 °C.
5. Grades C, D, E, P, and Q are reserved for special applications. See ClockBuilder Pro for details.
6. The Si5403-A-FMC-EVB ships with 10GBASE-SR SFP+ transceivers, optical cable along with the required software on an SD card. FMC requires a customer-provided AMD ZCU102, ZCU111, or ZCU216 FPGA eval board. FMC is only for AccuTime evaluation.

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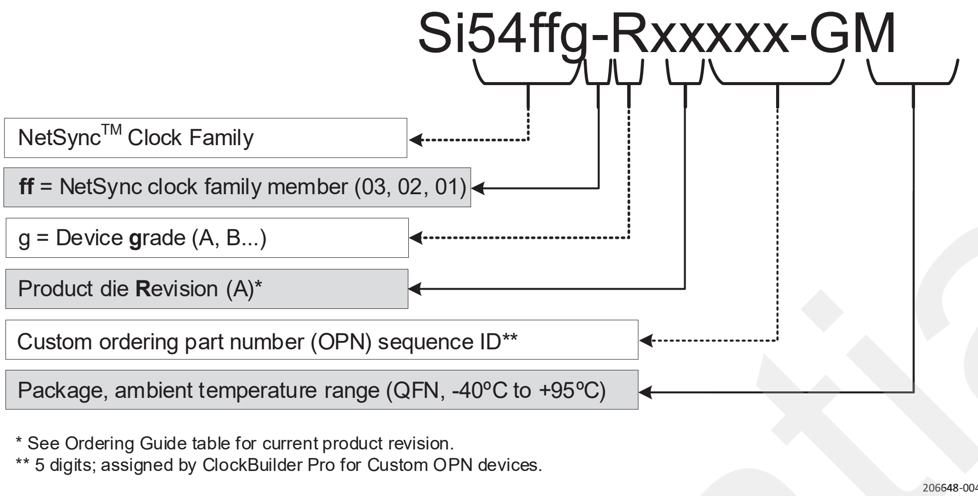

Figure 4. Ordering Guide

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Datasheets

- Si5510/08 Low-Phase-Noise, Jitter-Attenuating Clock for 5G/eCPRI
- Si5512: NetSync™ Low-Phase-Noise, Jitter-Attenuating Clock for 5G/eCPRI/SyncE/IEEE 1588
- Si5518 NetSync™ Low-Phase-Noise Jitter-Attenuating Clock for 5G/eCPRI/SyncE/IEEE 1588
- Si5403, Si5402, and Si5401: NetSync™ Network Synchronizer Clock for 5G, SyncE, and IEEE 1588 Applications

DATA SHEET

Si5510/08 Low-Phase-Noise, Jitter-Attenuating Clock for 5G/eCPRI

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The Si5510/08 are low-noise, high-performance wireless jitter-attenuating clocks with any-frequency outputs for eCPRI (ethernet-based Common Public Radio Interface) applications. The Si5510/08 are based on Skyworks fifth-generation DSPLL® technology, which combines frequency synthesis and jitter attenuation in a highly integrated digital solution with a cost-effective oscillator without the need for any external loop filter components.

A fixed frequency oscillator (XO or XTAL) provides a phase noise reference and frequency stability for free-run and holdover modes. A VCXO option is available for applications demanding the highest level of phase noise performance.

The RFPLL generates high performance low phase noise CPRI clocks for wireless remote radio heads (RRH). Each of the 18 clock outputs are configurable in any combination of high-performance JESD204B/C DCLK and SYSREF clock pairs, or other system clocks through the integer Q dividers. The RFPLL is a fully featured phase-locked-loop with adjustable DCO capability.

In addition to the RFPLL, the Si5510 integrates two low-noise MultiSynth™ fractional dividers. Any of the 18 clock outputs can be derived from either of the two MultiSynths.

Applications

- LTE-A and 5G Remote Radio Units (RRU) or Active Antenna Units (AAU)
- JESD204B/C clock generation
- Remote Access Networks (RAN), picocells, small cells
- Remote Radio Heads (RRH), wireless repeaters, mobile fronthaul and backhaul

Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to *Skyworks Definition of Green™*, document number SQ04–0074.

Key Points

- Utilizes fifth-generation DSPLL® and MultiSynth™ technologies
- Ultra high-performance clock generation for LTE-A and 5G RRUs
- Integer output frequencies up to 3.2 GHz
- Fractional output frequencies up to 650 MHz
- JESD204B/C clock generation (DCLK/ SYSREF) with synchronization across multiple devices
- Programmable delay at each output
- Ultra-low jitter: 47 fs RMS typical
- Low-power mode
- Phase Noise:
  - Noise floor –164 dBc/Hz at 491.52 MHz
  - –145 dBc/Hz at 800 kHz offset for a 491.52 MHz carrier frequency
- Spurs < –95 dBc at 122.88 MHz
- Supports DCO adjustable at 1 ppt resolution
- Full suite of status monitors

Block Diagram

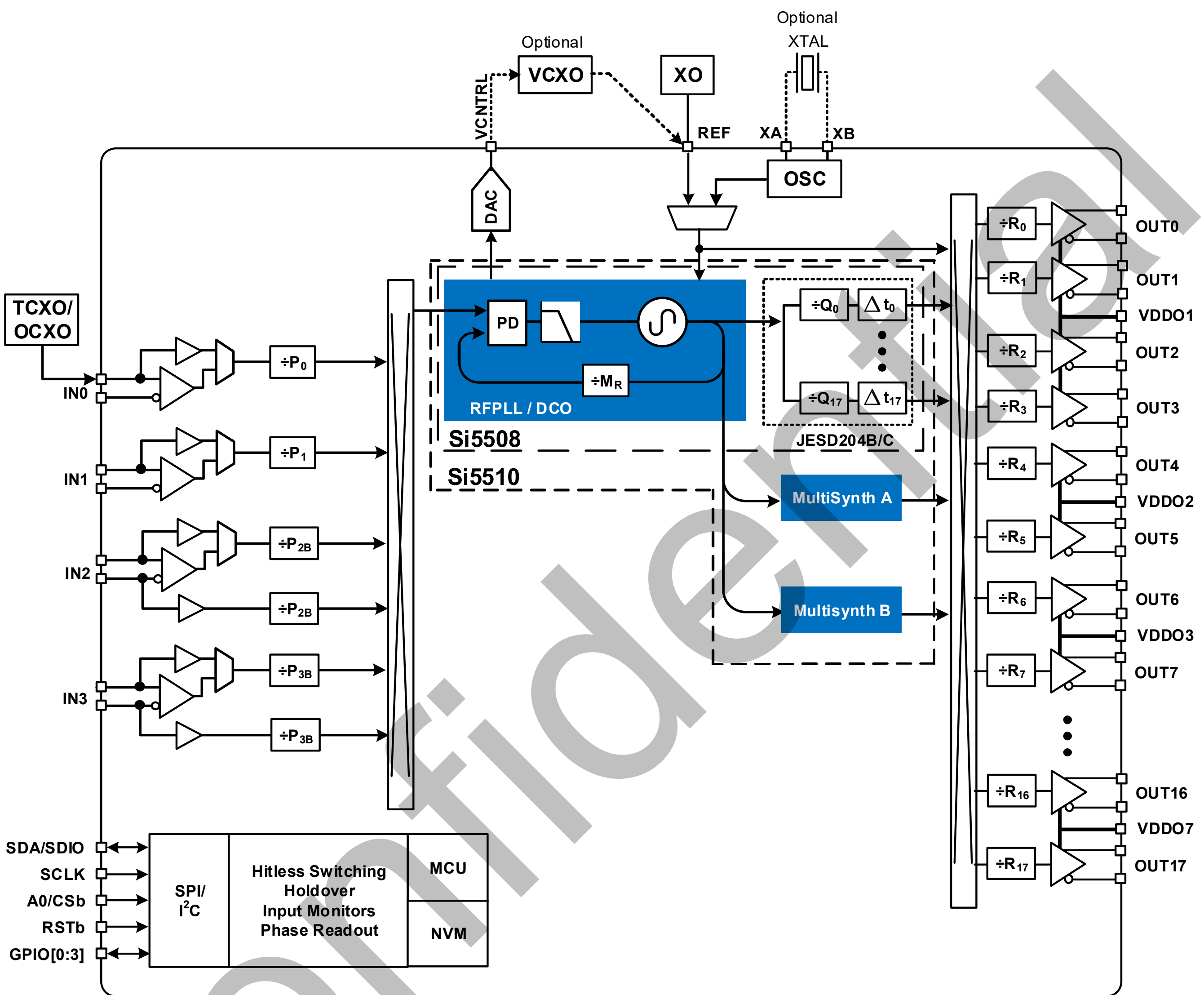

Figure 1. Si5510/08 Block Diagram

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1. Feature List

- RFPLL
  - Supports JESD204B/C Subclass 0, 1, and 2 Clocking
  - Ultra-low Phase Noise (example at 491.52 MHz carrier):
    - –164 dBc/Hz noise floor
    - –145 dBc/Hz at 800 kHz offset
- Ultra-low jitter performance:
  - <50 fs typ XO (12 kHz to 20 MHz at 491.52 MHz)
  - <45 fs typ VCXO (12 kHz to 20 MHz at 491.52 MHz)
- Selectable jitter attenuation bandwidth: 10 Hz to 400 Hz
- Automatic Free-Run, Holdover, and Locked modes
- Hitless input clock switching: automatic or manual with < 150 ps phase transient
- 18 Programmable Clock Outputs:
  - JESD204B/C DCLK or SYSREF. Up to nine DCLK/SYSREF pairs
  - Integer Q dividers: PP2S/1PPS to 3.2 GHz
  - JESD204B/C SYSREF pulser mode
  - MultiSynth Fractional Dividers: PP2S/1PPS to 650 MHz
  - Output-to-Output Static Delay: ±10 ns
  - Output-output skew: ±50 ps
  - LVDS, S-LVDS, ac-coupled LVPECL, LVCMOS, slew rate limited (SRL) LVCMOS, HCSL, CML
- Utilizes fifth-generation DSPLL® and MultiSynth technologies
- Zero Delay Mode
- 4/6 clock inputs:
  - Differential: 8 kHz to 1 GHz
  - CMOS: 8 kHz to 250 MHz
- Status monitoring (LOS, OOF, PHMON, FLOL and PLOL)
- Automatically generates free-running clocks at power up
- Automatically locks to a valid clock input
- Automatic holdover mode
- Core voltage: 3.3 V, 1.8 V
- Output driver supply voltages (VDDO): 3.3 V, 2.5 V, 1.8 V
- Serial Interface: I2C or SPI (3 or 4-wire)
- ClockBuilder® Pro (CBPro™) software tool simplifies device configuration
- Package: 72-Lead QFN, 10 x 10 mm
- Extended temperature range:
  - –40 to +95 °C ambient
  - –40 to +105 °C board
- Pb-free, RoHS compliant

Note: Specifications on this page are for reference only. Refer to Section 4. Electrical Specifications for device performance.

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2. Ordering Guide

Table 1. Si5510/08 Ordering Guide

Ordering Part Number (OPN)[1, 2, 3]	Number of DSPLLs, MultiSynths	Number of Outputs	Serial Interface	Package	Temperature Range
Si5510A-Bxxxxx-GM[4]	1-RFPLL 2-MultiSynths	18	SPI 4-wire or 3-wire	72-Lead QFN 10 x 10 mm	–40 to 95 °C ambient –40 to 105 °C board[5]
Si5510C-Bxxxxx-GM[4]	1-RFPLL 2-MultiSynths	18	I2C	72-Lead QFN 10 x 10 mm	–40 to 95 °C ambient –40 to 105 °C board[5]
Si5510D-Bxxxxx-GM[4]	1-RFPLL 2-MultiSynths	18	I2C	72-Lead QFN 10 x 10 mm	–40 to 95 °C ambient –40 to 105 °C board[5]
Si5510E-Bxxxxx-GM[4]	1-RFPLL 2-MultiSynths	18	SPI 4-wire or 3-wire	72-Lead QFN 10 x 10 mm	–40 to 95 °C ambient –40 to 105 °C board[5]
Si5508A-Bxxxxx-GM[4]	1-RFPLL No-MultiSynths	18	SPI 4-wire or 3-wire	72-Lead QFN 10 x 10 mm	–40 to 95 °C ambient –40 to 105 °C board[5]
Si5508C-Bxxxxx-GM[4]	1-RFPLL No-MultiSynths	18	I2C	72-Lead QFN 10 x 10 mm	–40 to 95 °C ambient –40 to 105 °C board[5]
Si5508D-Bxxxxx-GM[4]	1-RFPLL No-MultiSynths	18	SPI 4-wire or 3-wire	72-Lead QFN 10 x 10 mm	–40 to 95 °C ambient –40 to 105 °C board[5]
Si55xx-A-EVB[6]	—	18	—	Evaluation board	—

1. Add an “R” at the end of the OPN to denote tape and reel ordering options.
2. Custom, factory preprogrammed devices are available. See the figure below for 5-digit numerical sequence nomenclature.
3. Revision B will be the device qualified for mass production and loose samples.
4. Grade D and E are reserved for special applications, see CBPro for details.
5. Si55xx EVB can be configured as either Si5510 or Si5508.
6. Si55xx-A-EVB can be configured as either Si5510 or Si5508.

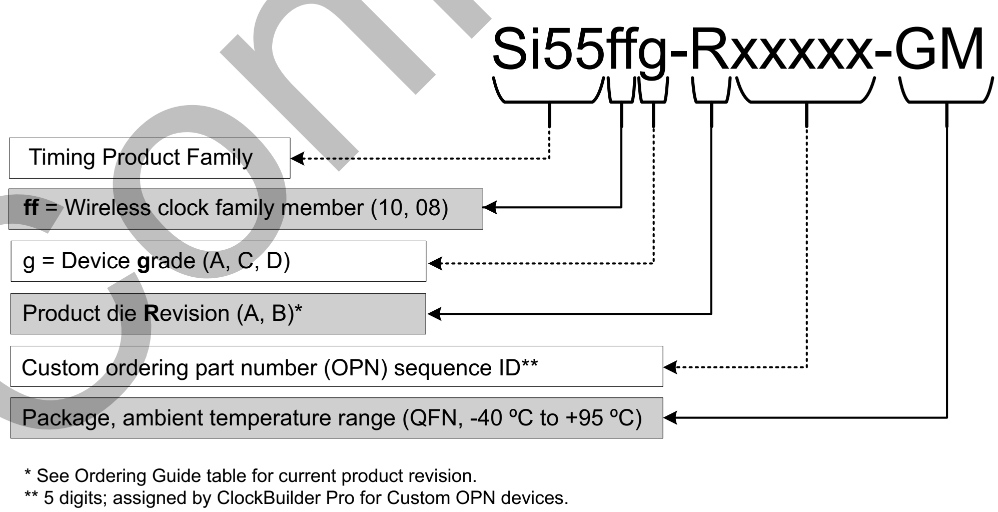

Figure 2. Si5510/08 Ordering Guide Diagram

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3. Functional Description

The Si5510/08 are high-performance JESD204B/C compatible RF clock jitter attenuators incorporating a fifth-generation RFPLL, with low noise Q-Divider outputs or up to two low-noise MultiSynths that generate integer or fractionally related output frequencies. These devices have integrated programmable loop filters and on-chip LDOs that provide excellent supply noise rejection requiring only a few external components. The RFPLL can operate from an external VCXO, XO or fixed frequency crystal (XTAL), known as single reference mode. The RFPLL supports Locked, Free-Run, and Holdover modes of operation with an optional DCO mode. There are four differential or six single-ended inputs available to the RFPLL. Two of the inputs (IN2, IN3) can be configured as dual single-ended inputs in applications where more than four inputs are required. Input selection can be manual or automatically controlled using an internal state machine. Any of the 18 output clocks (OUT0 to OUT17) can be sourced from any of the output dividers using a flexible crosspoint connection.

3.1. Frequency Configuration

The frequency configuration of the RFPLL is programmable through the serial interface and can also be stored in non-volatile memory. The combination of input dividers (P), fractional frequency multiplication (M), integer output division (Q), fractional output division (N), and integer output division (R) allows the generation of virtually any output frequency on any of the outputs. All divider values for a specific frequency plan are automatically calculated using the CBPro™ utility.

3.2. RFPLL Loop Bandwidth, Initial Lock, and Fast Lock Settings

The RFPLL loop bandwidth determines the amount of input clock jitter attenuation. The RFPLL will always remain stable with low peaking regardless of the loop bandwidth selection.

The RFPLL has configurable loop bandwidths. There are three configurations; each has a separate setting for the loop bandwidth:

- **Initial Lock Bandwidth:** The PLL uses this bandwidth when it exits Free-Run Mode and attempts to lock to a new input clock.
- **Loop Bandwidth:** This sets the bandwidth of the PLL once lock to an input is achieved.
- **Fastlock Bandwidth:** This sets the bandwidth of the PLL when exiting from holdover.

Selecting a low RFPLL loop bandwidth will generally lengthen the lock acquisition time. The Fastlock feature allows setting of a temporary Fastlock Loop Bandwidth that is used during the lock acquisition process. The RFPLL will revert to its normal loop bandwidth once lock acquisition has completed.

See the Si5518/12/10/08 Reference Manual and CBPro for more information, recommendations, and limits for setting PLL loop bandwidths for different configurations.

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3.3. Inputs

There are four differential inputs which can also be configured as single-ended CMOS inputs. Both IN0 and IN1 can support a single CMOS input, while IN2 and IN3 can be configured as dual CMOS inputs. This allows support for up to 6 CMOS inputs, or any combination of differential and CMOS inputs.

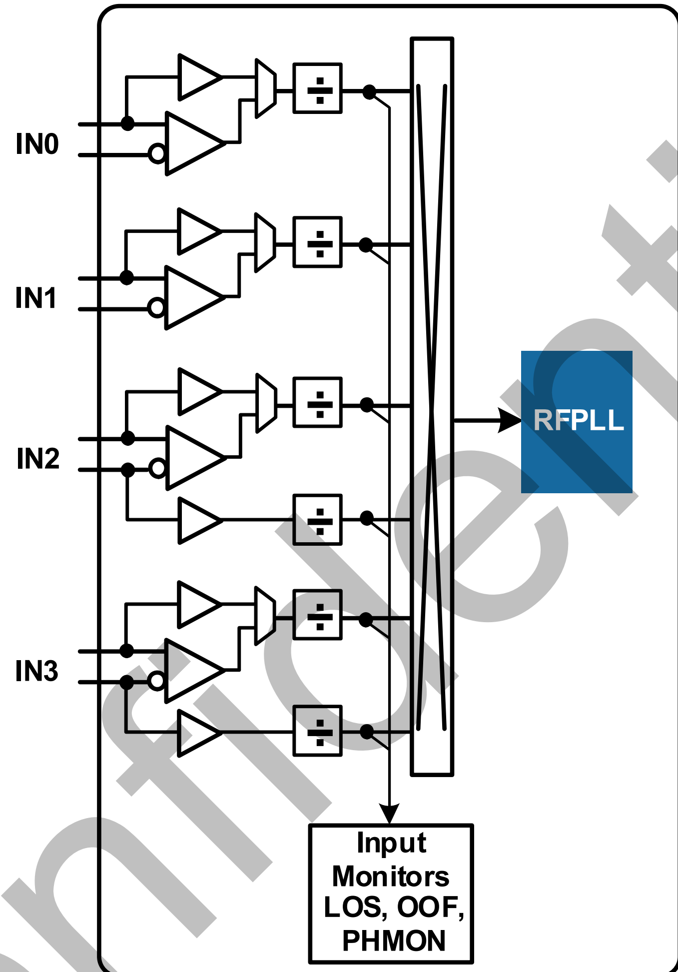

Figure 3. Input Structure

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3.3.1. Input Terminations

Refer to AN1293: Si55xx Schematic Design and Board Layout Guidelines and the Si5518/12/10/08 Reference Manual for guidance on input terminations.

3.3.2. Input Selection

Input selection of the RFPLL can be controlled manually through pin control, API command, CLI command, or automatically using an internal state machine.

3.3.2.1. Input Divider

The device utilizes both fractional and integer input (P) dividers to lock to any frequency input clock. The CBPro software chooses the optimum divide values based on the user-defined frequency plan. Each input divider (P0, P1, P2, P2b, P3, and P3b) can be configured independently of the others.

3.3.2.2. Manual Input Selection

In manual mode, the input selection is made by defining a GPIO pin as an input select pin and changing the input pin voltage level, or by writing an API or CLI command. Any of the inputs are available to the RFPLL through a crosspoint input selection switch. If there is no clock signal on the selected input, or if the input is not valid due to LOS/OOF/PHMON input alarms, the RFPLL will automatically enter Free-Run/Holdover Mode.

3.3.2.3. Automatic Input Selection

When configured in this mode, the RFPLL automatically selects a valid input that has the highest configured priority. The priority scheme is independently configurable and supports revertive or non-revertive selection. All inputs are continuously monitored for loss of signal (LOS), invalid frequency range (OOF), and phase (PHMON). Only valid inputs that have no LOS, OOF or phase monitor (PHMON) alarms can be selected by the automatic state machine. The RFPLL will enter Free-Run or Holdover Mode if there are no valid inputs available.

3.3.3. Unused Inputs

Unused inputs should be configured as “Unused (Powered Down)” and the pins may be left unconnected or ac-coupled to ground. See AN1293: Si55xx Schematic Design and Board Layout Guidelines and the Si5518/12/10/08 Reference Manual for recommendations on how to minimize system noise on any CMOS input and or any differential input configured as “Enabled” but not actively being driven by a clock.

3.3.4. Phase Readout (PHRD)

The phase readout Device API command can be used to measure the phase difference between different input clocks to the Si5510/08. Unused inputs that are not assigned to the RFPLL can also be configured as phase readout (PHRD) or phase readout feedback (PHRD_FB) inputs. These inputs can be used to measure the phase of an output of the Si5510/08 to the input(s) of known phase. PHRD and PHRD_FB inputs use the same alarms, such as LOS/OOF/PHMON, as the other clock inputs, but they are not assigned to the PLL.

3.4. Input Clock Switching

Clock inputs applied to the Si5510/08 can be either from the same source (0 ppm, same nominal frequency) or different sources (non-0 ppm, different nominal frequencies). The Si5510/08 automatically determines the optimal switching mode depending on the nominal frequency difference between the clocks at the time of the switch. When switching between 0 ppm inputs, the Si5510/08 performs either a hitless switch with phase buildout (PBO) or a phase pull-in (PPI) switch depending on the user selection in CBPro. When the input clocks have a non-0 ppm offset, the Si5510/08 performs a frequency-ramped input switch.

Refer to the Si5518/12/10/08 Reference Manual for additional guidance on input clock switching modes. All input clock switches are glitchless, which means that no runt pulses are generated at the output during the transition.

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3.4.1. Hitless Input Switching for 0 ppm Clocks-Phase Buildout (PBO)

Applications like eCPRI require that transients are kept to a minimum when switching between input clocks. Hitless switching with phase buildout (PBO) is a feature that prevents a transient from propagating to the output when switching between two clock inputs that have a fixed phase relationship. A hitless switch can only occur when the two input frequencies are frequency locked, meaning that the nominal frequencies are the same (0 ppm). Due to the nature of hitless switching, the input-to-output delay of the RFPLL is not preserved. The RFPLL simply absorbs the phase difference between the two input clocks during an input switch.

3.4.2. Phase Pull-In (PPI) Input Switching for 0 ppm Clocks

In some applications, such as traditional CPRI fronthaul clocking, the output phase must track the input phase with minimal delay. When the application requires the input-to-output delay to be preserved after clock switching, the phase pull-in clock switching mode should be selected. In this mode, the output phase will be pulled in at a user-programmable ramp rate referred to as the PPI slope (ns/s). With phase pull-in switching, the output phase always aligns with the newly selected input. PPI is always enabled for zero-delay mode applications.

3.4.3. Ramped Input Switching for Non-0 ppm Clocks

The ramped switching feature allows the RFPLL to switch between two input clock frequencies that have a non-0ppm offset without an abrupt frequency transient at the output. When the two input clock frequencies are not the same nominal frequency, the RFPLL will pull in the frequency difference between inputs at the ramp rate that is programmable in CBPro from ppb/s to ppm/s. The loss-of-lock (LOL) and LOOP_FILTER_RAMP_IN_PROGRESS indicators (accessible through the Device API) will assert while the RFPLL is ramping to the new clock frequency.

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3.5. Outputs

The Si5510/08 supports 18 differential output drivers configurable as AC Coupled LVPECL, LVDS, S-LVDS, CML, HCSL, LVCMOS, or SRL LVCMOS. When in LVCMOS mode, the differential pair becomes two single-ended outputs for a maximum of 36 possible outputs. Two of the output drivers (OUT16 and OUT17) have slew rate control when in LVCMOS mode. This allows limiting the rise time of the output signal to reduce the possibility of crosstalk to adjacent output drivers. The outputs have power supply pins (VDDOx) for output driver groups of 4-2-2-2-2-4-2, which can be individually powered by 3.3, 2.5, or 1.8 V. The LVCMOS output voltage is set by the VDDOx pin. Refer to Table 18, Pin Descriptions.

3.5.1. Output Crosspoint

A crosspoint allows any of the output drivers to connect with its associated Q divider or either of the MultiSynths. A digital output delay adjustment is possible on each of the Q divider outputs for JESD204B/C applications. The static delay adjustments are programmable and may be stored in NVM so that the desired output configuration is ready at power up.

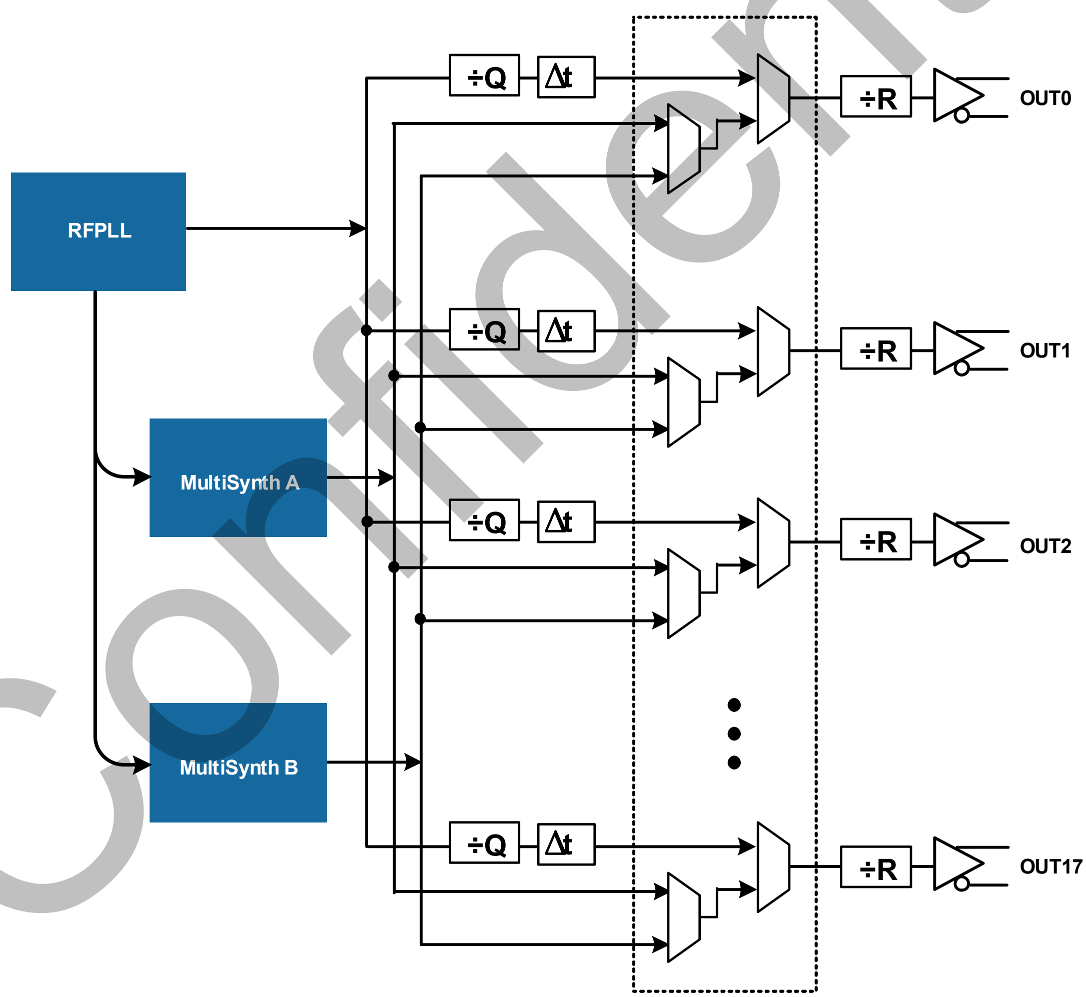

Figure 4. Output Structure

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3.5.2. Differential and LVCMOS Output Terminations

Refer to AN1293: Si55xx Schematic Design and Board Layout Guidelines and the Si5518/12/10/08 Reference Manual for guidance on output terminations.

3.5.3. Slew Rate Limited (SRL) LVCMOS Outputs

The swing of LVCMOS and SRL LVCMOS outputs is rail-to-rail; so, the swing is determined by the voltage of the corresponding VDDO pin of the LVCMOS or SRL LVCMOS output. Each output driver configured as LVCMOS or SRL LVCMOS has two outputs, OUTx/OUTxb. The polarity of each of the two outputs may be independently configured as a noninverted or inverted output as well as enabled or disabled.

OUT16/16b and OUT17/17b may be configured as SRL LVCMOS outputs, which have a selectable slew rate and generate significantly less crosstalk than conventional LVCMOS outputs, which is useful in jitter-critical applications.

SRL LVCMOS output clocks on OUT16/16b and OUT17/17b are intended only for low frequency clock applications. Refer to the Si5518/12/10/08 Reference Manual for the maximum Fout supported for each slew rate selection.

3.5.4. Output Enable/Disable

Each output driver may be enabled/disabled through programmable GPIO pins. There are two output enable groups, OE0 and OE1, which are logically OR'ed together to determine which outputs are enabled at any point in time. CBPro allows the control and selection of the GPIO pin mapping to the outputs.

Outputs may also be enabled/disabled using the device API. If an output is assigned as GPIO controlled, it cannot be controlled via the API. The API controlled output enable allows for more flexibility than the GPIO control as any of the outputs can be individually enabled/disabled via an API command.

The default output enable/disable behavior is a glitchless enable/disable. For clocks to start or stop as soon as possible, accepting runt pulses or glitches, instant output enable/disable can be used.

3.5.5. State of Disabled Output

The disabled state of an output driver may be configured as stop high, stop low, or Hi-Z. CMOS outputs <2 MHz can also be configured as Hi-Z with weak pullup/down.

Differential outputs, when disabled, will maintain the output common-mode voltage even while the output is not toggling. This minimizes disturbances when disabling and enabling clock outputs.

3.5.6. Output Dividers

The device utilizes both integer Q dividers and fractional NA, NB MultiSynth output dividers. The ClockBuilder Pro software chooses the optimal divide values based on the user-defined frequency plan.

A summary of each class of divider is listed below:

1. Output Q Divider: Q0-Q17
   - Integer Only Divide Value
2. Output N Divider: NA, NB
   - MultiSynth Divider, Integer or Fractional Divide Value

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3. Output Divider: R17-R0
- Integer Only Divide Value

3.5.7. Output Skew Control

Output skew control allows outputs that are derived from the Q dividers to be phase adjusted in steps of 1/fvco or 1/(4*fvco) when the fine adjust is enabled. The exact skew adjustment and step sizes are reported on the Output Skew Control Tab of the CBPro Wizard.

3.5.8. Output Synchronization (OSYNC)

The OSYNC input is used to align the phases of the integer Q divider output clocks to a SYNC input signal from a logic device (ASIC/FPGA) or a data converter. OSYNC can be used to achieve deterministic latency in a JESD204B/C Subclass 2 application. When asserted, the Q divider outputs will stop low glitch-free. When OSYNC is de-asserted, the first transition of all outputs will be aligned to the OSYNC signal within the data sheet delay from OSYNC de-asserted to output reenabled specification. OSYNC must be assigned to GPIO2.

OSYNC can also be used to align the phases of the Q divider output clocks between multiple Si5510/08 devices to a SYNC input signal. To achieve the chip-to-chip data sheet specification for output skew, the input clock to the Si5510/08 must be a CPRI frequency (N*1.92 MHz) and integer-related to the Q divider outputs.

OSYNC can also be initiated through an API command instead of a GPIO input; however, the OSYNC de-asserted to output reenabled specification cannot be guaranteed. The API command should not be used for multichip OSYNC.

3.6. RFPLL

The RFPLL controls the central VCO which provides many of the essential functions for the device such as generating ultra-low phase noise JESD204B/C clocks and maintaining free-run accuracy and holdover stability. It operates using one of many external frequency sources. A simple low-cost fixed frequency crystal (XTAL) provides the phase noise reference and the RFPLL locks to a clock input for jitter attenuation. Options of using a crystal oscillator (XO) or a voltage-controlled crystal oscillator (VCXO) are also available. The benefits and trade-offs of the phase noise reference are covered in the Si5518/12/10/08 Reference Manual and CBPro.

3.6.1. JESD204B/C Clock Generation

The RFPLL generates ultra-low phase noise JESD204B/C clocks for Subclass 0, Subclass 1, and Subclass 2 operation. Any of the 18 clock outputs can be assigned to generate JESD204B/C output clocks.

JESD204B/C Subclass 0 and Subclass 2 support is provided through the OSYNC input assignable to GPIO2.

JESD204B/C Subclass 1 support is provided with assignable SYSREF/DCLK timing skew, as well as with a SYSREF pulser that supports JESD204B/C "gapped" periodic outputs.

Static delay is assignable with a step size down to 1/4*VCO period (approximately 20 ps). Exact delay is reported in CBPro.

Each SYSREF output can be configured in continuous mode. SYSREFS in continuous mode may cause crosstalk with adjacent DCLK outputs. If using SYSREF in continuous mode a gap of one unused output is recommended between SYSREF and DCLK.

The SYSREFs can also be configured in pulsed mode. The SYSREF pulser provides 1, 2, 4, 8, 16, or 32 pulses on user request, with the SYSREF held static between requests. SYSREFs in pulsed mode will not couple with other channels since for the majority of operation they are disabled. A gap or unused output between DCLK and SYSREF is

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not necessary in pulsed mode. Each SYSREF can be independently assigned as Continuous or Pulsed mode with desired number of pulses in CBPro. A common SYSREF pulse request for all pulsed SYSREF outputs can be initiated either by a rising edge on assignable digital input SRCREQ, or by using the JESD_SYSREF_PULSER API via the serial interface.

3.7. DCO Mode

The RFPLL DCO can be frequency controlled in pre-defined steps ranging from <1 ppt to several ppm. The DCO can be controlled when the RFPLL is locked to an external clock or when it is in Free-Run/Holdover mode. The frequency adjustments are controlled through the serial interface by triggering a Device API command or by pin control using frequency increments (FINC) or decrements (FDEC). Both the FINC and FDEC pins are available through the configurable GPIO pins. A FINC will add the frequency step word to the PLL output frequency, while a FDEC will decrement it. Step sizes are configured in CBPro.

3.8. Zero Delay Mode (ZDM)

Zero delay mode (ZDM) is a mode of operation in which more accurate input-to-output phase delay can be achieved on the RFPLL by providing an external feedback from one of the clock outputs to one of the clock inputs. For more details on implementing ZDM, see AN1293: Si55xx Schematic Design and Board Layout Guidelines and the Si5518/12/10/08 Reference Manual.

3.9. External Reference Clocks (XA/XB, REF_IN)

The Si5510/08 operates from either an external crystal oscillator (XO) connected to the REF_IN pins or with an optional fixed-frequency crystal (XTAL) connected to the XA, XB pins. The internal oscillator (OSC) combined with a low cost external XTAL produces an ultra-low jitter reference clock for the RFPLL. When using an external XO, it's important to select one that meets the jitter performance requirements of the end application. Alternatively, the device can operate with an external voltage-controlled crystal oscillator (VCXO). Operating the device with only an XO or XTAL, or with only a VCXO is referred to as single reference mode, as shown in Figure 5, “Single Reference Mode,” on page 13. The low phase noise reference XO/VCXO or XTAL is connected to REF_IN or XA/XB.

The Si5510/08 can also be configured in a dual reference clock generator mode where a TCXO or OCXO provides improved frequency stability. In this case, the RFPLL locks to a TCXO or OCXO that is applied to one of the inputs. This mode is referred to as dual reference clock generator mode since the output frequencies track the TCXO or OCXO frequency. It is possible to DCO the RFPLL in dual reference clock generator mode. This configuration is shown in Figure 6, “Dual Reference Clock Generator Mode,” on page 14. The low phase noise reference XO/VCXO or XTAL is connected to REF_IN or XA/XB as described above.

Use CBPro to configure the device in either single reference mode or dual reference clock generator mode.

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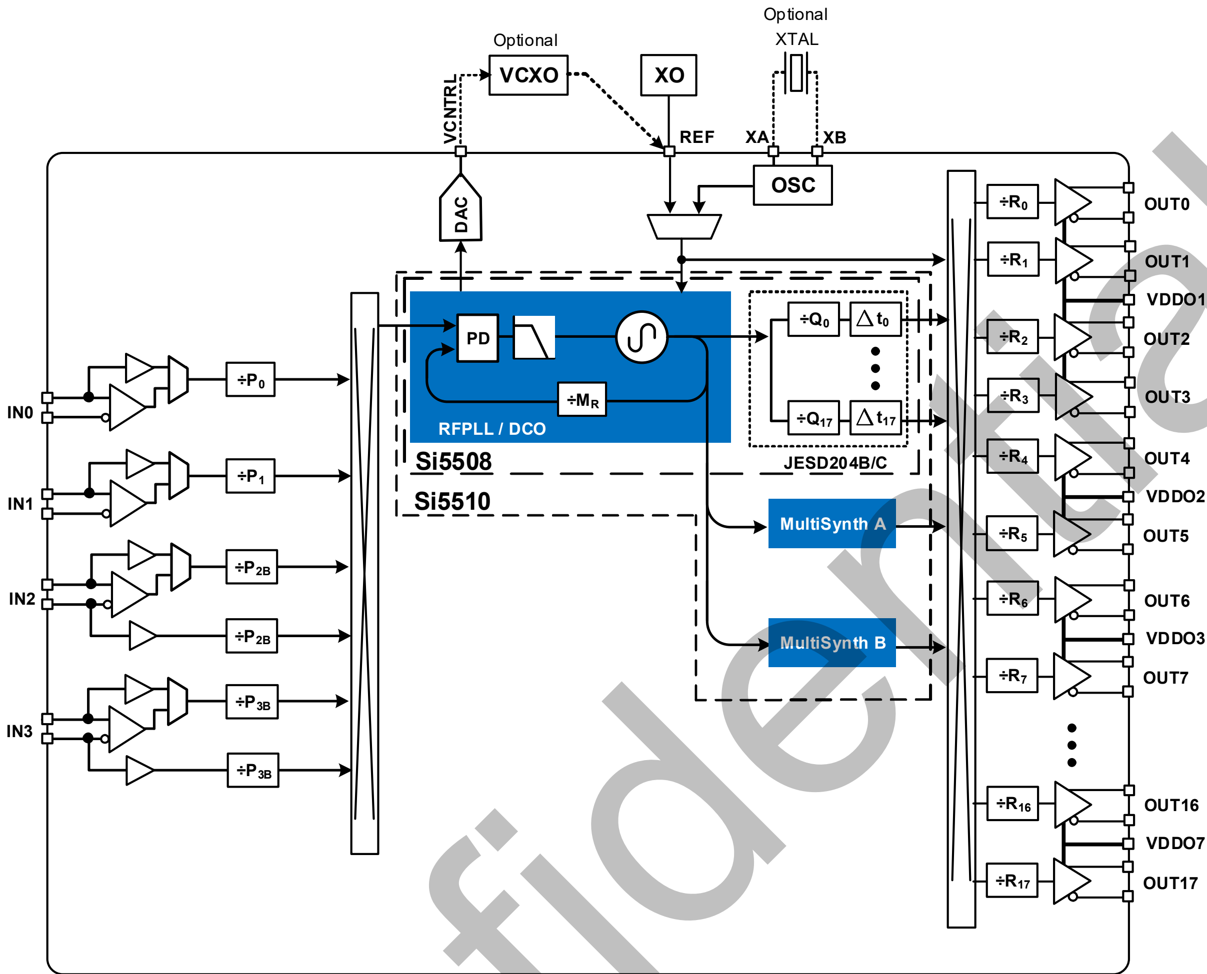

Figure 5. Single Reference Mode

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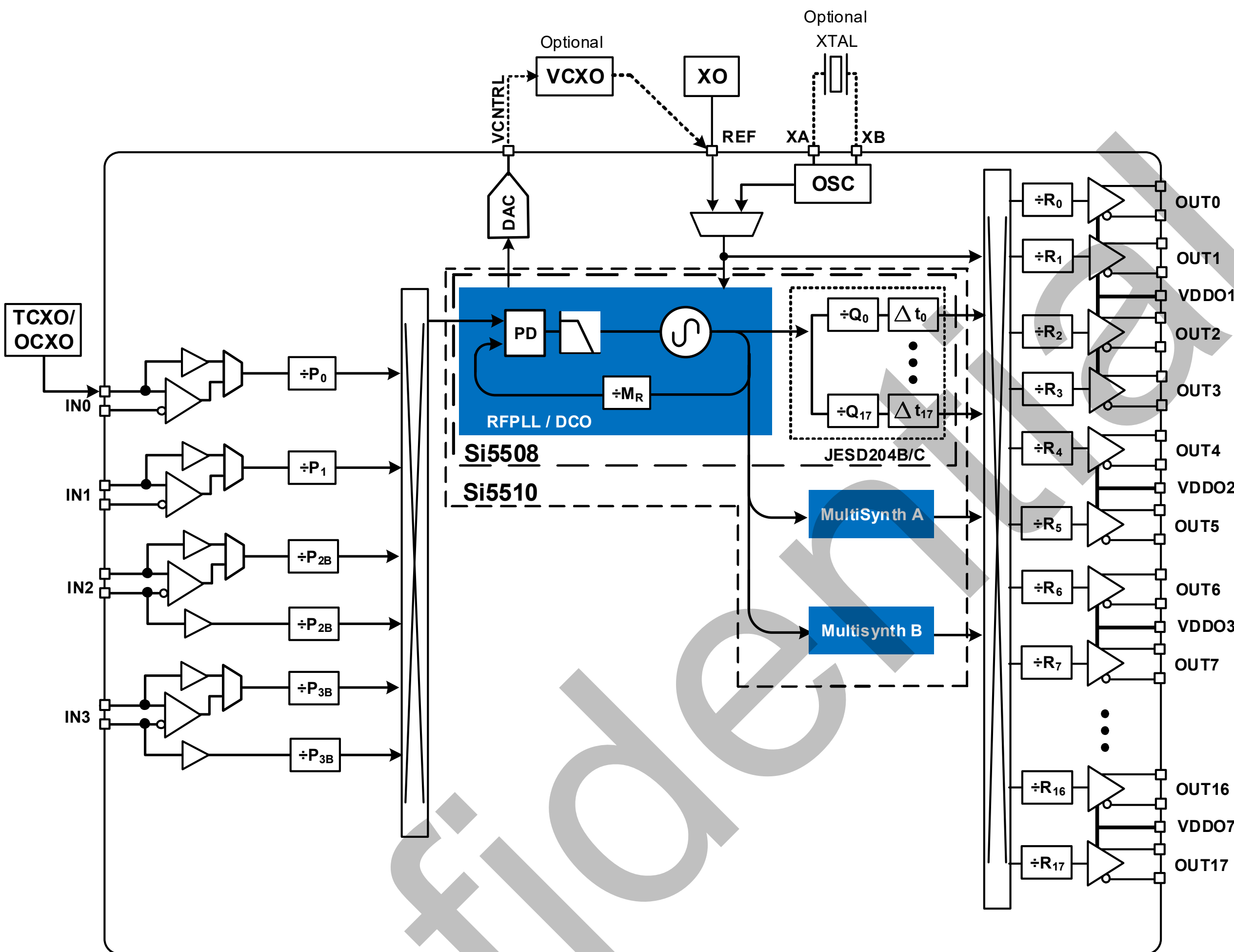

Figure 6. Dual Reference Clock Generator Mode

3.9.1. XA, XB Inputs

The XA/XB inputs are used to provide a fixed frequency reference for the RFPLL. The device includes internal XTAL loading capacitors which eliminate the need for external capacitors and also has the benefit of reduced noise coupling from external sources. A crystal in the range of 48 to 54 MHz is recommended for best jitter performance.

3.9.2. REF_IN Input

An alternative to using an external XTAL is to connect a crystal oscillator (XO) directly to the REF_IN Input. Another option is using an external voltage controlled crystal oscillator (VCXO). In VCXO mode, the RFPLL produces an analog control voltage which adjusts the VCXO's output frequency. This mode is useful when generating specific integer related output frequencies such as in wireless applications (e.g., 4G/LTE, 5G). The REF_IN inputs accommodate both single-ended CMOS as well as differential XOs/VCXOs. See the Si55xx, Si540x, and Si536x Recommended XTAL, XO, VCXO, TCXO, and OCXO Reference Manual for more information.

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3.9.3. VCXO Buffer Output

When the REF_IN input is a VCXO, there is a VCXO buffer output available that can be used to achieve the lowest midband phase noise (10 kHz to 1 MHz). This is often critical for high-end applications, such as mmWave. The VCXO buffer output tracks the phase and frequency of the input clock just as any of the other Si5510/08 outputs. However, since the VCO and Q dividers are bypassed, the buffer output frequency must equal the frequency of the VCXO. All of the remaining outputs and RFPLL are still available when using buffer output. The buffer output can be assigned to any of the outputs via the output crosspoint mux. The buffer output is not available when using an XO or XTAL.

3.10. GPIO Pins (General Purpose Input or Output)

There are four GPIO pins which have programmable functions. They can be assigned as either an input or an output from one of the functions shown in the table below. OUT6/11 can be repurposed as GPIs when they are not being used as clock outputs.

The GPIs are programmable as either active high or active low via ClockBuilder Pro. Active low GPIs are indicated by adding a "b" at the end of the function name for example “OEb” as displayed in ClockBuilder Pro. All GPI pins have a weak pull-up (PU) or pull-down (PD) resistor to set a default state when not externally driven. The default state of the GPI is always de-asserted except for OEx, which is, by default, asserted to enable the outputs. The internal resistance of the PU/PD resistor is 20 kΩ typical.

GPIO selectable status outputs (GPO) are push-pull and do not require any external pull-up or pull-down resistors.

Table 2. GPIO Pin Descriptions

Function	Description
GPIO Selectable Control Inputs (GPI)	
FINC	DCO frequency increment
FDEC	DCO frequency decrement
PLLR_FORCE_HO	Force holdover for RFPLL
PLLR_INSEL[0-2]	Input select pins for RFPLL. There are 3 bits to select from 1 of 6 inputs.
IN[0:5]_FAIL	Force input invalid. A low on this pin indicates to the automatic switching state machine that the associated input is not valid for selection. This is useful in applications that use their own input monitoring.
OE0–OE1	Output enable for specific outputs or group of outputs as defined by the grouping assigned in CBPro.
SRCREQ	JESD204B/C SYSREF pulse request
OSYNC	Synchronizes all or a subset of output dividers identified as PPS or SYSCLK in CBPro. **Assignable to GPIO2 only.
GPIO Selectable Status Outputs (GPO)	
PLLR_LOL	Loss of lock for RFPLL.
PLLR_HO	This pin indicates when RFPLL has entered the holdover state.
INx_LOS	Loss of signal status indicator for INx.
INx_OOF	Out of frequency status indicator for INx
REF_OOF	Out of frequency status indicator of the reference

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Table 2. GPIO Pin Descriptions (Continued)

Function	Description
REF_LOS	Loss of signal at XA/XB and REF pins
INTR	Interrupt pin for the device. Programmable Boolean combination of PLLR_LOL, INx_LOS, INx_OOF, PLLR_HO, REF_LOS, REF_OOF.
Primary Serial Interface (I2C/SPI)	
A1/SDO	A1/SDO of primary SPI port. **Assignable to GPIO3 only.
A0/CSb	A0/CSb of primary SPI port
SDA/SDIO	SDA/SDIO of primary SPI port
SCLK	SCLK of primary SPI port

3.11. Device Initialization and Reset

Once power is applied and RSTb is de-asserted, the device begins loading preconfigured register values and configuration data from NVM, and performs other initialization tasks. Communicating with the device through the serial interface is possible once this initialization period is complete (see tRDY). No output clocks will be generated until the initialization is complete, and the device locks to the external (VC)XO/XTAL (see tSTART_XO and tSTART_XTAL). A reset, initiated using the RSTb pin or through the Device API RESTART command, restores all registers to the values stored in NVM, and all circuits, including the serial interface, will be restored to their initial state. All clocks will stop during a hard reset. Other feature-specific resets are also available. See the Si5518/12/10/08 Reference Manual and AN1360: Serial Communications and API Programming Guide for Si536x, Si540x, and Si55xx Devices for more information on different methods of resetting the device.

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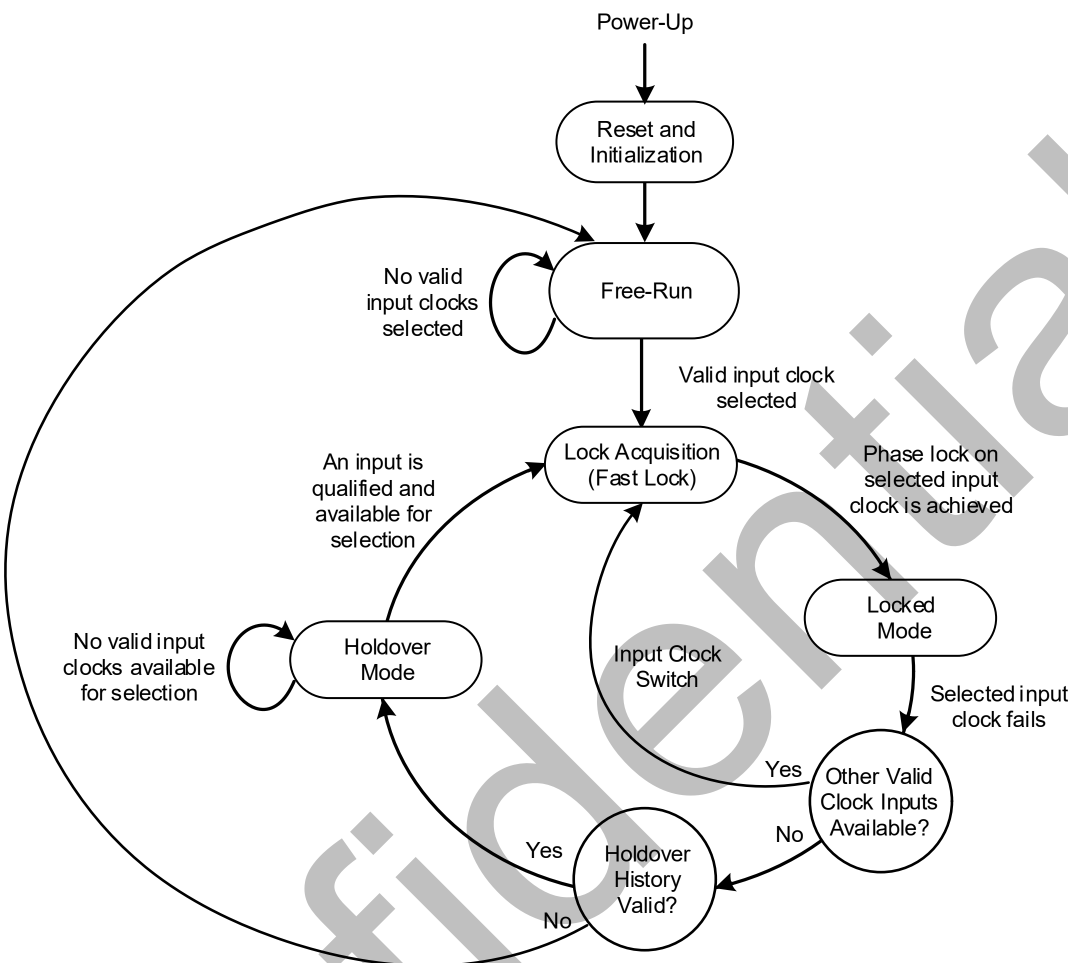

Figure 7. Modes of Operation

3.12. Modes of Operation

Once initialization is complete the RFPLL independently operates in one of four modes: Free-Run, Lock Acquisition, Locked, or Holdover. A state diagram showing the modes of operation is shown in the above figure. The following sections describe each of these modes in greater detail.

3.12.1. Free-Run Mode

The RFPLL will automatically enter Free-Run Mode once power is applied to the device and initialization is complete. In this mode, the frequency accuracy of the generated output clocks is entirely dependent on the frequency accuracy of the reference clock source. If a XTAL is connected to the XA/XB pins, then the clock outputs will generate a frequency at the XTAL's accuracy. For example, if a XTAL is operating at -28 ppm then clock outputs will also be -28 ppm. The same is true if a XO is connected at the REF_IN inputs instead of using XTAL at XA/XB. The frequency stability of the outputs will also be determined by the XTAL or XO.

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When a TCXO or OCXO is connected to the RFPLL inputs, then the frequency accuracy and stability of the outputs will be determined by the TCXO or OCXO. This is recommended for applications that need better accuracy and stability than what the XTAL or XO can provide.

3.12.2. Lock Acquisition Mode

The RFPLL independently monitors its configured inputs for a valid clock. If at least one valid clock is available for synchronization, the RFPLL will automatically start the lock acquisition process. If the fast lock feature is enabled, it will acquire lock faster than the RFPLL Loop Bandwidth would provide and then transition to the normal RFPLL loop bandwidth. During lock acquisition the outputs will generate a clock that follows the VCO frequency change as it pulls-in to the input clock frequency.

The Device API command reports the lock status of the RFPLL. When the RFPLL output frequency is within the threshold defined on the Frequency LOL (FLOL) page in CBPro, the PLL_OUT_OF_FREQUENCY bit de-asserts. Some time after that, the RFPLL will pull in the remaining phase defined on the Phase LOL (PLOL) page in CBPro. Once the RFPLL is frequency and phase locked, the PLL_LOSS_OF_LOCK (LOL) bit de-asserts, and the RFPLL enters locked mode.

3.12.3. Locked Mode

Once locked, the RFPLL will generate clock outputs that are both frequency and phase locked to their selected input clocks. Any frequency changes (e.g., because of temperature variations) of the reference clock (REF_IN) within the PLL loop bandwidth will be corrected by the loop ensuring 0 ppm lock to its input clock (IN). Any frequency changes of the reference clock (REF_IN) beyond the PLL loop bandwidth will pass through to the clock output.

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3.12.4. Holdover Mode

The RFPLL will automatically enter Holdover Mode when the selected input clock becomes invalid, holdover history is valid, and no other valid input clocks are available for selection. The RFPLL uses an averaged input clock frequency as its final holdover frequency to minimize the disturbance of the output clock phase and frequency when an input clock suddenly fails. The holdover circuit for the RFPLL stores historical frequency data while locked to a valid input clock. The final averaged holdover frequency value is calculated from a programmable window within the stored historical frequency data. Both the window size and delay are programmable as shown in the figure below. The window size determines the amount of holdover frequency averaging. The delay value allows ignoring frequency data that may be corrupt just before the input clock failure.

The maximum window size is a function of input frequency and is reported in CBPro the RFPLL. For higher frequency inputs up to 5000 seconds of holdover history can be stored. See CBPro for more information on this setting.

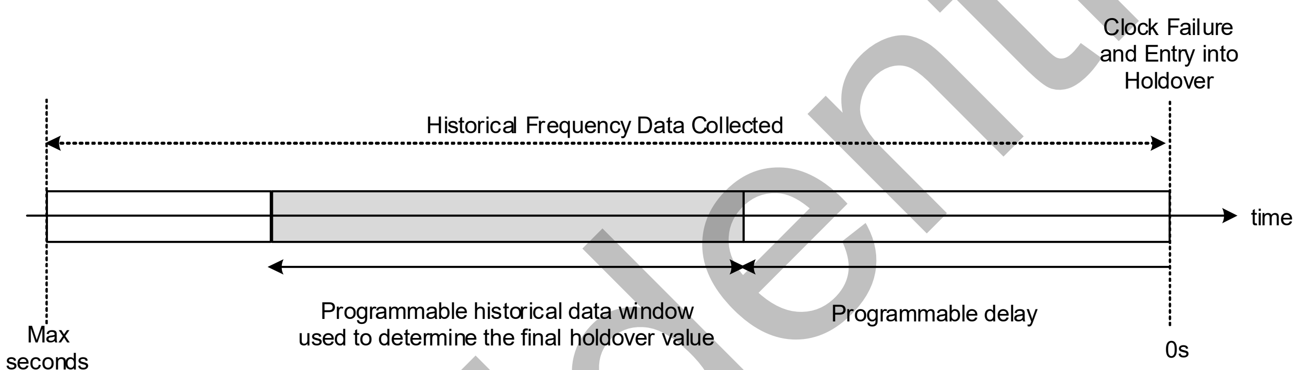

Figure 8. Programmable Holdover Window

When entering holdover, the RFPLL will pull its output clock frequency to the calculated averaged holdover frequency. While in holdover, the output frequency drift is entirely dependent on the external reference clock connected to the REF_IN input and, if an OCXO/TCXO holdover reference is used, also dependent on the holdover reference. If the input clock becomes valid, the RFPLL will automatically exit the holdover mode and re-acquire lock to the new input clock. This process involves pulling the output clock frequency to achieve frequency and phase lock with the input clock. This pull-in process is glitchless.

The RFPLL output frequency when exiting holdover can be ramped. Just before the exit is initiated, the difference between the current holdover frequency and the new desired frequency is measured. Using the calculated difference and a user-selectable ramp rate, the output is linearly ramped to the new frequency. The RFPLL loop BW does not limit or affect ramp rate selections (and vice versa). CBPro defaults to ramped exit from holdover and free-run. The ramp rate settings are configurable for initial lock (exit from freerun), exit from holdover, and clock switching.

If ramped holdover exit is disabled, the holdover exit is governed either by (1) the RFPLL loop BW or (2) the RFPLL Fastlock bandwidth, when enabled.

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3.13. Status and Alarms

The Si5510/08 monitors the input clocks and reference input for status and alarms. The status and alarms provide the internal state machine with real-time phase and frequency monitoring used for making decisions, such as switching inputs or entering holdover.

3.13.1. Input Clock Status

All input clocks are continuously monitored for faults using the Loss-of-Signal (LOS), Out-of-Frequency (OOF), and Phase Monitor (PHMON) alarms. When a differential input is configured as a dual CMOS input, then each CMOS input is independently monitored. Any enabled alarms for an input, such as LOS/OOF/PHMON, are logically ORed together to produce the input invalid alarm.

Any input clock with an alarm is not valid until all alarms are cleared. If RFPLL is locked to an input clock and that input clock becomes invalid, then the RFPLL may either switch to a valid input or enter holdover mode, depending on how the device is programmed.

API commands can be used to indicate if an alarm is valid, pending short term fault, under validation or invalid.

3.13.1.1. Loss of Signal (LOS)

The loss of signal alarm measures the period of each input clock cycle to detect phase irregularities or missing clock edges. Each of the input LOS circuits has its own programmable sensitivity, which allows missing edges or intermittent errors to be ignored. Loss of signal sensitivity is configurable using the CBPro utility. The LOS status for each of the monitors is accessible by checking the INPUT_STATUS API.

3.13.1.2. Out of Frequency (OOF) Detection

All inputs are monitored for frequency accuracy with respect to an OOF reference which is selected in Clock-Builder Pro. The OOF reference can be selected as either the XO/XTAL/VCXO or the OCXO/TCXO in dual reference mode. When available it is recommended to select the OCXO/TCXO as the OOF reference since it will have a tighter frequency accuracy compared to a free-running XTAL or a VCXO.

The OOF set and clear thresholds must be wider than the combined frequency accuracy of the OOF reference plus the stability of the input clock. A valid input clock frequency is one that remains within the OOF frequency range which is configurable from ±0.1 ppm to±500 ppm in steps of 0.1 ppm. A configurable amount of hysteresis is also available to prevent the OOF status from toggling at the failure boundary. An example is shown in the figure below. In this case, the OOF monitor is configured with a valid frequency range of ±15 ppm with 5 ppm of hysteresis. This OOF configuration will support a dual reference mode with a Stratum 3 level OCXO/TCXO and a SyncE input which both have ±4.6 ppm overall frequency accuracy.

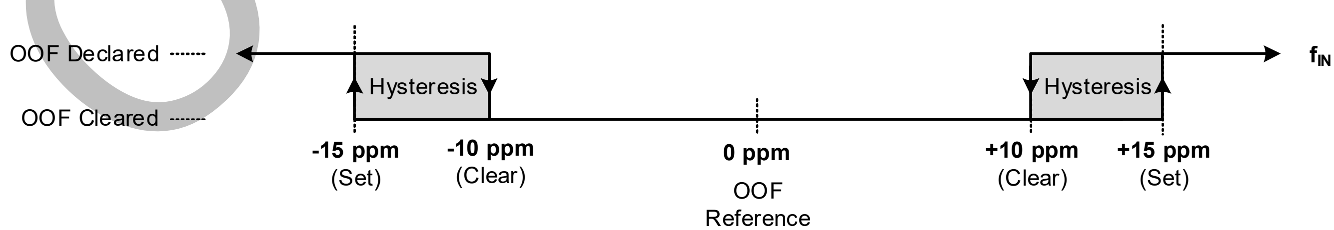

Figure 9. Example of Precise OOF Monitoring Assertion and De-assertion Triggers

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3.13.1.3. Phase Monitor (PHMON)

If a clock input undergoes a phase transient, a PLL locked to that input will filter the transient by its loop bandwidth; however, the transient will propagate to the output. Transients that propagate to the output have the potential to negatively impact downstream devices.

Phase Monitor (PHMON) alarm monitors the input clock phase or accumulated phase, and, if the input transient exceeds the programmable threshold, the PHMON alarm will be asserted. PHMON, like the other alarms, is quick to be asserted when the thresholds are violated yet slower to be de-asserted to prevent chattering around the threshold.

Each input clock has an independent PHMON alarm. Each alarm can be enabled/disabled individually, and its associated threshold may be independently configured. Note that OOF must be enabled and properly configured for PHMON to operate.

A ZDM input may use the PHMON alarm for monitoring purposes. However, it will have no effect on PLL bandwidth selection and will not cause input switching.

3.13.1.4. Short Term Holdover

The Short-Term Holdover (STHO) feature may be used when the input clock is expected to have a short-term fault and then quickly recover.

If an input clock has STHO enabled, and an LOS/OOF/PHMON alarm is asserted, then a PLL locked to that input will enter holdover and wait for a programmable duration until all alarms on the input clock are de-asserted.

If all alarms on the input clock are de-asserted before the programmable amount of time has passed, then the PLL will gracefully relock to the same input clock. If all the alarms on the input clock are not de-asserted before the programmable amount of time has passed, then the PLL will either switch to the next priority input clock or remain in holdover, depending on the input clock selection settings.

If STHO is disabled, then the PLL will skip the short-term holdover time and immediately switch to the next priority input clock or enter holdover, depending on the input clock selection settings.

STHO may be programmed using ClockBuilder Pro to set the duration or to enable or disable the feature for each input clock individually. Note that the STHO setting will affect all PLLs assigned to that input.

3.13.2. RFPLL Status

The RFPLL is continuously monitored for Loss-of-Lock (LOL). The final LOL status indicator is the logical OR of the Frequency Loss-of-Lock and Phase Loss-of-Lock statuses. See the Si5518/12/10/08 Reference Manual for more information.

3.13.2.1. Loss of Lock (LOL)

There is a loss of lock (LOL) monitor for the RFPLL. The LOL monitor asserts when the RFPLL has lost synchronization with its selected input clock. Any of the GPIOs can be programmed as a dedicated loss-of-lock pin that reflects the loss-of-lock condition for the RFPLL. The LOL monitor measures both the frequency and phase difference between the input and feedback clocks of the phase detector. The frequency monitor gives frequency lock detection (FLOL) while the phase monitor indicates true phase lock PLOL by detecting one or more single slips. Both the phase and frequency LOL monitors have clear and set thresholds and a timer to prevent LOL assertion from tog-

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gling or chattering as the RFPLL completes lock acquisition. The cycle slip detector also has configurable sensitivity.

3.13.2.2. Frequency Loss of Lock (FLOL)

The Frequency Loss-of-Lock (FLOL) monitor measures the frequency difference between the input clock and the feedback clock. The upper and lower LOL thresholds are programmable, which dictates when the alarm will be asserted or de-asserted. It is recommended to program the clear threshold to be less than the set threshold to allow for hysteresis in the FLOL set/clear behavior. This prevents the FLOL alarm from chattering or causing multiple interrupts. FLOL, like the other alarms, is quick to be asserted when the threshold is violated yet slower to be de-asserted. The alarm validates that the frequency difference between the input and feedback clocks has truly settled to within the LOL clear threshold before the FLOL alarm is de-asserted. The time required to validate the frequency difference increases as the loop bandwidth of the PLL decreases.

3.13.2.3. Lock Status Bits

There are four lock status bits that serve as four additional Frequency LOL thresholds. The Status Bit (STB) is asserted if the frequency difference between the input clock and feedback clock exceeds the programmable STB threshold. The assertion or de-assertion of an STB does not contribute to the FLOL or LOL status. The lock status bits may be read via the API. In the lock acquisition process, the de-assertion of a STB does not indicate that the PLL is frequency locked. This is because the frequency may chatter around the STB threshold. On the other hand, the de-assertion of FLOL requires the frequency difference to truly settle below the LOL clear threshold.

3.13.2.4. Phase Loss of Lock (PLOL)

The Phase Loss-of-Lock (PLOL) alarm measures the phase difference between the input clock and feedback clock. The PLOL set threshold is programmable so the alarm will assert or de-assert depending on phase difference between the input and feedback clocks relative to the threshold setting. It is recommended to set the clear threshold below the set threshold to allow for hysteresis. This prevents the alarm from chattering or causing multiple interrupts. During the lock acquisition process, the input clock and feedback clock will likely have a significant frequency mismatch; so, the PLOL is not asserted until FLOL is de-asserted. Once FLOL has been de-asserted, the two frequencies are stable with respect to each other. Then the feedback clock phase can be pulled in to within the PLOL clear threshold.

3.13.2.5. Cycle Slip Detection

The RFPLL may be monitored for cycle slips. Like the PLOL alarm, cycle slip detection is not enabled until FLOL is de-asserted. Additionally, PLOL must be enabled for cycle slip detection to be enabled. Cycle slips both in the positive and negative direction are monitored. The API can be used to read the total count of positive cycle slips, negative cycle slips and the total count or both positive and negative slips.

3.13.3. External Reference Status

An external reference must always be provided to the device. The Si5510/08 will monitor the external reference input for LOS, OOF, and LOL. If a fault is detected on the external reference, then the outputs will be disabled. Any external reference faults may be read via the API.

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3.13.4. Interrupt Status

The interrupt flag is asserted when any of the status indicators of the device changes state. The interrupt status may be assigned a GPIO pin, or it may be checked using an API command to show which status indicator caused the interrupt to be asserted.

The Interrupt Configuration page in CBPro lists all the status indicators that can be programmed to activate the interrupt pin.

The status indicators that are enabled are logically OR'd together so that the assertion of any of these status indicators will cause the interrupt pin to assert. The interrupt pin status depends on the sticky versions of the individual status indicators, so the interrupt pin will stay asserted until the sticky status indicators are cleared.

3.14. Serial Interface

Configuration and operation of the Si5510/08 is controlled by reading and writing API commands using the I2C or SPI interface. The SPI mode operates in either 4-wire or 3-wire modes. The following tables define the GPIO pins assigned to the SPI interface.

Table 3. Primary Serial Interface Pins

Pin Number	3-Wire SPI	4-Wire SPI	I^2C
55	CSb	CSb	A0
52	SDIO	SDI	SDA
53	SCLK	SCLK	SCK
56	Unused	SDO	A1

3.15. NVM Programming

At power-up, the device loads its default configuration and settings from internal non-volatile memory (NVM). The NVM can be preprogrammed at the factory with a custom frequency plan such that the device starts generating clocks on its first power-up, or the NVM can be programmed in the field using the API command set. NVM programming in the field must be done with VDDA set to 3.3V. NVM programming in the field is not supported in Low-Power mode. For more details on NVM programming options, refer to Si5518/12/10/08 Reference Manual and AN1360: Serial Communications and API Programming Guide for Si536x, Si540x, and Si55xx Devices.

3.16. Application Programming Interface (API)

Communication between the customer's host processor and the Si5510/08 internal microcontroller (MCU) is accomplished through the serial interface. The Si5510/08 MCU contains firmware that allows users to have command-level access to the device API. Internal registers are not accessible through the API because all features of the Si5510/08 can be accessed through the Device API. The primary serial port (SPI or I2C) allows programming of the Si5510/08, and the secondary serial port (SPI 3-wire only) is intended for Phase Readback and status monitoring operations. See the Si5518/12/10/08 Reference Manual for more information and examples of the API. Details of the API commands are available through ClockBuilder Pro. For instructions on using the Device API and for

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instructions on programming the clock device, see AN1360: Serial Communications and API Programming Guide for Si536x, Si540x, and Si55xx Devices.

3.17. Power Supplies

The Si5510/08 has 14 power supply pins. The separate power supplies are used for different functions, providing power locally where it is needed on the die to improve isolation. When no outputs are enabled for a particular VDDOx, that supply pin may be left unconnected. Please refer to the AN1293 Si55xx Schematic Design and Board Layout Guide for more details on power management and filtering recommendations.

3.17.1. Power Supply Sequencing

There are no power sequencing requirements between supplies. VDDA and VDD18 should be powered up before releasing RSTb. VDDA must be equal to the highest voltage supply.

3.17.2. Power Supply Ramp Rate

Power supply ramp times must stay within the maximum supply voltage ramp rate as defined in Table 7 on page 28.

3.17.3. Low Power Mode

In Low-Power Mode, the analog core supply voltage (VDDA) of the Si5510/08 is set to 1.8 V in order to reduce power consumption. Since VDDA must be equal to the highest voltage applied to the Si5510/08, in Low-Power Mode, all voltage supplies including VDDO must be 1.8 V. A 1.8 V VDDO restricts the output format to S-LVDS, LVCMOS, or HCSL. If LVPECL or LVDS output format is required, Low-Power Mode cannot be used. NVM programming in the field is not supported in Low-Power Mode since NVM programming requires VDDA to be 3.3 V. Additionally the VCXO mode is not supported in Low-Power Mode. Please refer to AN1293 Si55xx Schematic Design and Board Layout Guide Confidential for VDDREF and XO/XTAL connections and terminations for Low-Power Mode.

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4. Electrical Specifications

All minimum and maximum specifications in the following tables are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise noted.

Table 4. Absolute Maximum Ratings[1, 2, 3, 4]

Parameter	Symbol	Test Condition	Value	Unit
DC supply voltage	V_{DDIN}		–0.5 to 3.8	V
	V_{DDREF}		–0.5 to 3.8	V
	V_{DD18}		–0.5 to 2.4	V
	V_{DDA}		–0.5 to 3.8	V
	V_{DDO}		–0.5 to 3.8	V
	V_{DDIO}		–0.5 to 3.8	V
Input voltage range	V_{I1}	REF_IN/REF_INb, INx/INxb	–0.85 to 3.8	V
	V_{I2}	GPIO0-3, RSTb, SCLK, SDA/SDIO, A0/CSb	–0.5 to 3.8	V
	V_{I3}	XA/XB	–0.5 to 2.7	V
Latch-up tolerance	LU		JESD78 compliant	
ESD tolerance	HBM	100 pF, 1.5 kΩ	2.0	kV
Storage range	TSTG		–55 to 150	°C
Maximum junction temperature in operation	T_{JCT}		125	°C
Soldering temperature (Pb-free profile)[5]	T_{PEAK}		260	°C
Soldering time at TPEAK (Pb-free profile)[5]	T_P		20 to 40	sec

1. Exposure to maximum rating conditions for extended periods may reduce device reliability. Exceeding any of the limits listed here may result in permanent damage to the device.
2. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
3. RoHS-6 compliant.
4. For more packaging information, go to https://www.skyworksinc.com/Product_Certificate.aspx
5. The device is compliant with JEDEC J-STD-020.

ESD Handling: *Industry-standard ESD handling precautions must be adhered to at all times to avoid damage to this device.*

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Table 5. Thermal Conditions

Parameter	Symbol	Test Condition	Typical Value		Unit
			JEDEC[1]	CEVB[2]	
Thermal resistance junction to ambient	Θ_{JA}	Still air	16.15	11.17	°C/W
		1 m/s	10.77	8.10	°C/W
		2 m/s	9.63	7.53	°C/W
Thermal resistance junction to board[3]	Ψ_{JB}	Still air	3.33	3.08	°C/W
Thermal resistance junction to top center	Ψ_{JC}	Still air	0.03	0.05	°C/W

1. Based on PCB dimension: 4-in. x 4.5-in., PCB thickness: 1.6 mm, number of Cu layers: 2.
2. Customer EVB: 8-layer board, board dimensions: ~9-in. x 9-in., all 8-layers are copper poured.
3. ΨJB can be used to calculate the junction temperature based on the board temperature and power dissipation for a given frequency plan, Tj = TPCB + (ΨJB *PD). TPCB should be measured as close to the Si5510/08 DUT as possible since temperature may vary across the PCB.

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Table 6. Recommended Operating Conditions

V_{DD18} = 1.8 V ±5%, V_{DDA} = V_{DDREF} = 3.3 V ±5%; All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C.
Low-Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDREF} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient temperature	T_A		–40	25	95	°C
Board temperature	T_B		–40	65	105	°C
Junction temperature	T_{JMAX}[1]		—	—	125	°C
Core supply voltage	V_{DD18}		1.71	1.80	1.89	V
	V_{DDA}[2]		3.14	3.30	3.47	V
		Low power mode	1.71	1.80	1.89	V
	V_{DDREF}		3.14	3.30	V_{DDA}[2]	V
		Low power mode	1.71	1.80	1.89	V
Input supply voltage	V_{DDIN}		3.14	3.30	V_{DDA}[2]	V
			2.38	2.50	2.62	V
			1.71	1.80	1.89	V
GPIO supply voltage	V_{DDIO}		3.14	3.30	V_{DDA}[2]	V
			2.38	2.50	2.62	V
			1.71	1.80	1.89	V
Clock output driver supply voltage	V_{DDO}		3.14	3.30	V_{DDA}[2]	V
			2.38	2.50	2.62	V
			1.71	1.80	1.89	V

1. Ambient temperature of 95 °C may not be possible with all configurations. This is dependent on device configuration. Tj cannot exceed a max of 125 °C.
2. VDDA must be greater than or equal to the highest voltage applied to the device. In Low-Power Mode, all voltage supplies must be set to 1.8 V.

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Table 7. DC Characteristics

V_{DD18} = 1.8 V ±5%, V_{DDA} = V_{DDREF} = 3.3 V ±5%; All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C.
Low-power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDREF} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Core supply current (V_{DD18} + V_{DDA})	I_{DD18}	Si5510/08[1, 2]	—	380	640	mA
	I_{DDA}	Si5510/08[1, 2]	—	210	230	mA
	I_{DD18_PD}	RSTb = 0	—	120	300	mA
	I_{DDA_PD}	RSTb = 0	—	15	16	mA
Periphery supply current (V_{DDIN} + V_{DDIO} + V_{DDREF})	I_{DDIN} + I_{DDIO}	Si5510/08[1, 2]	—	58	76	mA
	I_{DDREF}	Si5510/08[1, 2]	—	12	14	mA
	I_{DDIN_PD} + I_{DDIO_PD} + I_{DDREF_PD}	RSTb = 0	—	2	3	mA
Output buffer supply current (V_{DDOX})	I_{DDOX} (per output)	LVPECL (2.5 V, 3.3 V) @ 122.88 MHz[3]	—	24	26	mA
		LVDS (2.5 V, 3.3 V) @ 122.88 MHz[3]	—	13	15	mA
		S-LVDS (1.8 V) @ 122.88 MHz[3]	—	12	14	mA
		3.3 V LVCMOS @ 122.88 MHz[4]	—	19	22	mA
		2.5 V LVCMOS @ 122.88 MHz[4]	—	15	17	mA
		1.8 V LVCMOS @ 122.88 MHz[4]	—	11	12	mA
		HSCL internal termination (1.8 V, 2.5 V, 3.3 V) @ 122.88 MHz[5]	—	20	23	mA
		CML (1.8 V, 2.5 V, 3.3 V) @ 122.88 MHz[3]	—	14	17	mA
	I_{DDOX_PD}	RSTb = 0	—	0.23	0.3	mA
Total power dissipation	P_D	Si5510/08[2]	—	1.9	2.6	W
		Si5510/08 low-power mode[3]	—	1.4	2	W
Supply voltage ramp rate	T_{VDD}	Fastest V_{DD} ramp rate allowed on startup	—	—	100	V/ms

1. Si5510 typical test configuration: The following frequencies on 10 LVDS outputs: 2 to 491.52 MHz (Q), 1 to 122.88 MHz (Q), 2 to 1.92 MHz (Q), 1 to 100 MHz (NA), 1 to 50 MHz (NA), 2 to 156.25 MHz (NB), 1 to 125 MHz (NB). Excludes power dissipated in termination resistors. VDDIN = 1.8 V, VDDO = 3.3 V.
2. Typical test configuration: Same as Note 1, except all supplies set to 1.8 V for Low-Power Mode. Output formats changed to S-LVDS format.
3. Differential outputs terminated into an ac-coupled differential 100 Ω load.
4. LVCMOS outputs measured into a 5-inch, 50 Ω PCB trace with 5 pF load.
5. No external termination; amplitude 800 mVpp_se.

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Table 8. Input Specifications

V_{DD18} = 1.8 V ±5%, V_{DDA} = V_{DDREF} = 3.3 V ±5%; All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C.
Low-Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDREF} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C.

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
LVCMOS (XO/VCXO Applied to REF_IN)						
Input frequency range	f_{IN_CMOS}	Frequencies > 48 MHz are recommended for best performance.	30.72	—	250	MHz
Slew rate[1, 2, 3]	SR		0.75	—	—	V/ns
Input voltage	V_{IL}		—	—	V_{DDREF} x 0.3	V
	V_{IH}		V_{DDREF} x 0.7	—	—	V
Input resistance	R_{IN}		—	63	—	kΩ
Duty cycle	DC		40	—	60	%
Capacitance	C_{IN_SE}		—	1.25	—	pF
Differential (XO/VCXO Applied to REF_IN)						
Input frequency range	f_{IN_DIFF}	Frequencies > 48 MHz are recommended for best performance.	30.72	—	983.04	MHz
Voltage swing[2]	V_{IN_DIFF}		200	350 (LVDS) 800 (LVPECL)	1800	mVpp_se
Slew rate[1, 2, 3]	SR		0.75	—	—	V/ns
Duty cycle	DC		40	—	60	%
Capacitance	C_{IN_DIFF}		—	2.5	—	pF
Crystal (Connected to XA/XB Pins)[4]						
Frequency range	f_{IN_XTAL}		48	54	61.44	MHz
Load capacitance	CL		—	8	—	pF
Crystal drive level	dL		—	—	200	µW
Equivalent series resistance	R_{ESR}		Refer to the Si55xx/Si540x/Si536x Recommended XTALs Reference Manual to determine ESR and shunt capacitance values.			
Shunt capacitance	C0					
Differential (INx/INxb)						
Input frequency range	f_{IN_DIFF}	Differential, AC coupled	0.008	—	1000	MHz
	f_{IN_SE}	Single-ended, AC coupled	0.008	—	250	MHz
Voltage swing	V_{IN_DIFF}	Differential, AC coupled	200	350 (LVDS) 800 (LVPECL)	1800	mVpp_se
	V_{IN_SE}	Single-ended, AC coupled	400	1600	1800	mVpp_se
Slew rate[3, 5]	SR		0.4	—	—	V/ns
Duty cycle	DC		40	—	60	%
Capacitance	C_{IN_DIFF}		—	2.5	—	pF
LVCMOS (INx/INxb)						
Input frequency range	f_{IN_LVCMOS}		0.008	—	250	MHz
Slew rate[3, 5]	SR		0.2	0.4	—	V/ns
Input voltage	V_{IL}		—	—	V_{DDIN} x 0.3	V
	V_{IH}		V_{DDIN} x 0.7	—	—	V
Input resistance	R_{IN}		—	63	—	kΩ

Table 8. Input Specifications (Continued)

V_{DD18} = 1.8 V ±5%, V_{DDA} = V_{DDREF} = 3.3 V ±5%; All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C.
Low-Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDREF} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C.

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Duty cycle	DC		40	—	60	%
Capacitance	C_{IN_SE}		—	1.25	—	pF
Output Synchronization Pin (OSYNC)						
Update rate	f_{UR}		—	—	150	Hz
Input voltage	V_{IL}		—	—	V_{DDIO} x 0.3	V
	V_{IH}		V_{DDIO} x 0.7	—	—	V
Minimum pulse width[6]	PW		3	—	—	ms
Delay variation from OSYNC de-asserted to output re-enabled[7, 8]	t_{sync}		–1.6	—	1.6	ns
Internal pull-up	R_{IN}		—	20	—	kΩ
Other Control Input Pins (RSTb, FINC, FDEC, OE, PLLR_FORCE_HO, PLLR_INSEL[#], IN_FAIL[#])						
Update rate	f_{UR}	RSTb[9]	—	—	1	Hz
		FINC, FDEC	—	—	800	kHz
Input voltage	V_{IL}		—	—	V_{DDIO} x 0.3	V
	V_{IH}		V_{DDIO} x 0.7	—	—	V
Minimum pulse width	PW		150	—	—	ns
Programmable internal pullup, pulldown	R_{IN}		—	20	—	kΩ

1. The minimum slew rate on the XO/VCXO applied to REF_IN is recommended to meet the specified jitter performance.
2. To achieve this slew rate and voltage swing, use one of the XOs or VCXOs from the Si55xx/Si540x/Si536x Recommended XTALs Reference Manual placed as close as possible to the REF_IN pins.
3. Slew rate can be estimated using the following simplified equation: SR = ((0.8 - 0.2) x VIN_VPP_se)/tr.
4. To meet specified jitter performance use one of the XTALs from the Si55xx/Si540x/Si536x Recommended XTALs Reference Manual.
5. The minimum slew rate on the input clock applied to INx/INxb is recommended to meet the specified input-to-output delay and close-in phase noise (<1 kHz) performance.
6. No API commands can be sent to the device while the OSYNC pin is asserted.
7. Nominal delay is reported in CBPro and will vary based on configuration.
8. OSYNC delay variation is not specified for SYNC outputs.
9. Glitches and toggles on RSTb more frequent than fUR may cause the device to lock up in reset. Power cycle the device to restore operation.

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Table 9. I^{2}C Timing Specifications (SCL, SDA)

V_{DD18} = 1.8 V ±5%, V_{DDA} = V_{DDREF} = 3.3 V ±5%; All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C.
Low-Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDREF} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C.

Parameter	Symbol	Test Condition	Standard Mode 100 kbps		Fast Mode 400 kbps		Unit
			Min	Max	Min	Max	
SCL clock frequency	f_{SCL}		—	100	—	400	kHz
SMBus timeout	—		25	35	25	35	ms
Hold time (repeated) START condition	$t_{HD:STA}$		4.0	—	0.6	—	µs
LOW period of the SCL clock	t_{LOW}		4.7	—	1.3	—	µs
HIGH period of the SCL clock	t_{HIGH}		4.0	—	0.6	—	µs
Setup time for a repeated START condition	$t_{SU:STA}$		4.7	—	0.6	—	µs
Data hold time	$t_{HD:DAT}$		100	—	100	—	ns
Data setup time	$t_{SU:DAT}$		250	—	100	—	ns
Setup time for STOP condition	$t_{SU:STO}$		4.0	—	0.6	—	µs
Bus free time between a STOP and START condition	t_{BUF}		4.7	—	1.3	—	µs
Data valid time	$t_{VD:DAT}$		—	3.45	—	0.9	µs
Data valid acknowledge time	$t_{VD:ACK}$		—	3.45	—	0.9	µs

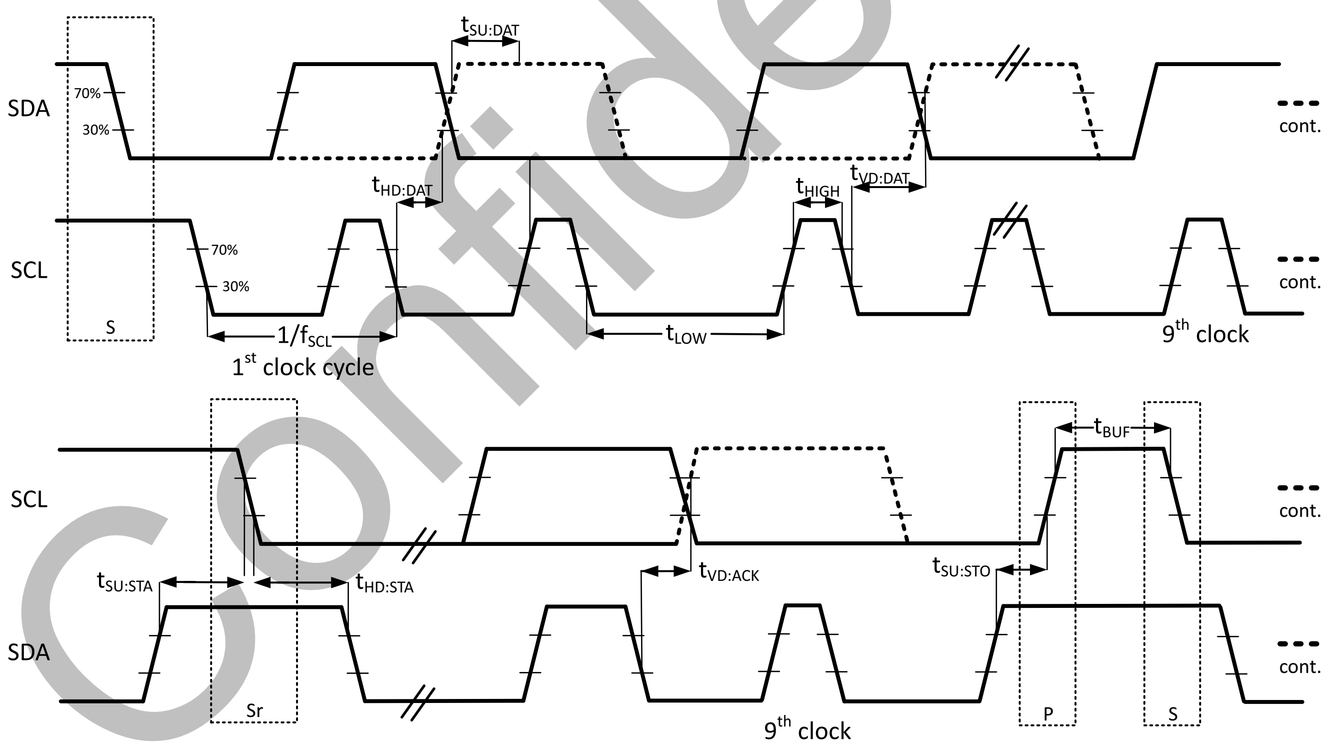

Figure 10. I^{2}C Serial Port Timing Standard and Fast Modes

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Table 10. SPI Timing Specifications (4-Wire)

V_{DD18} = 1.8 V ±5%, V_{DDA} = V_{DDREF} = 3.3 V ±5%; All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C.
Low-Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDREF} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C.

Parameter	Symbol	Min	Typ	Max	Unit
SCLK frequency	f_{SPI}	—	—	30	MHz
SCLK duty cycle	T_{DC}	40	—	60	%
SCLK period	T_C	33.333	—	—	ns
Delay time, SCLK fall to SDO active	T_{D1}	—	12.5	20	ns
Delay time, SCLK fall to SDO	T_{D2}	—	10	15	ns
Delay time, CSb rise to SDO tri-state	T_{D3}	—	10	20	ns
Setup time, CSb to SCLK	T_{SU1}	5	—	—	ns
Hold time, SCLK fall to CSb	T_{H1}	5	—	—	ns
Setup time, SDI to SCLK rise	T_{SU2}	5	—	—	ns
Hold time, SDI to SCLK rise	T_{H2}	5	—	—	ns
Delay time between chip selects (CSb)	T_{CS}	5	—	—	µs

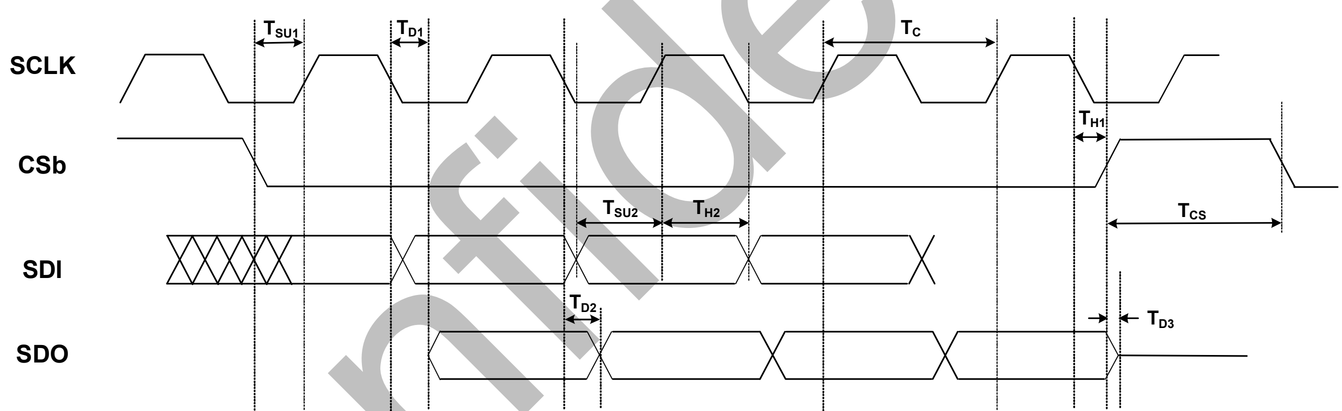

Figure 11. 4-Wire SPI Serial Interface Timing

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Table 11. SPI Timing Specifications (3-Wire)

V_{DD18} = 1.8 V ±5%, V_{DDA} = V_{DDREF} = 3.3 V ±5%; All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C.
Low-Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDREF} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C.

Parameter	Symbol	Min	Typ	Max	Unit
SCLK frequency	f_{SPI}	—	—	30	MHz
SCLK duty cycle	T_{DC}	40	—	60	%
SCLK period	T_C	33.33	—	—	ns
Delay time, SCLK fall to SDIO turn-on	T_{D1}	—	12.5	20	ns
Delay time, SCLK fall to SDIO next-bit	T_{D2}	—	10	15	ns
Delay time, CSb rise to SDIO tri-state	T_{D3}	—	10	20	ns
Setup time, CSb to SCLK	T_{SU1}	5	—	—	ns
Hold time, CSb to SCLK fall	T_{H1}	5	—	—	ns
Setup time, SDI to SCLK rise	T_{SU2}	5	—	—	ns
Hold time, SDI to SCLK rise	T_{H2}	5	—	—	ns
Delay time between chip selects (CSb)	T_{CS}	5	—	—	µs

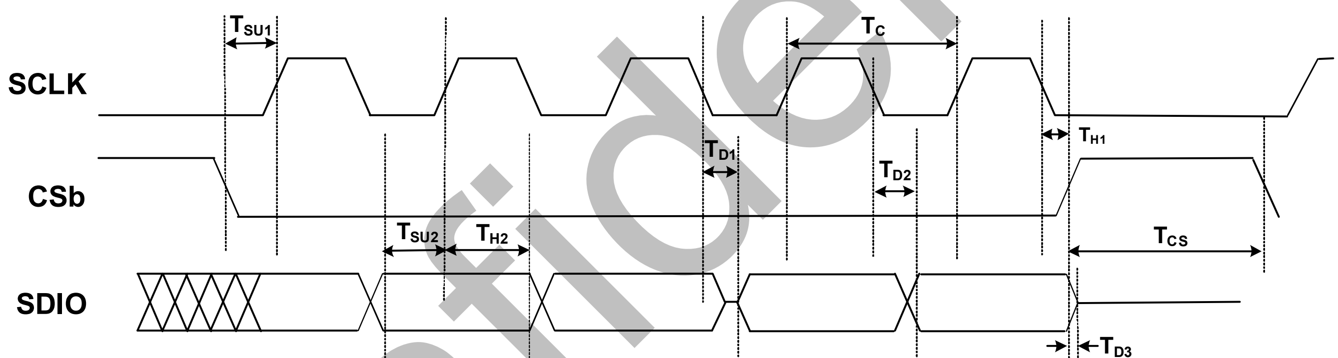

Figure 12. 3-Wire SPI Serial Interface Timing

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Table 12. Differential Clock Output Specifications

V_{DD18} = 1.8 V ±5%, V_{DDIN} = V_{DDIO} = 3.3 V ±5%, 1.8 V, V_{DDREF} = V_{DDA} = 3.3 V ±5%, V_{DDO} = 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C.
Low-Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDREF} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A= –40 to 95 °C.

Parameter	Symbol	Test Condition			Min	Typ	Max	Units
Output frequency	f_{OUT}	Q divider, non-PPS[1]			0.008	—	3200	MHz
		Q divider, PPS			0.5	—	1	Hz
		NA divider, non-PPS[2]			0.008		650	MHz
		NA divider, PPS			0.5	—	1	Hz
		NB divider			0.008		650	MHz
Duty cycle	DC	f < 400 MHz			49.5	50	50.5	%
		400 MHz < f < 3.2 GHz			48	50	52	
Output-to-output skew	T_{SK}	Q divider outputs, same differential format[3]			–50	—	50	ps
		MultiSynth (NA or NB) outputs, same differential format, same MultiSynth[3]						
		VCXO buffered outputs, same differential format						
		Q divider outputs, differential SYSCLK to LVCMOS SYNC			0	—	300	
		Q divider to VCXO buffered outputs, same differential format[4]			–1200	—	1200	
OUT-OUTb skew	T_{SK_OUT}	Skew between positive and negative output pins	VDDO = 3.3 V	LVPECL, LVDS, CML, and custom diff f < 491.52 MHz	—	—	10	ps
			VDDO = 2.5 V	LVPECL, LVDS, CML, and custom diff f < 491.52 MHz	—	—	25	
			VDDO = 3.3 V/2.5 V	LVPECL, LVDS, CML, and custom diff f > 491.52 MHz	—	—	25	
			VDDO = 1.8 V	CML, S-LVDS, and custom diff All frequencies	—	—	35	
Output voltage swing[5]	V_{OUT}	VDDO = 3.3 V/2.5 V		LVDS	330 x SF	360 x SF	380 x SF	mVpp_se
		VDDO = 1.8 V		S-LVDS	350 x SF	370 x SF	410 x SF	
		VDDO = 3.3 V/2.5 V		AC coupled LVPECL	780 x SF	840 x SF	910 x SF	
		VDDO = 3.3 V/2.5 V/1.8 V		CML	390 x SF	420 x SF	460 x SF	
		VDDO= 3.3 V/2.5 V		Custom diff 600 mVpp_se	560 x SF	610 x SF	650 x SF	
Output voltage swing scaling factor OUT0–15	SF	f < 491.52 MHz			1	1	1	SF
		491.52 MHz < f < 983.04 MHz			0.9	0.95	1	
		983.04 MHz < f < 1.47456 GHz			0.8	0.9	1	
		1.47456 GHz < f < 2.47456 GHz			0.7	0.75	0.85	
		f > 2.47456 GHz			0.5	0.6	0.75	
Output voltage swing scaling factor OUT16/17[6]	SF	f < 491.52 MHz			1	1	1	
		491.52 MHz < f < 983.04 MHz			0.9	0.95	1	
		983.04 MHz < f < 1.47456 GHz			0.8	0.9	1	
		1.47456 GHz < f < 2.47456 GHz			0.7	0.75	0.85	
		f > 2.47456 GHz			0.5	0.6	0.75	

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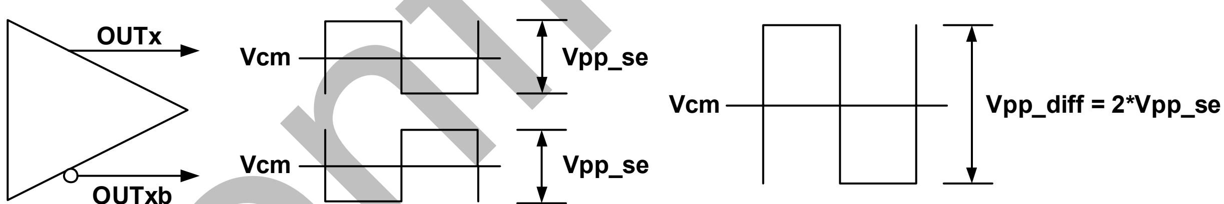
Table 12. Differential Clock Output Specifications (Continued)

V_{DD18} = 1.8 V ±5%, V_{DDIN} = V_{DDIO} = 3.3 V ±5%, 1.8 V, V_{DDREF} = V_{DDA} = 3.3 V ±5%, V_{DDO} = 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C.
Low-Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDREF} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A= –40 to 95 °C.

Parameter	Symbol	Test Condition		Min	Typ	Max	Units
Common mode voltage	V_{CM}	VDDO = 3.3 V/2.5 V	LVDS, custom differen-tial, CML	1.15	1.2	1.25	V
		VDDO = 1.8 V	S-LVDS, CML	0.85	0.9	0.95	
Rise and fall times (20% to 80%), OUT0 - 15	t_r/t_f	VDDO = 3.3 V/2.5 V	LVDS, AC coupled LVPECL, custom	—	125	260	ps
		VDDO = 1.8 V	S-LVDS	—	150	270	
		VDDO = 3.3 V/2.5 V	CML	—	150	280	
Rise and fall times (20% to 80%), OUT016-17	t_r/t_f	VDDO = 3.3 V/2.5 V	LVDS, AC coupled LVPECL, custom	—	140	300	ps
		VDDO = 1.8 V	S-LVDS	—	165	310	
		VDDO = 3.3 V/2.5 V/1.8 V	CML	—	165	320	
Differential output impedance	Z_O	All differential formats		—	100	—	Ω
Power supply noise rejection[7]	PSR	25 kHz sinusoidal noise		—	–96	—	dBc
		100 kHz sinusoidal noise		—	–97	—	
		500 kHz sinusoidal noise		—	–93	—	
		1 MHz sinusoidal noise		—	–93	—	
Output-to-output crosstalk[8]	$XTALK_{OUT}$	Differential outputs, same format		—	–95	—	dBc
Input-to-output crosstalk[9]	$XTALK_{IN}$	Differential input and output, same format		—	–90	—	dBc

1. Q dividers support output frequencies within the specified range equal to fVCO/Q where Q is an integer.
2. NA, NB MultiSynths support any output frequency within the specified range.
3. SYNC outputs are not included in this output-to-output skew specification.
4. "Align Qdivs to VCXO buffered output(s)" must be selected on the "Output Skew Control" page of CBPro. When Q divider outputs are aligned to the VCXO buffered output the input-to-output-delay is no longer specified unless using zero-delay mode.
5. Output voltage swing is dependent on frequency range. Scale all values by the output voltage swing scaling factor (SF). Voltage swing is specified in mVpp_SE as shown below.



6. OUT16/17 have programmable slew rate limit capability when configured as SRL LVCMOS. This causes additional attenuation for higher frequency outputs.The Output Voltage Swing Scaling Factor (SF) for OUT16/OUT17 is shown below. It is recommended to use OUT0-15 for fOUT > 491.52 MHz.

7. Measured for a 122.88 MHz output frequency. 100 mVpp sinewave noise added to VDDO = 3.3 V and noise spur amplitude measured.

8. Crosstalk spur measured with the victim running at 153.6 MHz and the aggressor at 156.25 MHz. Victim and aggressor are separated by two unused channels.

9. Crosstalk spur measured with the victim running at 153.6 MHz on OUT0 and the aggressor at 156.25 MHz on IN3.

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Table 13. HCSL Clock Output Specifications

V_{DD18} = 1.8 V ±5%, V_{DDIN} = V_{DDIO} = 3.3 V ±5%, 1.8 V ±5%, V_{DDREF} = V_{DDA} = 3.3 V ±5%, V_{DDO} = 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5% T_A = –40 to 95 °C
Low Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDREF} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C.

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Output frequency	f_{OUT}	Q divider, non PPS[1]	0.008	–	500	MHz
		Q divider, PPS	0.5	–	1	Hz
		NA divider, non PPS[2]	0.008	–	500	MHz
		NA divider, PPS	0.5	–	1	Hz
		NB divider[2]	0.008	–	500	MHz
Duty cycle	DC	f < 400 MHz	49.5	50	50.5	%
		400 MHz < f < 500 MHz	48	50	52	
Output-to-output skew	T_{SK}	Q divider outputs, same differential format[3]	–50	–	50	ps
		MultiSynth (NA or NB) outputs, same differential format, same Multi-Synth				
		VCXO buffered outputs, same differential format				
		Q divider outputs, Differential SYSCLK to LVCMOS SYNC output	0	–	300	
		Q divider to VCXO buffered outputs, same differential format[4]	–1200	–	1200	
OUT-OUTb skew	T_{SK_OUT}	Skew between positive and negative output pins. VDDO=3.3V, HCSL standard, 800 mVpp_se, int term	–	–	15	ps
		VDDO=3.3V, HCSL standard, 800 mVpp_se, ext term	–	–	25	
		VDDO=3.3V, HCSL fast, 800 mV or 1200 mV, ext term	–	–	10	
		VDDO=2.5V, HCSL standard, 800 mVpp_se, int term	–	–	15	
		VDDO=2.5V, HCSL standard, 800 mVpp_se, ext term	–	–	30	
		VDDO=2.5V, HCSL fast, 800 mV or 1200 mV, ext term	–	–	20	
		VDDO=1.8V, HCSL standard, 800 mVpp_se, int term	–	–	22	
		VDDO=1.8V, HCSL standard, 800 mVpp_se, ext term	–	–	70	
		VDDO=1.8V, HCSL fast, 800 mV, ext term	–	–	36	
Output voltage swing[5]	V_{OUT}	VDDO = 3.3 V/ 2.5 V/1.8 V, HCSL standard, 800 mVpp_se, int term	740*SF	810*SF	960*SF	mVpp_se
		VDDO = 3.3 V/ 2.5 V/1.8 V, HCSL standard, 800 mVpp_se, ext term	730*SF	810*SF	960*SF	
		VDDO = 3.3 V/ 2.5 V, HCSL fast, 800 mVpp_se, ext term	730*SF	810*SF	960*SF	
		VDDO = 3.3 V/ 2.5 V, HCSL fast, 1200 mVpp_se, ext term	1100*SF	1175*SF	1260*SF	
Output voltage swing Scaling Factor (SF) standard, 800mVpp_se, int term OUT0-17	SF	f < 10 MHz	1	1	1	SF
		10 MHz < f < 100 MHz	0.91	0.94	0.95	
		100 MHz < f < 200 MHz	0.89	0.91	0.93	
		200 MHz < f < 400 MHz	0.83	0.85	0.92	
		f > 400 MHz	0.74	0.78	0.89	
Output voltage swing Scaling Factor (SF) standard, 800 mVpp_se, ext term OUT0-17	SF	f < 10 MHz	1	1	1	SF
		10 MHz < f < 100 MHz	0.97	0.96	0.97	
		100 < f < 200 MHz	0.94	0.93	0.95	
		200 MHz < f < 400 MHz	0.91	0.90	0.88	
		f > 400 MHz	0.68	0.71	0.75	

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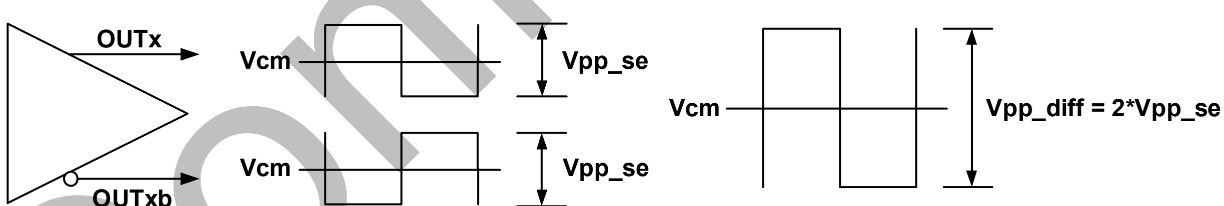
Table 13. HCSL Clock Output Specifications (Continued)

V_{DD18} = 1.8 V ±5%, V_{DDIN} = V_{DDIO} = 3.3 V ±5%, 1.8 V ±5%, V_{DDREF} = V_{DDA} = 3.3 V ±5%, V_{DDO} = 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5% T_A = –40 to 95 °C
Low Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDREF} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C.

Parameter	Symbol	Test Condition		Min	Typ	Max	Units
Output voltage swing Scaling Factor (SF) Fast, 800 or 1200 mVp-p_se, ext term OUT0-17	SF	f < 10 MHz		1	1	1	SF
		10 MHz < f < 100 MHz		0.98	0.99	0.99	
		100 < f < 200 MHz		0.94	0.94	0.96	
		200 MHz < f < 400 MHz		0.94	0.95	0.97	
		f > 400 MHz		0.89	0.92	0.95	
Common mode voltage	V_{CM}	VDDO = 3.3 V/2.5 V/1.8 V	HCSL 800 mVpp_se	0.35	0.425	0.52	V
		VDDO = 3.3 V/2.5 V	HCSL 1200 mVpp_se	0.55	0.6	0.68	
Rise and fall times (20% to 80%) OUT0 - 15	t_r/t_f	VDDO = 3.3 V/2.5 V/1.8 V	HCSL fast, 800 or 1200 mVpp_se, ext term	–	270	360	ps
		VDDO = 3.3 V/2.5 V/1.8 V	HCSL standard, 800 mVpp_se, ext term	–	450	700	
		VDDO = 3.3 V/2.5 V/1.8 V	HCSL standard, 800 mVpp_se, int term	–	270	420	
Rise and fall times (20% to 80%) OUT16-17[6]	t_r/t_f	VDDO= 3.3 V/2.5 V/1.8 V	HCSL fast, 800 or 1200 mVpp_se, ext term	–	285	400	ps
		VDDO = 3.3 V/2.5 V/1.8 V	HCSL standard, 800 mVpp_se, ext term	–	465	740	
		VDDO = 3.3 V/2.5 V/1.8 V	HCSL standard, 800 mVpp_se, int term		285	460	
Differential output impedance	Z_O	HCSL standard slew rate, int term		–	100	–	Ω
		HCSL standard slew rate, ext term		–	Hi-Z	–	
		HCSL fast slew rate, ext term		–	200	–	
Output-to-output crosstalk[7]	$XTALK_{OUT}$	HCSL outputs, same format		–	–95	–	dBc
Input-to-output crosstalk[8]	$XTALK_{IN}$	HCSL input and output, same format		–	–90	–	dBc

1. Q dividers support output frequencies within the specified range equal to fVCO/Q where Q is an integer.
2. NA, NB MultiSynths support any output frequency within the specified range.
3. SYNC outputs are not included in this output-to-output skew specification.
4. "Align Qdivs to VCXO buffered output(s)" must be selected on the "Output Skew Control" page of CBPro. When Q divider outputs are aligned to the VCXO buffered output the input-to-output-delay is no longer specified unless using zero-delay mode.
5. Output voltage swing is dependent on frequency range, HCSL slew rate and HCSL termination settings . Scale all voltage swing values by the scaling factor (SF). Voltage swing is specified in mVpp_SE as shown below.



6. OUT16/17 have programmable slew rate limit capability when configured as LVCMOS. This causes additional attenuation for higher frequency outputs. The Output Voltage Swing Scaling Factor (SF) for OUT16/OUT17 is shown below. It is recommended to use OUT0-15 for fOUT > 491.52 MHz.
7. Crosstalk spur measured with the victim running at 153.6 MHz and the aggressor at 156.25 MHz. Victim and aggressor are separated by two unused channels.
8. Crosstalk spur measured with the victim running at 153.6 MHz on OUT0 and the aggressor at 156.25 MHz on IN3.

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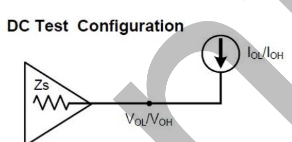
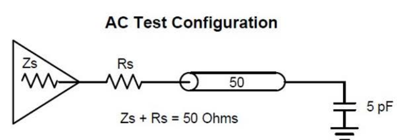
Table 14. LVCMOS Clock Output Specifications

V_{DD18} = 1.8 V ±5%, V_{DDA} = V_{DDREF} = 3.3 V ±5%; All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = -40 to 95 °C.
Low-Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDREF} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A= –40 to 95 °C.

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Output frequency	f_{OUT}	Q divider, non-PPS[1]	0.008	—	250	MHz
		Q divider, PPS	0.5	—	1	Hz
		NA divider, non-PPS[2]	0.008	—	250	MHz
		NA divider, PPS[2]	0.5	—	1	Hz
		NB divider[2]	0.008	—	250	MHz
Duty cycle	DC	f < 100 MHz	49.5	—	50.5	%
		100 MHz < f < 250 MHz	45	—	55	
Output voltage high[3]	V_{OH}	VDDO= 3.3 V/2.5 V/1.8 V IOH = –8/–6/–4 mA, IOL = 8/6/4 mA	VDDO x 0.85	—	—	V
Output voltage low[3]	V_{OL}		—	—	VDDO x 0.15	V
Rise and fall times (20% to 80%)[4, 5, 6]	t_r/t_f	LVCMOS	0.35	0.8	1.35	ns
		SRL LVCMOS "4 ns rise/fall"	3	4	6	ns
		SRL LVCMOS "6.5 ns rise/fall"	4	6.5	10	
		SRL LVCMOS "13 ns rise/fall"	7	13	24	
		SRL LVCMOS "25 ns rise/fall"	13	25	42	

1. Q dividers support output frequencies within the specified range equal to fVCO/Q where Q is an integer.
2. NA, NB MultiSynths support any output frequency within the specified range.
3. VOL VOH is measured at IOL /IOH as shown in the DC Test Configuration.
4. A 15 to 25 Ω series termination resistor (RS) is recommended to help match the source impedance to a 50 Ω PCB trace. A 5 pF capacitive load is assumed as shown in the AC test configuration.





5. Slew rate limited (SRL) LVCMOS format only available on OUT16/OUT17
6. SRL LVCMOS format clocks are intended only for low frequency clock applications. Refer to the Si5518/12/10/08 Reference Manual for the maximum f_{OUT} supported for each slew rate selection.

Table 15. VCNTRL Output Pin Specifications

V_{DDREF} = V_{DDA} = 3.3 V ±5%, T_A = –40 to 95 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Output voltage high	V_{OH}	V_{DDREF} = 3.3 V[1] R_{LOAD} > 20 kΩ	V_{DDREF} x 0.9	—	—	V
Output voltage low	V_{OL}		—	—	V_{DDREF} x 0.1	V

1. VCXO is not supported in low-power mode.

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Table 16. Output Status Pin Specifications

V_{DDIO} = 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A= –40 to 95 °C
Low-Power Mode: VDDIO = 1.8 V ±5%

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Serial and Status Output Pins (GPIO, SDA/SDIO, SDO)						
Output voltage high	V_{OH}[1]	I_{OH} = –2 mA	V_{DDIO} x 0.85	—	—	V
Output voltage low	V_{OL}	I_{OL} = 2 mA	—	—	V_{DDIO} x 0.15	V

1. The V_{OH} specification does not apply to the open-drain SDA output when the serial interface is in I^2C mode. V_{OL} remains valid in all cases.

Table 17. Performance Characteristics

V_{DD18} = 1.8 V ±5%, V_{DDA} = V_{DDREF} = 3.3 V ±5%; All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C.
Low-Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDREF} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A= –40 to 95 °C.

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Initial start-up time	t_{START_XO}	Time from POR to when the device generates free-running clocks from NVM frequency plan	—	25	40	ms
	t_{START_XTAL}		—	120	270	
	t_{RDY}	POR to API ready	—	25	30	
PLL lock time[1]	t_{ACQ}	RFPLL, IN = 19.44 MHz, BW = 100 Hz, FLOL De-assert	—	0.23	0.35	s
		RFPLL, IN = 19.44 MHz, BW = 100 Hz, LOL De-assert	—	1.3	1.6	
Output delay adjustment	t_{QDIV}	Range[2]	–TVCO x 127	—	+TVCO x 127	ps
		Resolution		TVCO	—	
		Resolution - fine delay enabled		TVCO/4	—	
Jitter peaking	J_{PK}	RFPLL	—	—	0.1	dB
Max phase transient during hitless switch[3]	t_{SWITCH}		—	35	150	ps
Pull-in range[4]	ω_P		—	±100	—	ppm
Input-to-output delay + variation[5, 6]	$t_{IODELAY}$	RFPLL	–400	—	400	ps
	t_{ZDELAY}	ZDM	–100	—	100	
RMS jitter performance[7] 12 kHz to 20 MHz	J_{GEN_VCXO}[8]	491.52 MHz, Q div	—	43	65	fs
		156.25 MHz, NA or NB div (NA and NB only supported in Si5510)	—	81	135	
	$J_{GEN\_VCXO\_BUFF\_OUT}$[8]	122.88 MHz, buffer output	—	38	—	
	J_{GEN_XO}[9]	491.52 MHz, Q div	—	47	70	
		156.25 MHz, NA or NB div (NA and NB only supported in Si5510)	—	91	135	

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Table 17. Performance Characteristics (Continued)

V_{DD18} = 1.8 V ±5%, V_{DDA} = V_{DDREF} = 3.3 V ±5%; All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C.
Low-Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDREF} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A= –40 to 95 °C.

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Phase noise performance[10]	PN_491.52M_VCXO_Q_Div[8]	10 Hz	—	–79	—	dBc/Hz
		100 Hz	—	–99	—	
		1 kHz	—	–124	—	
		10 kHz	—	–135	—	
		100 kHz		–141	—	
		800 kHz	—	–146	—	
		1 MHz	—	–146	—	
		10 MHz	—	–162	—	
		40 MHz	—	–164	—	
	PN_122.88M_VCXO_ BUFF_OUT[8]	10 Hz	—	–92	—	dBc/Hz
		100 Hz	—	–108	—	
		1 kHz	—	–136	—	
		10 kHz	—	–153	—	
		100 kHz	—	–163	—	
		800 kHz	—	–167	—	
		1 MHz	—	–167	—	
		10 MHz	—	–167	—	
		40 MHz	—	–168	—	
	PN_491.52M_XO_Q_Div[10]	10 Hz	—	–79	—	dBc/Hz
		100 Hz	—	–107	—	
		1 kHz	—	–127	—	
		10 kHz	—	–135	—	
		100 kHz	—	–138	—	
		800 kHz	—	–145	—	
		1 MHz	—	–146	—	
		10 MHz	—	–161	—	
		40 MHz	—	–164	—	

1. FLOL de-asserts once frequency lock is achieved. LOL de-asserts once both frequency and phase lock are achieved. Refer to 3.12.2. Lock Acquisition Mode for more details on LOL thresholds.
2. Output delay adjustment range will vary depending on frequency plan. Output delay adjust range (ns) is displayed in the “Output Skew Control” step of the CBPro Wizard. FVCO range is 10.4 GHz to 13 GHz.
3. Phase transient specification only applies to clock switches between two synchronous inputs to the RFPLL configured for a phase build-out clock switching mode in CBPro.
4. When using a VCXO reference, the pull-in range for RFPLL will be limited by the APR of the VCXO. For more information, see the Si5518/12/10/08 Reference Manual.
5. Input-to-output (IO) delay is measured at the output driver with respect to the input. Fin = Fout. This spec excludes wander form the OCXO/TCXO.
6. Input-to-output delay is measured at the output driver with respect to the input after the output phase has achieved a steady state value. This spec excludes wander from the OCXO/TCXO.
7. Added jitter and spurs due to crosstalk is frequency-plan-dependent and can be determined using the ClockBuilder Pro Spur Analysis tool.
8. Jitter generation conditions: VCXO = 122.88 MHz Rakon RVX1490U-V4104, fIN = 156.25 MHz, LVPECL output format, RFPLL BW = 40 Hz. VCXO buffer output jitter and phase noise specifications include the jitter and phase noise of the VCXO.
9. Jitter generation conditions: XO = 54 MHz TXC 7X54070001, fIN = 156.25 MHz, LVPECL output format, RFPLL BW = 40 Hz.
10. An SMA-100a low noise signal generator is used as the input to the RFPLL for phase noise performance.

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5. Typical Operating Characteristics

The phase noise plots shown below were taken under the following conditions: f_{IN} = 156.25 MHz, f_{OUT} LVDS, RFPLL BW = 40 Hz, VCXO = 122.88 MHz Rakon RVX1490U-V4104, TA = 25 °C for VCXO.

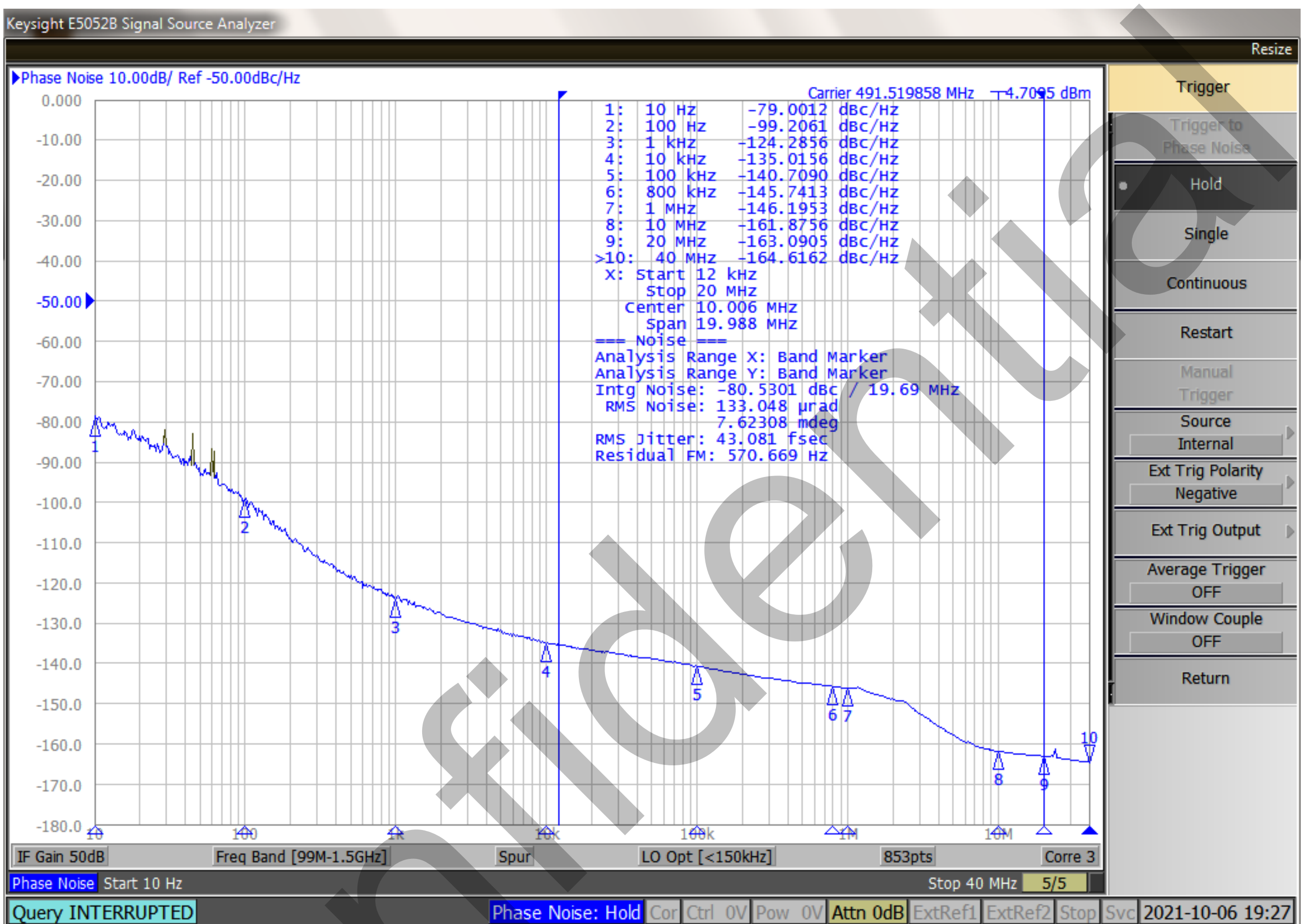

Figure 13. VCXO Configuration, f_{IN} = 156.25 MHz, f_{OUT} = 491.52 MHz

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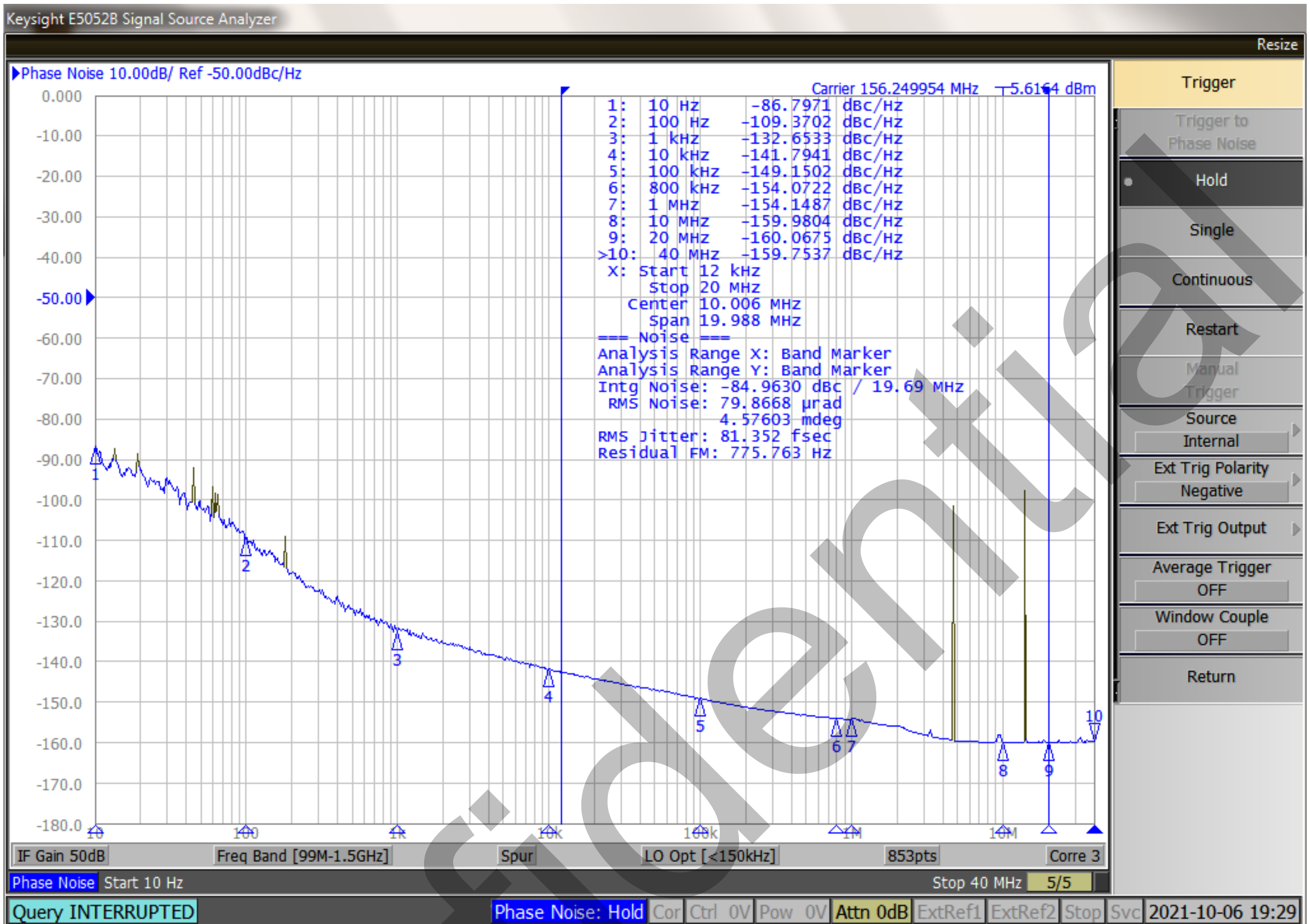

Figure 14. Si5510 Only: VCXO Configuration, f_{IN} = 156.25 MHz, f_{OUT} = 156.25 MHz

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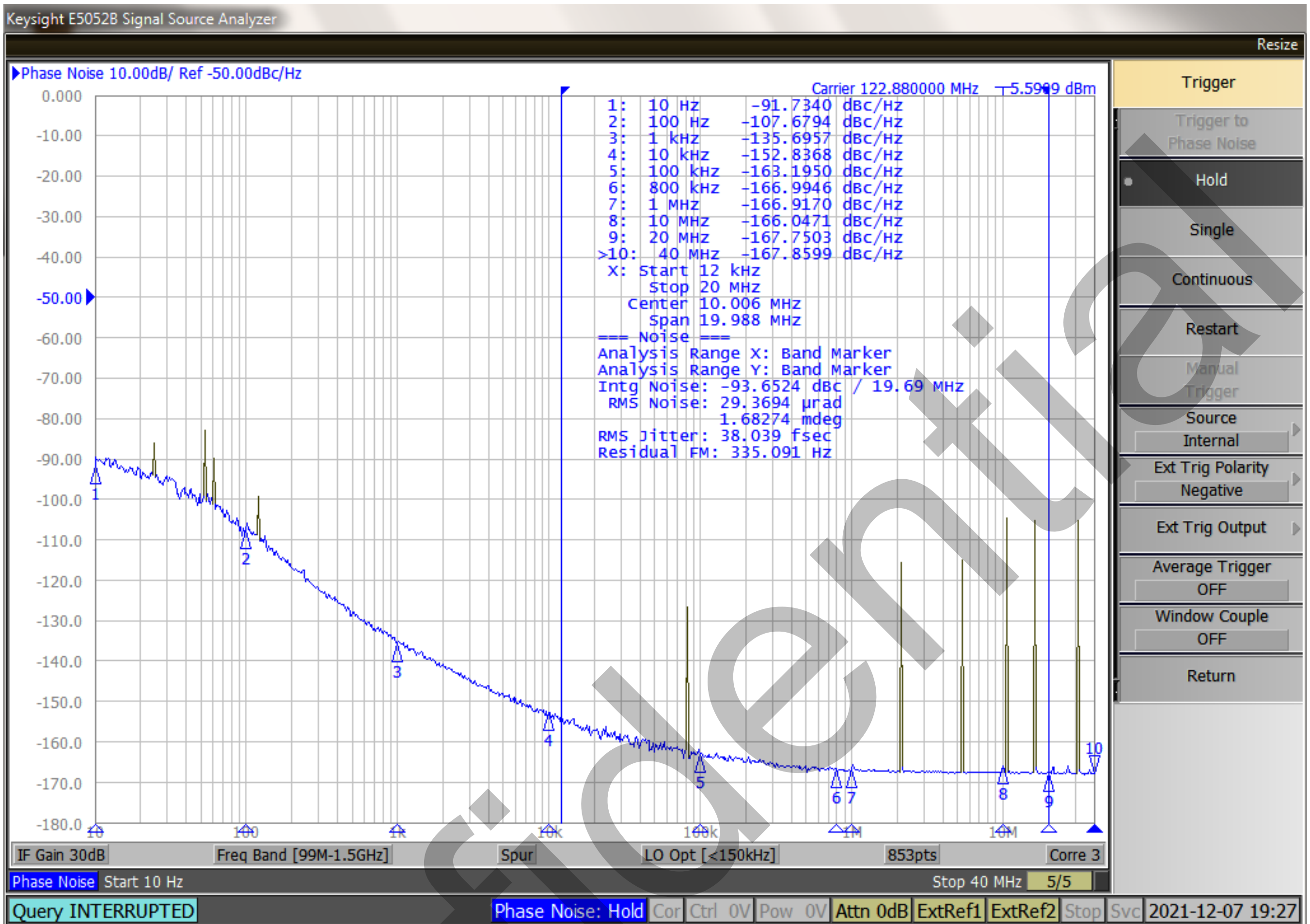

Figure 15. VCXO Buffer Output Configuration, f_{IN} = 156.25 MHz, f_{OUT} = 122.88 MHz

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The phase noise plots shown below were taken under the following conditions: f_{IN} =156.25 MHz, f_{OUT} LVDS, RFPLL BW = 40 Hz, XO = 54 MHz TXC 7X54070001, TA = 25 °C for XO.

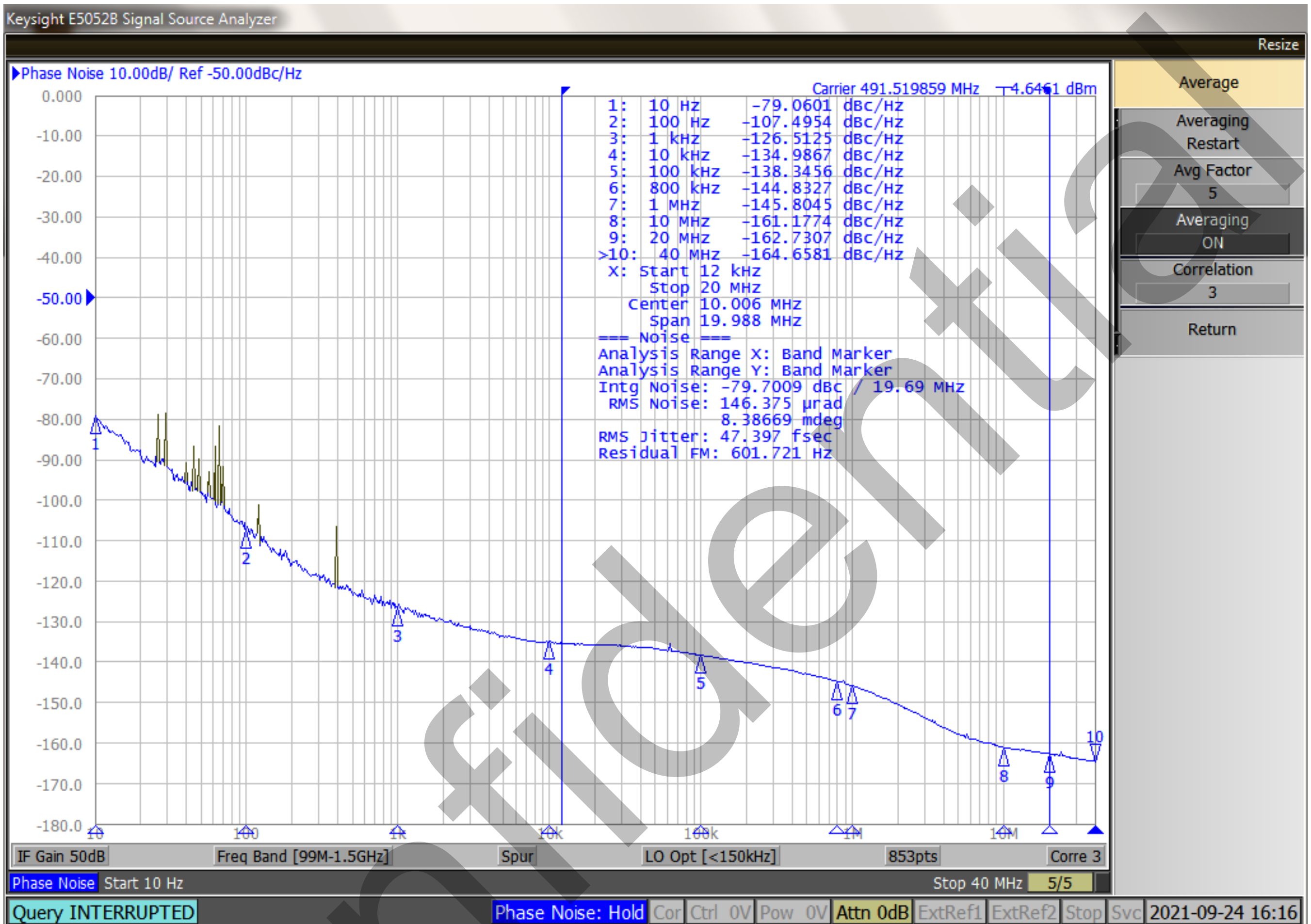

Figure 16. XO Configuration, f_{IN} = 156.25 MHz, f_{OUT} = 491.52 MHz

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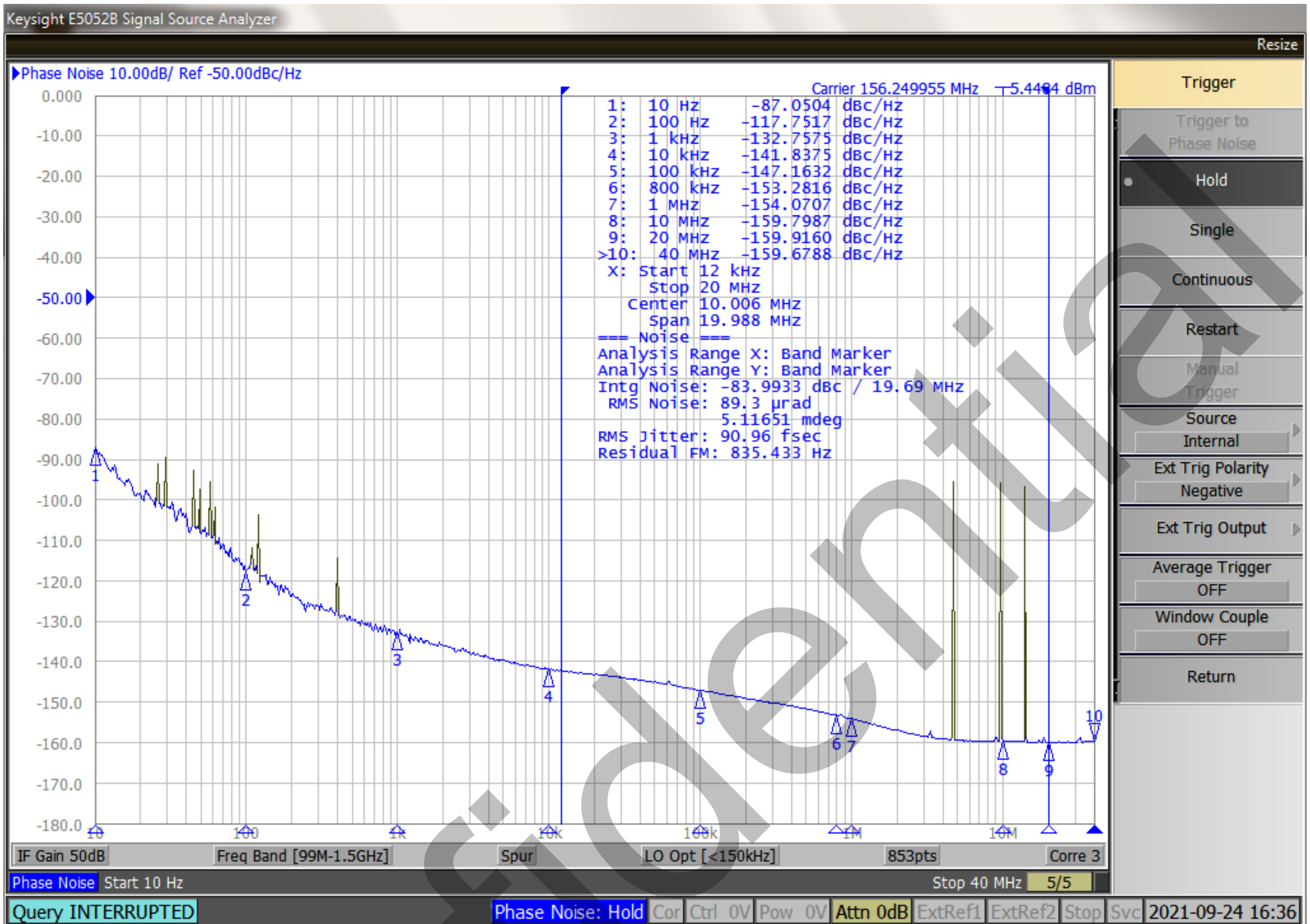

Figure 17. Si5510 Only: XO Configuration, f_{IN} = 156.25 MHz, f_{OUT} = 156.25 MHz

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6. Pin Descriptions

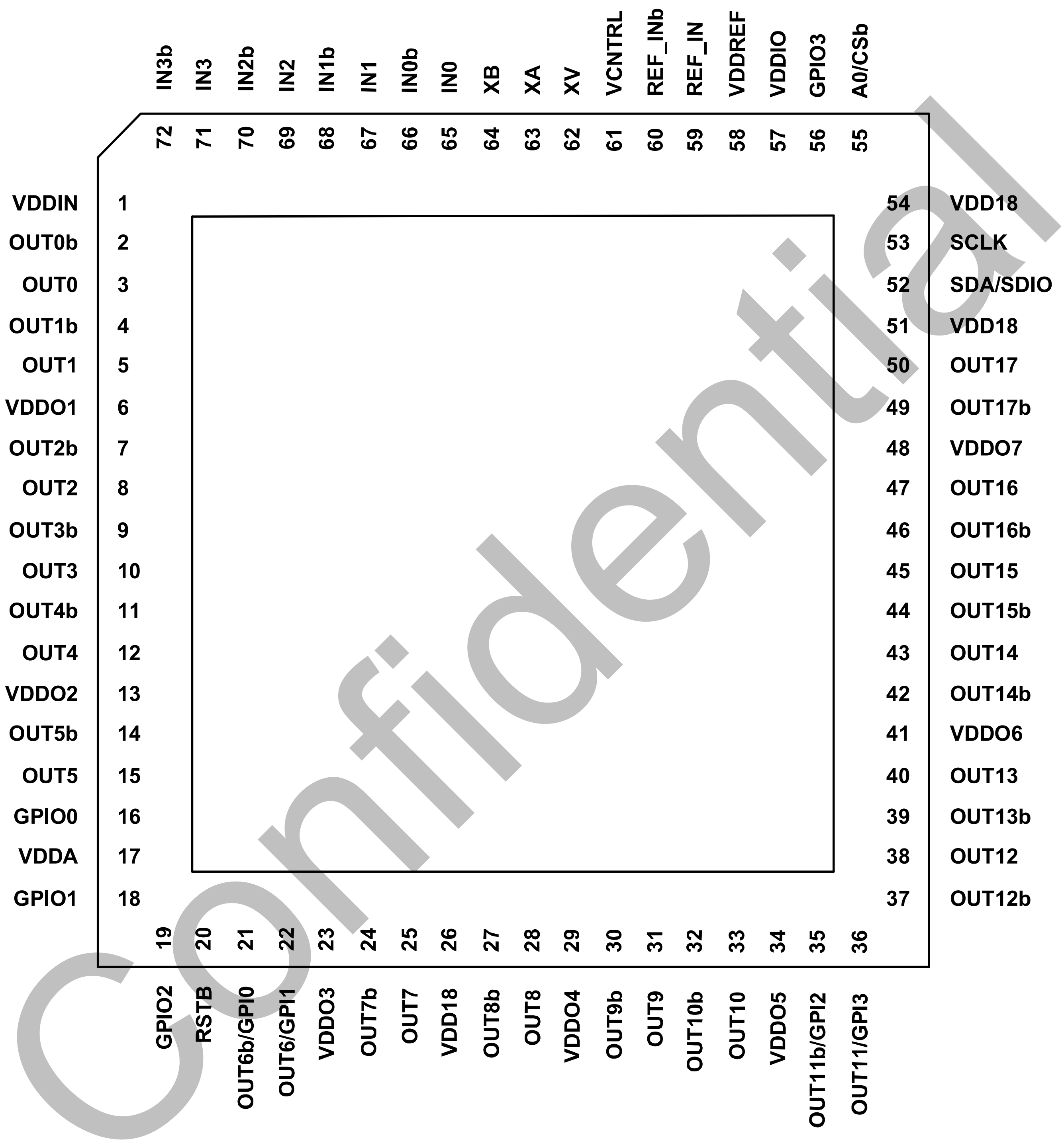

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Figure 18. Pin Descriptions

Table 18. Pin Descriptions

Pin Name	Pin Number	Pin Type[1]	Function
Inputs			
REF_IN	59	I	Input for low phase noise (XO or VCXO).
REF_INb	60		
XV	62	I	**XTAL and VCNTRL Shield** Connect this pin directly to the XTAL and VCNTRL capacitor ground pins. Do not ground the XV pin. XV should be isolated from the PCB ground plane. Refer to the AN1293 Si55xx Schematic Design and Board Layout Guide Confidential for layout guidelines.
XA	63	I	**Crystal Input** Pins for external crystal (XTAL). XA and XB pins can be left unconnected when not in use.
XB	64		
IN0	65	I	**Clock Inputs** IN0 to IN3 accept an input clock for synchronizing the device. They support both differential and single-ended clock signals. When operating in single-ended mode, inputs IN2 and IN3 can provide two SE inputs each for a total of six inputs. Refer to the Si5518/12/10/08 Reference Manual and AN1293: Si55xx Schematic Design and Board Layout Guide for input termination options. These pins are high-impedance and must be terminated externally. IN0 to IN3 can be disabled in CBPro and the pins left unconnected if unused.
IN0b	66		
IN1	67		
IN1b	68		
IN2	69		
IN2b	70		
IN3	71		
IN3b	72		
Outputs			
VCNTRL	61	O	**VCXO Control Voltage** Connect this pin directly to the VCXO control voltage input. Place a 0.01 µF capacitor as close to VCNTRL as possible, between the VCNTRL pin and XV, to reduce noise. VCNTRL may be left unconnected when not using a VCXO reference.
OUT0b	2	O	**Output Clocks** The output clocks can be programmed as single-ended CMOS or differential LVDS, S-LVDS, CML, HCSL or ac-coupled LVPECL and support a programmable signal amplitude and common-mode voltage. Desired output signal format is configurable in CBPro. Termination recommendations are provided in the Si5518/12/10/08 Reference Manual. Unused outputs should be left unconnected.
OUT0	3		
OUT1b	4		
OUT1	5		
OUT2b	7		
OUT2	8		
OUT3b	9		
OUT3	10		
OUT4b	11		
OUT4	12		
OUT5b	14		
OUT5	15		
OUT6b GPI0	21	I or O	**Output Clocks with Input Option** Output 6 can alternatively be assigned as two general purpose inputs (GPI0/GPI1) that can be programmed to have any of the input control functions listed in 3.10. GPIO Pins (General Purpose Input or Output) Regardless of whether Output 6 is functioning as a clock output or GPI, the power supply is VDDO3.
OUT6 GPI1	22		
OUT7b	24	O	**Output Clocks** The output clocks can be programmed as single-ended CMOS or differential LVDS, S-LVDS, CML, HCSL or ac-coupled LVPECL and support a programmable signal amplitude and common-mode voltage. Desired output signal format is configurable in CBPro. Termination recommendations are provided in the Si5518/12/10/08 Reference Manual. Unused outputs should be left unconnected.
OUT7	25		
OUT8b	27		
OUT8	28		
OUT9b	30		
OUT9	31		
OUT10b	32		
OUT10	33		

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Table 18. Pin Descriptions (Continued)

Pin Name	Pin Number	Pin Type[1]	Function
OUT11b GPI2	35	I or O	**Output Clocks with Input Option** Output 11 can alternatively be assigned as two general purpose inputs (GPI2/GPI3) that can be programmed to have any of the input control functions listed in GPIO Pin Descriptions. Regardless of whether output 11 is functioning as a clock output or GPI, the power supply will be VDDO5.
OUT11 GPI3	36		
OUT12b	37	O	**Output Clocks** The output clocks can be programmed as single-ended CMOS or differential LVDS, S-LVDS, CML, HCSL or ac-coupled LVPECL and support a programmable signal amplitude and common-mode voltage. Desired output signal format is configurable in CBPro. Termination recommendations are provided in the Si5518/12/10/08 Reference Manual. Unused outputs should be left unconnected.
OUT12	38		
OUT13b	39		
OUT13	40		
OUT14b	42		
OUT14	43		
OUT15b	44		
OUT15	45		
OUT16b	46	O	**Output Clocks with Programmable CMOS Slew Rate** When outputs 16 and 17 are configured as CMOS outputs, they can also have the slew rate adjusted. Because of this they do not support a glitch- less pulsed SYSREF mode. Continuous SYSREF mode is supported.
OUT16	47		
OUT17b	49		
OUT17	50		
Serial Interface			
SDA SDIO	52	I/O	**Serial Data Interface** This is the bidirectional data pin (SDA) for the I2C mode, or the bidirectional data pin (SDIO) in the 3-wire SPI mode, or the input data pin (SDI) in the 4-wire SPI mode. When in I2C mode, this pin must be pulled-up using an external resistor of at least 1 kΩ. No pull-up resistor is needed when in SPI mode.
SCLK	53	I	**Serial Clock Input** This pin functions as the serial clock input for both I2C and SPI modes. When in I2C mode, this pin must be pulled-up using an external resistor of at least 1 kΩ. No pull-up resistor is needed when in SPI mode.
A0 CSb	55	I	**Address Select 0/Chip Select** This pin functions as the hardware controlled lsb of the device address (A0) in I2C mode. In SPI mode, this pin functions as the chip select input (active low). This pin is internally pulled-up and can be left floating if unused.
GPIO3 (A1/SDO)	56	O	**Address Select 1/ Serial Data Output/GPIO3** This input pin operates as the hardware controlled next to lsb portion of the device address (A1) in I2C mode. In 4-wire SPI mode this pin operates as the serial data output (SDO). In 3-wire SPI mode this pin can function as an additional GPIO pin (GPIO3).
Control/Status			
GPIO0	16	I or O	**Programmable General Purpose Input or Outputs** These pins can be programmed to the functions defined in 3.10. GPIO Pins (General Purpose Input or Output)
GPIO1	18		
GPIO2	19		
RSTb	20	I	**Reset Pin** This pin functions as an active-low reset input and is used to generate a device reset when held low for at least the specified Minimum Pulse Width. This resets the device back to a known state and reloads the NVM frequency plan and application. All clocks will stop while the RSTb pin is asserted. If there is no frequency plan in NVM the reset pin will return the device to the bootloader state in which it is waiting for the frequency plan and application to be downloaded by the host controller. This pin accepts a CMOS input and is internally pulled up with a ~20 kΩ resistor to VDDIO. VDDA and VDD18 must be powered up and stable before releasing RSTb. RSTb must not be toggled faster than the maximum update rate (fUR) specification. Please refer to AN1293: Si55xx Schematic Design and Board Layout Guidelines for more details on RSTb pin circuitry.
Power			
VDDIN	1	P	**Input Clock Supply Voltage** Supply voltage 3.3 V, 2.5 V or 1.8 V for the input clock buffers.

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Table 18. Pin Descriptions (Continued)

Pin Name	Pin Number	Pin Type[1]	Function
VDDO1	6	P	**Output Clock Supply Voltage 1 to 7** Supply voltage 3.3 V, 2.5 V, or 1.8 V for outputs. Leave VDDO pins of unused output drivers unconnected. An alternate option is to connect the VDDO pin to a power supply and disable the output driver to minimize current consumption. A 0402 1 µF capacitor should be placed very near each of these pins. VDDO may not exceed VDDA. The banks of outputs are powered as follows: VDDO1 to OUT[0:3] VDDO2 to OUT[4:5] VDDO3 to OUT[6:7] VDDO4 to OUT[8:9] VDDO5 to OUT[10:11] VDDO6 to OUT[12:15] VDDO7 to OUT[16:17] Data sheet jitter performance requires all outputs in a given bank to operate at a single frequency.
VDDO2	13		
VDDO3	23		
VDDO4	29		
VDDO5	34		
VDDO6	41		
VDDO7	48		
VDDA	17	P	**Core Analog Supply Voltage** This core supply can operate from a 3.3 V or 1.8 V power supply for Low-Power Mode. Note that all other supply voltages must be equal or lower voltage than the VDDA pin; so, in Low-Power Mode, no other supply can exceed 1.8 V. A 0402 1 µF capacitor should be placed very near each of these pins.
VDD18	26	P	**Core Supply Voltage 1.8 V** The device core operates from a 1.8 V supply. A 0402 1 µF capacitor should be placed very near each of these pins.
VDD18	51	P	
VDD18	54	P	
VDDIO	57	P	**Control, Status IO Clock Supply Voltage** Supply voltage 3.3 V, 2.5 V, or 1.8 V for the serial interface, control, and status inputs and outputs.
VDDREF	58	P	**Reference Supply Voltage** Supply voltage of 3.3 V or 1.8 V supported for the reference. For best performance, VDDREF should be the same voltage as the VDD_XO or VDD_VCXO.
GND PAD	Package bottom	P	**Exposed Die Attach Pad** The exposed die attach pad (ePAD) on the bottom of the package must be connected to electrical ground.

1. I = Input, O = Output, P = Power

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7. Package Outline

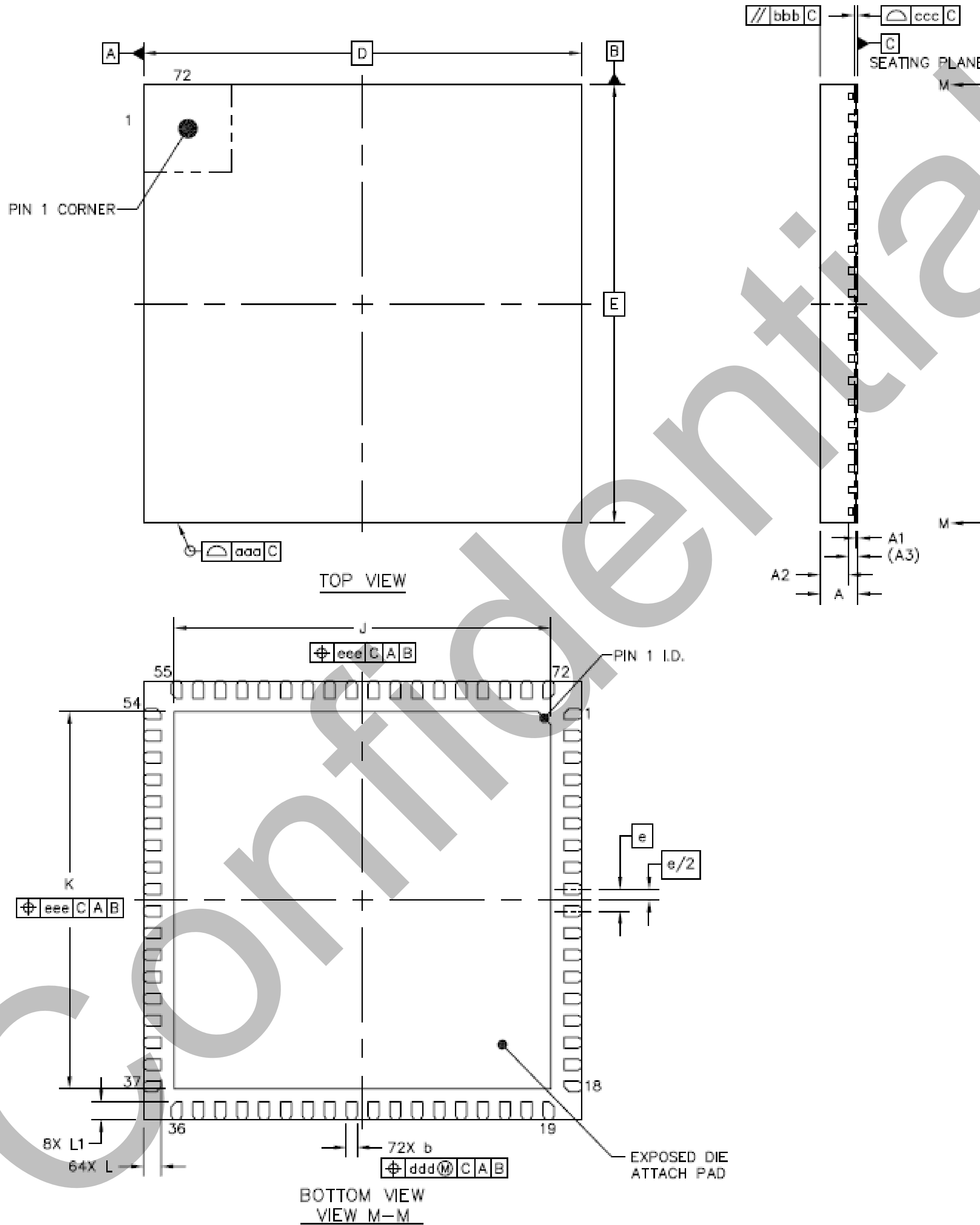

Figure 19. 72-Pin QFN Package

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Table 19. 72-Pin QFN Package Dimensions[1]

		Symbol	Min	Typ	Max
Total thickness		A	0.8	0.85	0.9
Stand off		A1	0	0.035	0.05
Mold thickness		A2	—	0.65	—
L/F thickness		A3		0.203 REF	
Lead width		b	0.2	0.25	0.3
Body size	X	D		10 BSC	
	Y	E		10 BSC	
Lead pitch		e		0.5 BSC	
EP size	X	J	8.5	8.6	8.7
	Y	K	8.5	8.6	8.7
Lead length		L	0.35	0.4	0.45
		L1	0.3	0.4	0.45
Package edge tolerance		aaa		0.1	
Mold flatness		bbb		0.1	
Coplanarity		ccc		0.08	
Lead offset		ddd		0.1	
Exposed pad offset		eee		0.1	
Weight		N/A	—	0.35 g	—

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
Dimensioning and Tolerancing per ANSI Y14.5M-1994.
This drawing conforms to JEDEC Solid State Outline MO-220.

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8. PCB Land Pattern

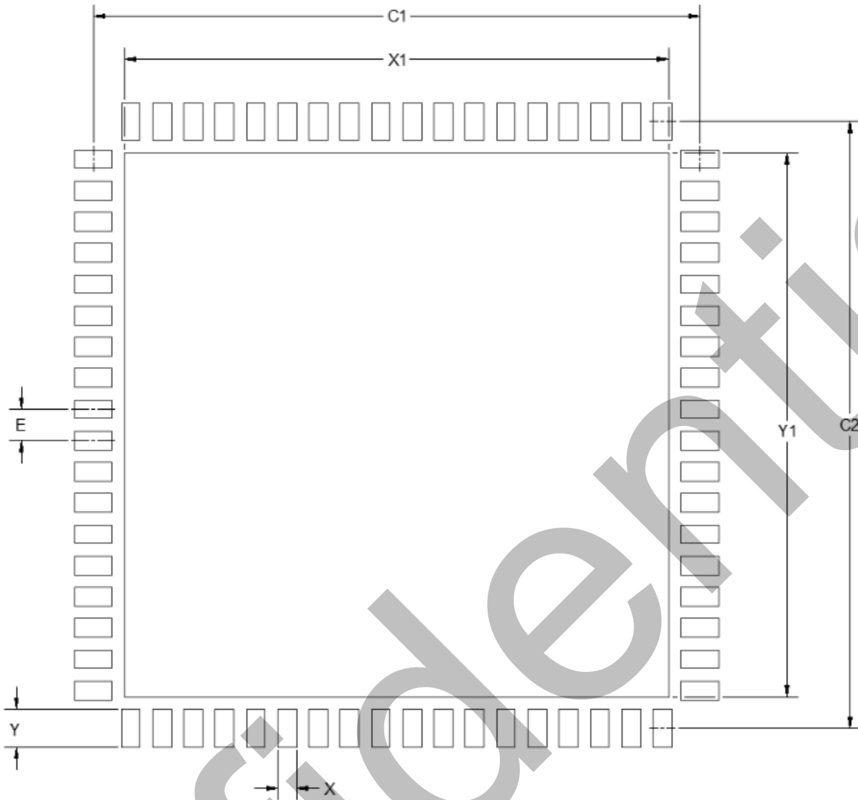

Figure 20. PCB Land Pattern

Table 20. PCB Land Pattern Dimensions

Dimension	mm	Notes
C1	9.70	**General** The notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine tune their SMT process as required for their application and tooling. All dimensions shown are in millimeters (mm). This Land Pattern Design is based on the IPC-7351 guidelines. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm. **Solder Mask Design** All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad. **Stencil Design** A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release. The stencil thickness should be 0.125 mm (5 mils). The ratio of stencil aperture to land pad size should be 1:1 for all pads. A 4x4 array of 1.45 mm square openings on a 2.00 mm pitch should be used for the center ground pad. Card Assembly A No-Clean, Type-3 solder paste is recommended. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.
C2	9.70	
E	0.50	
X	0.30	
Y	0.60	
X1	8.70	
Y1	8.70	

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9. Part Marking

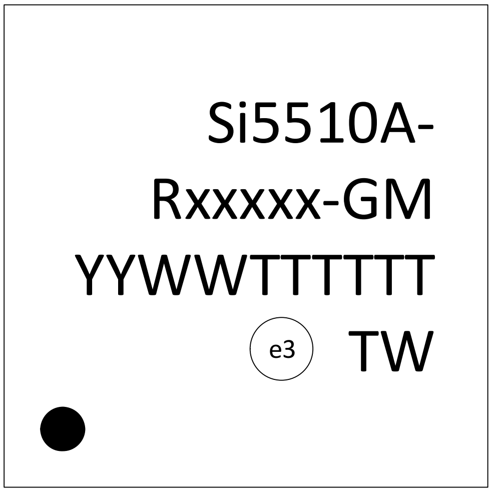

Figure 21. Si5510 Top Marking

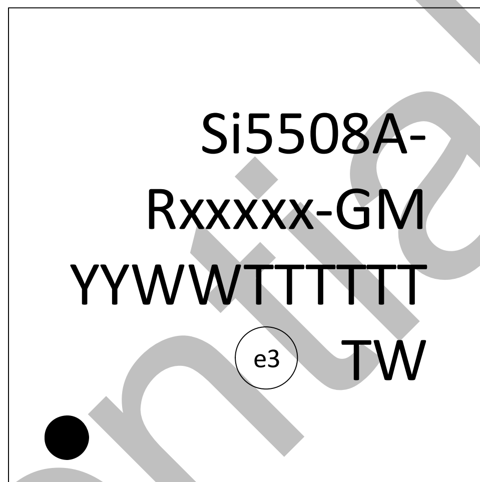

Figure 22. Si5508 Top Marking

Table 21. Top Marking Explanation[1]

Line	Characters	Description
1	Si5510A- or Si5508A-	Base part number and device grade. A = Device Grade.
2	Rxxxxx-GM	R = Product revision. Refer to Ordering Guide. xxxxx = Customer specific NVM sequence number. Optional NVM code assigned for custom, factory pre-programmed devices. Characters are not included for standard, factory default configured devices. -GM = Package (QFN) and temperature range (–40 to +95 °C)
3	YYWWTTTTTT	YYWW = Characters correspond to the year (YY) and work week (WW) of package assembly. TTTTTT = Manufacturing trace code.
4	Circle w/ 0.6 mm (72-QFN) diameter	Pin 1 indicator, left-justified
	e3 TW	Pb-free symbol, center-Justified TW = Taiwan, country of origin (ISO abbreviation)

1. Refer to Ordering Guide for more information.

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10. Revision History

Revision	Date	Description
B	November 8, 2023	Added watermark

A	November 1, 2023	• Minor updates to datasheet template which includes sequential renumbering of all figures and tables as well as typos and text clarifications.
		• Section 1. Feature List
		  o Changed Selectable jitter attenuation bandwidth from 10 Hz to 4kHz to 10Hz to 400Hz.
		• Section 3.3. Inputs
		  o Figure 6. Input structure block diagram
		    ▪ Added PHMON to Input Monitors
		• Section 3.5.3. Slew Rate Limited (SRL) LVCMOS Output
		  o Added last paragraph to incorporate information found in other application notes, Reference Manuals and support documents.
		• Section 3.11 Device Initialization and Reset
		  o Clarified section by added new sentence "All clocks will stop during a hard reset" after sentence "A hard reset is initiated using RSTb pin or through the Device API RESTART command." And referenced "A hard reset is initiated using RSTb pin or through the Device API RESTART command." Referenced the Si5518/12/10/08 Reference Manual as well as AN1360 for more information.
		• Section 3.15 NVM Programming
		  o Fixed typos
		• Section 3.16. Application Programming Interface
		  o Clarified that the secondary serial port only supports SPI 3-wire.
		• Section 3.17 Power Supplies
		  o Replace Si55xx Reference Manual with AN1293 Si55xx Schematic Design and Board Layout Guide.
		• Section 3.17.2 Power Supply Ramp Rate
		  o Added reference to Table 7 for supply voltage ramp rate.
		• 3.17.3 Low Power Mode
		  o Added statement in text as a reminder to customers that NVM programming is not possible in low-power-mode as VDDA must be at 3.3V.
		• Table 4. Electrical Specifications
		  o Replaced Notes 1,2,3 with new Notes 1,2,3,4,5 to match Si5518.
		  o Soldering Time at TPEAK (Pb-free profile) changes to Note 5
		• Table 7. DC Characteristics
		  o Change -0 to -40 to fix typo in conditions at top of table.
		  o Core Supply Current (V_{DD18} + V_{DDA}) Parameter
		    ▪ I_{DD18} Symbol Test Condition
		      • Added note 2 to Si5510/08[1,2]
		      • Deleted Si5510/08 Low Power Mode[2] row
		    ▪ I_{DDA} Symbol Test Condition
		      • Added note 2 to Si5510/08[1,2]
		      • Deleted Si5510/08 Low Power Mode[2] row
		  o Periphery Supply Current Parameter

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A	November 8, 2023	• Added note 2 to Si5510/08[1,2] • Deleted Si5510/08 Low Power Mode[2] row ▪ I_{DDREF} Symbol Test Condition • Added note 2 to Si5510/08[1,2] • Deleted Si5510/08 Low Power Mode[2] row. ▪ Added new Note 2 to table and renumbered remaining Notes o Output buffer supply current (V_{DDOX}) Parameter ▪ Renumbered notes of each test condition for this parameter. o Total Output power dissipation, P_D ▪ Changed Si5510/08 low-power mode[3] to note 3 o Notes at bottom of Table 7. ▪ Updated and added to notes 1, 2, 3, 4 to 1, 2, 3, 4, 5. • Table 8, Input Specifications o Differential (XO/VCXO Applied to REF_IN) ▪ Voltage Swing changed to Note 2 ▪ Slew Rate, added Note 1 and removed Note 4 o Differential (INx/INxb) ▪ Slew Rate, added Note 3 and removed Note 4 o LVCMOS (INx/INxb) ▪ Slew Rate, change to Notes 2 and 5. • Table 12. Differential Clock Output Specifications o Parameter Output Frequency ▪ NA Divider, PPS • Removed Note 3 ▪ NB divider • Removed Note 3 o Parameter Output-to-output skew, Symbol TSK ▪ MultiSynth (NA or NB) outputs, same differential format, same MultiSynth • Removed Note 3 o Parameter Output voltage swing scaling factor OUT16/17, Symbol SF ▪ Added Note 6 o Parameter OUT-OUTb Skew, Symbol TSK_OUT ▪ Expanded Test Conditions portion of table which allowed some specs to be tightened without changing the overall spec Min/Max. o Removed HCSL line items from the following Table 12 Parameter sections and added new HCSL Output Table 13. ▪ Parameter Output Voltage Swing[5], Symbol $V_{OUT.}$ ▪ Parameter Common Mode Voltage, Symbol $V_{CM.}$ ▪ Parameter Differential Output Impedance, Symbol Z_0. o Expanded table for Parameter Rise and Fall Times (20% to 80%) ▪ Added Parameter Rise and Fall Times (20% to 80%) OUT0 - 15, Symbol t_r/t_f • Removed HCSL line items from the following Table 13 Parameter sections and added new HCSL Output Table 14. ▪ Added Parameter Rise and Fall Times (20% to 80%) OUT16 - 17[6], Symbol t_r/t_f

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Revision	Date	Description
A	November 8, 2023	• Outputs 16 and 17 have programmable CMOS Slew Rate so spec tables reflect the Typ and Max for those output types. o Power Supply Noise Rejection[6] ▪ Changed note from note 7 to note 6. o Output-to-Output Crosstalk[7] ▪ Changed note from note 8 to note 7. o Input-to-Output Crosstalk[8] ▪ Changed note from note 9 to note 8. o Note 6 ▪ Removed Note 6 • Removed HCSL line items from Table 13 and added new HCSL Output Table 14. • Renumbered remaining notes. • Table 13. HCSL Clock Output Specifications o Added new Table 13 for HCSL Clock Output Specifications and removed HCSL line items from Table 12 and expanded. • Table 14. LVCMOS Clock Output Specifications o Parameter Output voltage low, Symbol VOL ▪ Changed from Note 4 to Note 3 o Added Note 6 to Parameter Rise and Fall Time (20% to 80%) [4,5,6] o Added new Note 6 to the Notes section • Table 17. Performance Characteristics o Added statement to Note 6 to clarify ▪ "after the output phase has achieved a steady state value." o Updated Note 10 to clarify based on new ClockBuilder Pro Spur Analysis tool which helps customers analyze added jitter and spurs due to cross talk. • Table 19. Pin Descriptions o Pin Name: RSTb, Pin: 20, Pin Type: I ▪ Added addition text on RSTb operation incorporating information found in other application notes, Reference Manuals and other Si5518 support documents. o Pin Name: XV pin 62 and Input clock pins 65 through 72. ▪ Reference AN1293 Si55xx Schematic Design and Board Layout Guide instead of Si5518/12/10/08 Reference Manual. o Pin Names INx – INxb, pins 65 through 72, Pin Type: I ▪ Added AN1293: Si55xx Schematic Design and Board Layout Guide in addition to the Si5518/12/10/08 Reference Manual. • Table 22. Top Marketing Explanation o Line: 2, Characters: Rxxxxx-GM ▪ Fixed typo on temperature range from -40 to +85C to 40 to +95C.
1.0	July 2022	Initial release.

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DATA SHEET

Si5512: NetSync™ Low-Phase-Noise, Jitter-Attenuating Clock for 5G/eCPRI/SyncE/IEEE 1588

The Si5512 is a 12-output variant of the 18-output Si5518 device. The Si5512 fully supports all of the network synchronization functionality of the Si5518 but does not support some RF functionality, such as a VCXO phase noise reference or OSYNC for JESD204B/C Subclass 2. The Si5512 is intended to support wireless network synchronization applications that split digital and RF functions onto separate PCBs. Split-board applications, such as massive MIMO, require an Si5512 network synchronizer on the digital board followed by an RF jitter attenuator or buffer for each of the RF cards residing on physically separated boards.

The Si5512 may also be combined with optional AccuTime™ IEEE 1588 software offering a complete IEEE 1588v2 solution for phase and frequency synchronization. AccuTime 1588 software consists of a unique servo algorithm paired with a protocol stack that runs on the host processor.

The RFPLL generates high performance low phase noise CPRI clocks for wireless remote radio heads (RRH). Each of the 12 clock outputs are configurable in any combination of DCLK, SYSREF, or other system clocks. Each DSPLL® is a fully featured network synchronization phase-locked loop with adjustable DCO for IEEE 1588 Ethernet front haul synchronization.

Applications

- LTE-A and 5G Remote Radio Units (RRU)
- JESD204B/C clock generation
- IEEE1588 slave clocks (T-TSC), Telecom-Boundary Clocks (T-BC)
- IEEE1588 assisted partial timing support clocks (T-BC-A, T-TSC-A), partial timing support (T-BC-P, T-TSC-P)
- IEEE 1588 Grandmaster clocks (T-GM)
- Remote Access Network (RAN), picocells, small cells
- Remote Radio Head (RRH), wireless repeaters, mobile front haul and back haul

Key Features

- Utilizes fifth-generation DSPLL and MultiSynth™ technologies
- Ultra high-performance clock generation for LTE-A and 5G RRUs with IEEE 1588/SyncE
- Optional AccuTime IEEE 1588 software
- Integer output frequencies up to 1.2288 GHz
- Fractional output frequencies up to 650 MHz
- JESD204B/C clock generation (DCLK/SYSREF) with synchronization across multiple devices
- Programmable delay at each output
- Ultra-low jitter: 47 fs RMS typical
- Phase noise:
  - Noise floor –164 dBc/Hz at 491.52 MHz
  - –145 dBc/Hz at 800 kHz offset for a 491.52 MHz carrier frequency
- Spurs < –95 dBc at 122.88 MHz
- Support IEEE1588 with DCO adjustable at 1 ppt resolution
- Locks to 1PPS and PP2S
- Full suite of status monitors
- Supports ITU-T G.8273.2 (T-TSC, T-BC), ITU-T G.8273.4 (T-BC-P, T-BC-A, T-TSC-P, T-TSC-A), G.8262 (EEC Options 1 and 2), G.8262.1 (eEEC), G.8261 (TC12-17), and PRTC (T-GM)
- Low-power mode
- 72 QFN 10 x 10 mm, 6 inputs, 12 outputs
- AccuTime IEEE 1588 Software
  - Field tested and proven with compliance reports available
  - Demo platform support
  - O-RAN compatible
  - IEEE 1588 servo loop and protocol stack software runs on host processor

Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to *Skyworks Definition of Green™*, document number SQ04–0074.

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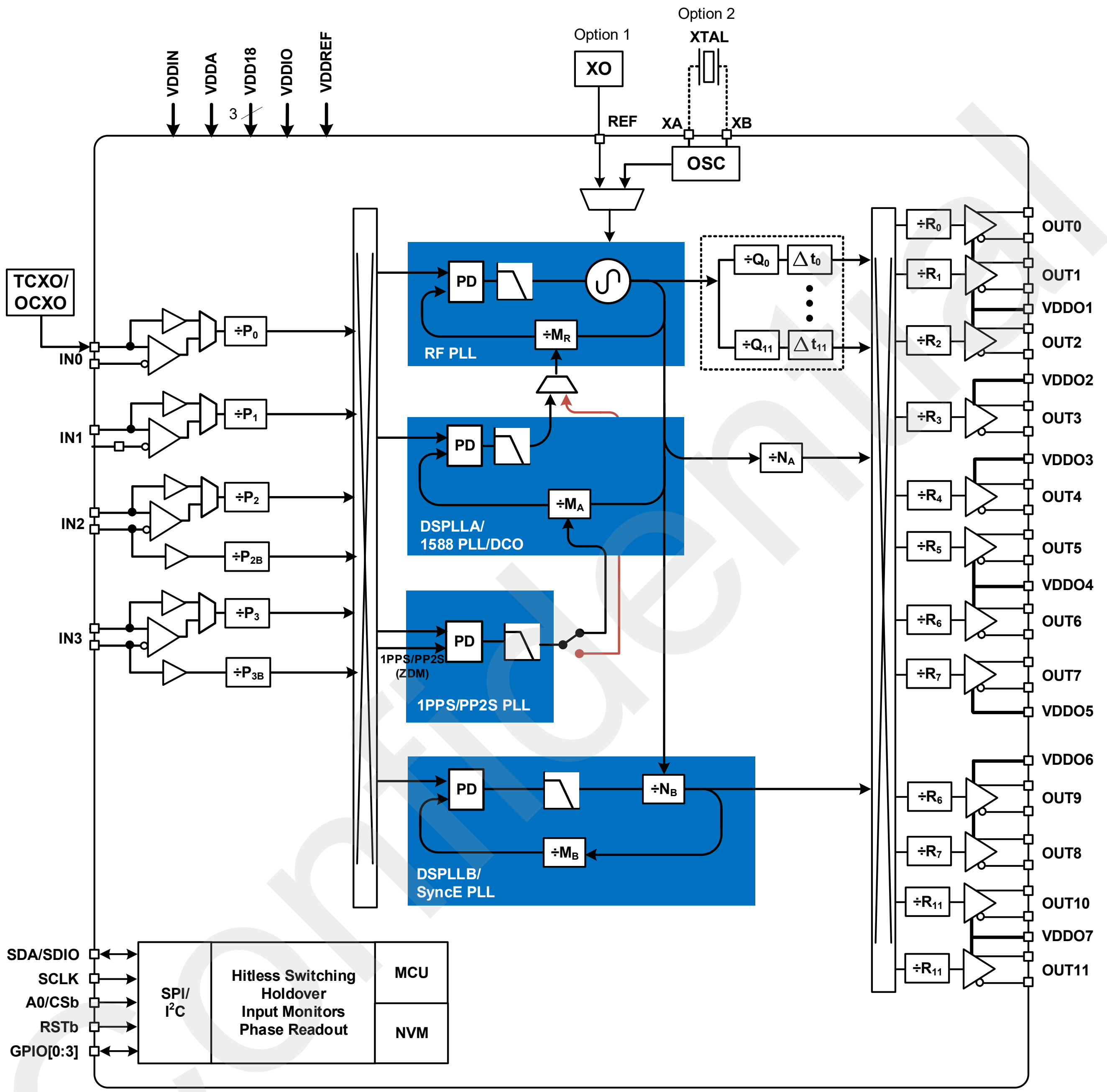
Option 1
Option 2
XO
XTAL
VDDIN
VDDA
VDD18
VDDIO
VDDREF
3
REF
XA
XB
OSC
TCXO/
OCXO
IN0
IN1
IN2
IN3
÷P0
÷P1
÷P2
÷P2B
÷P3
÷P3B
PD
RF PLL
÷MR
÷Q0
Δt0
÷Q11
Δt11
DSPLLA/
1588 PLL/DCO
÷MA
÷NA
1PPS/PP2S
(ZDM)
1PPS/PP2S PLL
÷NB
÷MB
DSPLLB/
SyncE PLL
÷R0
÷R1
÷R2
÷R3
÷R4
÷R5
÷R6
÷R7
÷R11
OUT0
OUT1
VDDO1
OUT2
VDDO2
OUT3
VDDO3
OUT4
OUT5
VDDO4
OUT6
OUT7
VDDO5
VDDO6
OUT9
OUT8
OUT10
VDDO7
OUT11
SDA/SDIO
SCLK
A0/CSb
RSTb
GPIO[0:3]
SPI/
I2C
Hitless Switching
Holdover
Input Monitors
Phase Readout
MCU
NVM

1. Feature List

NOTE: Specifications given on this page are for reference only. Refer to "4. Electrical Specifications" on page 29 for device performance.

- RFPLL
  - Supports JESD204B/C Subclass 0, 1
  - Ultra-low Phase Noise (example at 491.52 MHz carrier):
    - –164 dBc/Hz noise floor
    - –145 dBc/Hz at 800 kHz offset
  - Ultra-low jitter performance:
    - <50 fs typ XO (12 kHz to 20 MHz at 491.52 MHz)
    - Selectable jitter attenuation bandwidth: 10 Hz to 400 Hz Dual Reference JA.
- DSPLL A, DSPLL B
  - Independent network synchronization DSPLLs
  - Supports ITU-T G.8273.2 (T-TSC, T-BC), ITU-T G.8273.4 (T-BC-P, T-BC-A, T-TSC-P, T-TSC-A), and PRTC (T-GM)
  - Programmable loop bandwidth: 1 mHz to 4 kHz
  - Automatic Free-Run, Holdover, and Locked modes
  - Hitless input clock switching: automatic or manual with < 150 ps phase transient
- PPSPLL
  - Instant lock for 1PPS/PP2S
  - Programmable loop bandwidth 1 mHz to 25 mHz
  - Programmable phase slope limiting (PSL) and phase pull-in rate (PPI)
- 12 Programmable Clock Outputs:
  - JESD204B/C DCLK or SYSREF. Up to six DCLK/SYSREF pairs
  - Integer Q dividers: PP2S/1PPS to 1.2288 GHz
  - JESD204B/C SYSREF Pulser Mode
  - Multisynth Fractional Dividers: PP2S/1PPS to 650 MHz
  - Output-to-Output Static Delay: ±10 ns
  - Output-output skew: ±50 ps
  - LVDS, S-LVDS, AC coupled LVPECL, LVCMOS, Slew Rate Limited (SRL) LVCMOS, HCSL, CML
- Utilizes fifth-generation DSPLL and MultiSynth technologies
- Zero Delay Mode for all PLLs
- 4/6 clock inputs:
  - Differential: 8 kHz to 1 GHz
  - CMOS: 1PPS, PP2S, 8 kHz to 250 MHz
- Status monitoring (LOS, OOF, PHMON, FLOL and PLOL)
- Automatically generates free-running clocks at power up
- Automatically locks to a valid clock input
- Automatic Holdover Mode
- Core voltage: 3.3 V, 1.8 V
- Output driver supply voltages (VDDO): 3.3 V, 2.5 V, 1.8 V
- Serial Interface: I^{2}C or SPI (3 or 4-wire)
- ClockBuilder® Pro software tool simplifies device configuration
- Package: 72-Lead QFN, 10 x 10 mm
- Extended temperature range:
  - –40 to +95 °C ambient
  - –40 to +105 °C board
- Pb-free, RoHS compliant

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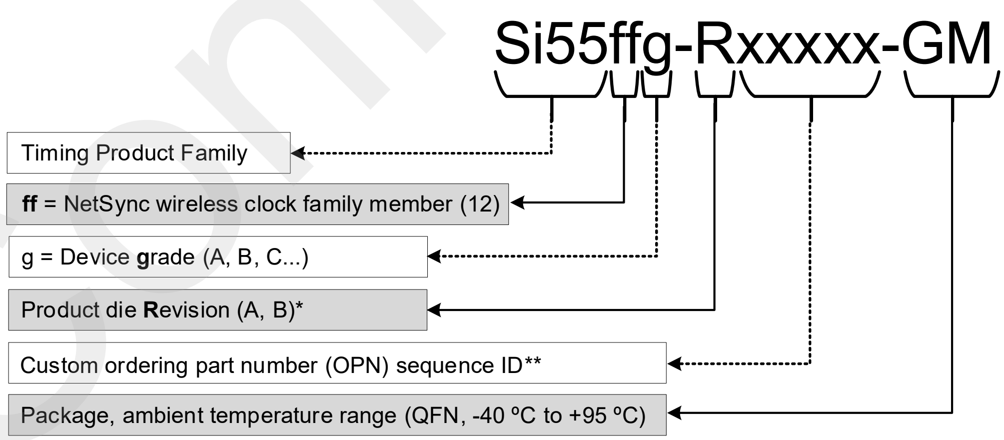
2. Ordering Guide

Table 1. Si5512 Ordering Guide

Ordering Part Number (OPN)[1,2,3]	Number of DSPLLs	Number of Outputs	Serial Interface	AccuTime IEEE 1588 Software Support[4]	Package	Temperature Range
Si5512A-Bxxxxx-GM	1-RFPLL, 2-DSPLL	12	SPI 4–wire or 3–wire	No	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient[5]
Si5512B-Bxxxxx-GM	1-RFPLL, 2-DSPLL	12	SPI 4–wire only	Yes	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient[5]
Si5512C-Bxxxxx-GM	1-RFPLL, 2-DSPLL	12	I^2C	No	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient[5]
Si5512D-Bxxxxx-GM[6]	1-RFPLL, 2-DSPLL	12	SPI 4–wire only	Yes	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient[5]
Si5512E-Bxxxxx-GM[6]	1-RFPLL, 2-DSPLL	12	SPI 4–wire only	Yes	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient[5]
Si5512P-Bxxxxx-GM[6]	1-RFPLL, 2-DSPLL	12	SPI 4–wire or 3–wire	No	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient[5]
Si5512Q-Bxxxxx-GM[6]	1-RFPLL, 2-DSPLL	12	SPI 4–wire or 3–wire	Yes	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient[5]
Si5512R-Bxxxxx-GM[6]	1-RFPLL, 2-DSPLL	12	I^2C	No	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient[5]
Si55xx-A-EVB	1-RFPLL, 2-DSPLL	12	—	No	Evaluation Board	—
Si5518-A-FMC-EVB[7]	—	—	—	Yes	FPGA Mezzanine Card (FMC)	—

1. Add an "R" at the end of the OPN to denote tape and reel ordering options.
2. Custom, factory preprogrammed devices are available as well as unconfigured base devices. See Figure 1 for 5-digit numerical sequence nomenclature.
3. Revision B will be the device qualified for mass production and loose samples.
4. AccuTime IEEE 1588 software is only supported on certain part grades. Use this table to determine which grades support AccuTime.
5. Ambient temperature of 95 °C may not be possible with all configurations. This is dependent on device configuration. Tj cannot exceed a max of 125 °C.
6. Grades D, E, P, Q, and R are reserved for special applications. See ClockBuilder Pro for details.
7. The Si5518-A-FMC ships with 10GBASE-SR SFP+ transceivers, optical cable along with the required software on an SD card. FMC requires a customer-provided AMD ZCU102, ZCU111 or ZCU216 or ZCU670 FPGA evaluation board. FMC is only for AccuTime evaluation. Customers using the Si5512 should use the Si5518-A-FMC to evaluate AccuTime IEEE 1588 software.



* See Ordering Guide table for current product revision.
** 5 digits; assigned by ClockBuilder Pro for Custom OPN devices.

Figure 1. Si5512 Ordering Guide Diagram

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3. Functional Description

The Si5512 combines a high-performance JESD204B/C compatible RF clock jitter attenuator and two fifth-generation DSPLLs supporting SyncE/IEEE1588 network synchronization. This provides a highly-integrated synchronization solution for wireless applications where both IEEE 1588 and JESD204B/C clock generation are needed. Only a few external components are required for a complete synchronization function. The RFPLL and DSPLLs can operate from an external XO or fixed frequency crystal (XTAL). Both the DSPLLs and RFPLL support Locked, Free-Run, and Holdover modes of operation with an optional DCO Mode for IEEE 1588 applications. An optional external TCXO or OCXO provides frequency accuracy and stability for Free-Run and Holdover modes. This is referred to as Dual-Reference Mode. The RFPLL is locked to the OCXO/TCXO but is also modulated by the input to DSPLLA. See "3.10. External Reference Clocks (XA/XB, REF_IN)" on page 15 for more details. There are four differential/single-ended inputs available to synchronize any of the phase-locked loops. Two of the inputs (IN2, IN3) can be configured as dual single-ended inputs in applications where more than four inputs are required. Input selection can be manual or automatically controlled using an internal state machine. Any of the 12 output clocks (OUT0 to OUT11) can be sourced from any of the PLLs using a flexible crosspoint connection.

There is an additional PPSPLL that can be used for synchronization to a 1PPS/PP2S input. If the application uses AccuTime SW, then the 1PPS from GNSS should instead be timestamped by the host controller in order to have the GNSS assist the PTP servo for smooth transitions when the GNSS is lost and again recovered.

Skyworks offers a comprehensive IEEE 1588 solution for applications in a centralized "pizza box" or "split board" architectures. It consists of three components: An IEEE 1588 protocol stack, a packet synchronizer servo algorithm (or "servo"), and the Si5512 network synchronizer clock. The IEEE 1588 stack receives Ethernet packets from the host processor MAC, processes IEEE 1588 packets, and sends time stamp data to the IEEE 1588 servo algorithm implemented on the host. The servo statistically processes the time stamps and adjusts a 1588 system clock that runs the Time of Day (ToD) counter in the host.

The Si5512 is commonly used in a "split board" application. A split board application consist of a digital base band board (PHY, ToD, network processor, the Si5512 network synchronizer clock) and a second RF board containing the ADCs/DACs which are clocked by a wireless jitter attenuator such as the Si5510/08 or Si5386.

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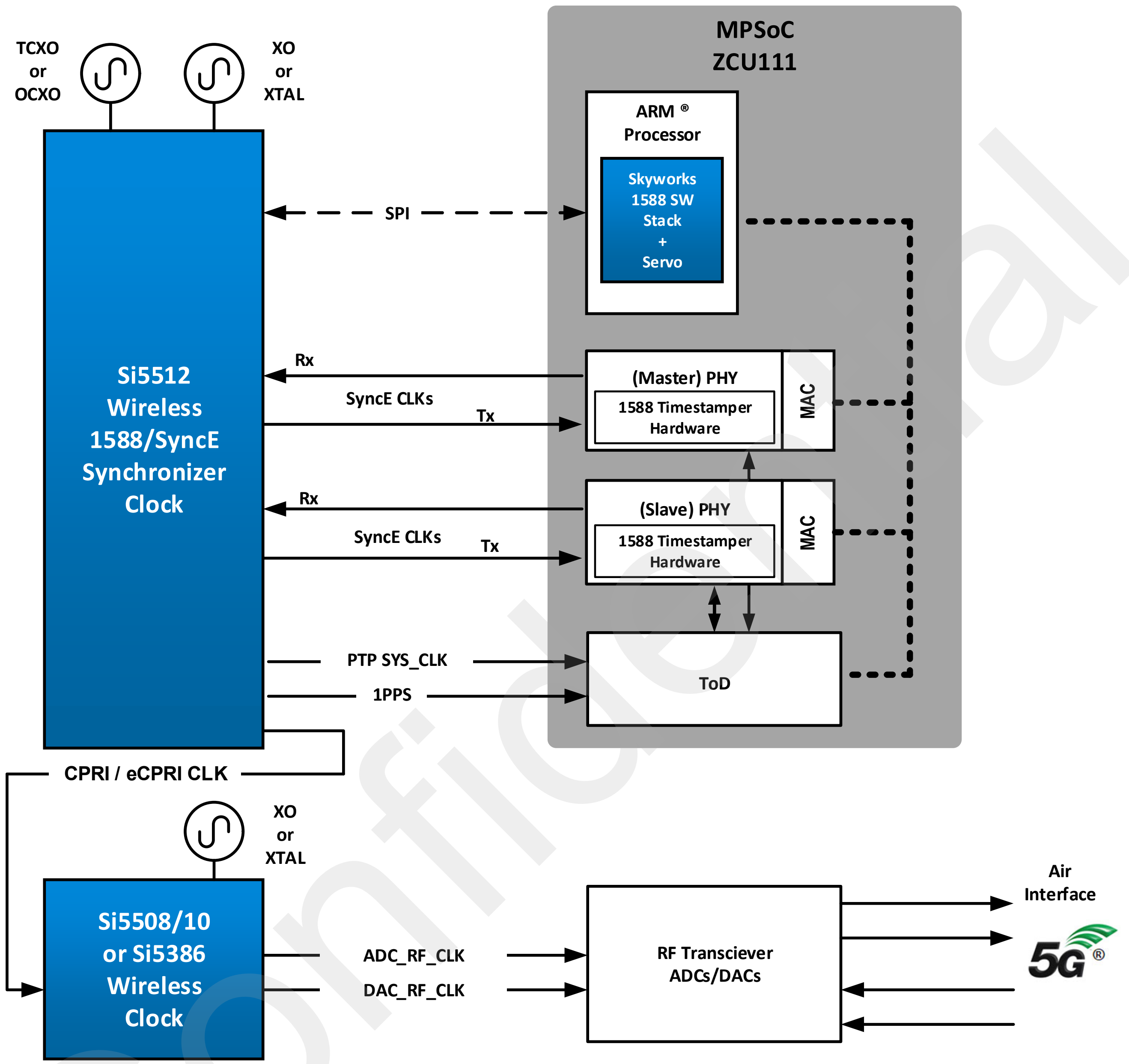

Figure 2. Si5512 IEEE1588 Demo Platform

3.1. Frequency Configuration

The frequency configuration of the DSPLL is programmable through the serial interface and can also be stored in non-volatile memory. The combination of input dividers (P), fractional frequency multiplication (M), integer output division (Q), fractional output division (N), and integer output division (R) allows the generation of virtually any output frequency on any of the outputs. All divider values for a specific frequency plan are easily determined using the ClockBuilder Pro utility.

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3.2. DSPLL Loop Bandwidth, Initial Lock, and Fast Lock Settings

The DSPLL loop bandwidth determines the amount of input clock jitter attenuation. Each DSPLL has a configurable loop bandwidth. The DSPLL will always remain stable with low peaking regardless of the loop bandwidth selection.

Each of the DSPLLs, and the PPSPLL have configurable loop bandwidths. There are three configurations, each with a separate setting for the loop bandwidth:

- **Initial Lock Bandwidth**—The PLL uses this bandwidth when it exits Free-Run Mode and attempts to lock to a new input clock.
- **Loop Bandwidth**—This sets the bandwidth of the PLL once lock to an input is achieved.
- **Fastlock Bandwidth**—This sets the bandwidth of the PLL when exiting from holdover.
  - Selecting a low DSPLL loop bandwidth will generally lengthen the lock acquisition time. The Fastlock feature allows setting a temporary Fastlock Loop Bandwidth that is used during the lock acquisition process. The DSPLL will revert to its normal loop bandwidth once lock acquisition has completed.

See the "Si5518/12/10/08 Reference Manual" and ClockBuilder Pro for more information, recommendations, and limits for setting PLL loop bandwidths for different configurations.

3.3. Inputs

There are four differential inputs which can also be configured as single-ended CMOS inputs. Both IN0 and IN1 can support a single CMOS input, while IN2 and IN3 can be configured as dual CMOS inputs. This allows support for up to six CMOS inputs, or any combination of differential and CMOS inputs.

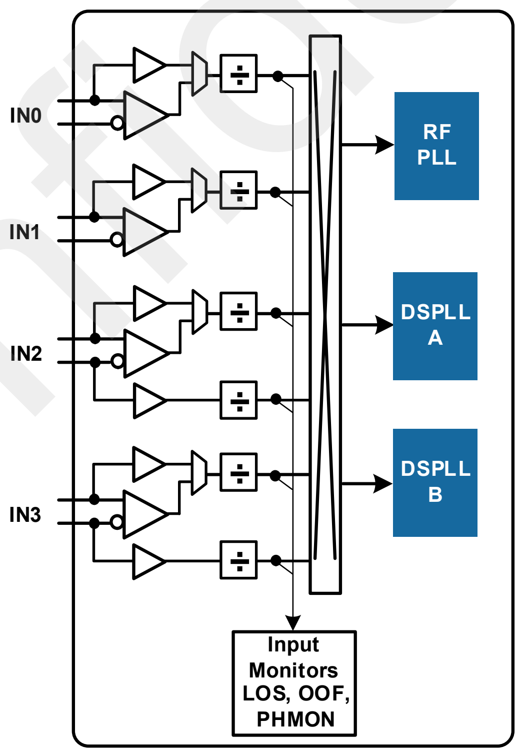

Figure 3. Input Structure

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3.3.1. Input Terminations

Refer to "AN1293: Si55xx Schematic Design and Board Layout Guidelines" and the "Si5518/12/10/08 Reference Manual" for guidance on input terminations.

3.3.2. Input Selection

Input selection for any of the PLLs can be controlled manually through pin control, API command, CLI command, or automatically using an internal state machine.

3.3.2.1. Input Divider

The device utilizes both fractional and integer input (P) dividers to lock to any frequency input clock. The ClockBuilder Pro software will choose the optimal divide values based on the user-defined frequency plan. Each input divider (P0, P1, P2, P2b, P3, and P3b) can be configured independently of the others.

3.3.2.2. Manual Input Selection

In Manual Mode, the input selection is made by defining a GPIO pin as an input select pin and changing the input pin voltage level, or by writing an API or CLI command. Any of the inputs are available to any of the PLLs through a crosspoint input selection switch. If there is no clock signal on the selected input, or if the input is not valid due to LOS/OOF/PHMON input alarms, the PLL will automatically enter Free-Run/Holdover Mode. This applies to both the DSPLLs, RFPLL, and the PPSPLL.

3.3.2.3. Automatic Input Selection

When configured in this mode, each of the PLLs automatically selects a valid input that has the highest configured priority. The priority scheme is independently configurable for each PLL and supports revertive or non-revertive selection. All inputs are continuously monitored for loss of signal (LOS), invalid frequency range (OOF), and phase (PHMON). Only valid inputs that have no LOS, OOF or phase monitor (PHMON) alarms can be selected for synchronization by the automatic state machine. The PLL(s) will enter Free-Run or Holdover Mode if there are no valid inputs available.

3.3.3. Unused Inputs

Unused inputs should be configured as "Unused (Powered Down)", and the pins may be left unconnected or ac-coupled to ground. See "AN1293: Si55xx Schematic Design and Board Layout Guidelines" and the "Si5518/12/10/08 Reference Manual" for recommendations on how to minimize system noise on any CMOS input and or any differential input configured as "Enabled" but not actively being driven by a clock.

3.3.4. Phase Readout (PHRD)

The Phase Readout Device API can be used to read and measure the phase between multiple input clocks to the Si5512. Unused inputs that are not assigned to a DSPLL can also be configured as phase readout (PHRD) or phase readout feedback (PHRD_FB) inputs. These inputs can be used to measure the phase of an output of the Si5512 to the input(s) of known phase. PHRD and PHRD_FB inputs use the same alarms, such as LOS/OOF/PHMON, as the other clock inputs, but they are not assigned to a DSPLL.

3.4. Input Clock Switching

Clock inputs applied to the Si5512 can be either from the same source (0ppm, same nominal frequency) or different sources (non-0ppm, different nominal frequencies). The Si5512 automatically determines the optimal switching mode depending on the nominal frequency difference between the clocks at the time of the switch. When switching between 0ppm inputs, the Si5512 performs either a hitless switch with phase buildout (PBO) or a phase pull in (PPI) switch depending on the user selection in ClockBuilder Pro. When the input clocks have a non-0 ppm offset, the Si5512 performs a frequency-ramped input switch. Automatic input clock switching is not available for PPSPLL.

Refer to the "Si5518/12/10/08 Reference Manual" for additional guidance on input clock switching modes. All input clock switches are glitchless meaning there will be no runt pulses generated at the output during the transition.

3.4.1. Hitless Input Switching for 0 ppm Clocks—Phase Buildout (PBO)

Applications like SyncE/eCPRI require that transients are kept to a minimum when switching between input clocks. Hitless switching with phase buildout (PBO) is a feature that prevents a transient from propagating to the output when switching between two clock inputs that have a fixed phase relationship. A hitless switch can only occur when the two input frequencies are frequency locked, meaning that the nominal frequencies are the same (0 ppm). Due to the nature of hitless switching, the input-to-output delay of the PLL is not preserved. The DSPLL simply absorbs the phase difference between the two input clocks during an input switch. The phase buildout feature supports clock frequencies down to a minimum input frequency of 8 kHz.

3.4.2. Phase Pull-In (PPI) Input Switching for 0 ppm Clocks

In some applications, the output phase must track the input phase with minimal delay. This is particularly common in applications which require synchronization to an external 1PPS such as a GNSS receiver or traditional CPRI front haul clocking. When the application requires the input-to-output delay to be preserved after clock switching, the phase pull-in clock switching mode should be selected. In this mode, the output phase will be pulled in at a user-programmable ramp rate referred to as the PPI slope (ns/s). With phase pull-in switching, the output phase always aligns with the newly selected input. PPI is always enabled for Zero-Delay Mode and PPSPLL applications.

3.4.3. Ramped Input Switching for Non-0 ppm Clocks

The ramped switching feature allows the DSPLLs to switch between two input clock frequencies that have a non-0 ppm offset without an abrupt frequency transient at the output. When the two input clock frequencies are not the same nominal frequency, the DSPLL will pull in the frequency difference between inputs at the ramp rate that is programmable in ClockBuilder Pro from ppb/s to ppm/s. The loss-of-lock (LOL) and the LOOP_FILTER_RAMP_IN_PROGRESS indicators (accessible through the Device API) will assert while the DSPLL is ramping to the new clock frequency.

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3.5. Outputs

The Si5512 supports 12 differential output drivers configurable as ac-coupled LVPECL, LVDS, S-LVDS, CML, HCSL, LVCMOS, or SRL LVCMOS. When in LVCMOS Mode, the differential pair becomes two single-ended outputs for a maximum of 36 possible outputs. Two of the output drivers (OUT10 and OUT11) have slew rate control when in LVCMOS Mode. This allows limiting the rise time of the output signal to reduce the possibility of crosstalk to adjacent output drivers. The outputs have power supply pins (VDDOx) for output driver groups of 3-1-1-2-1-2-2, which can be individually powered by 3.3, 2.5, or 1.8 V. The LVCMOS output voltage is set by the VDDOx pin. Refer to “7. Pin Descriptions” on page 47.

3.5.1. Output Crosspoint

A crosspoint allows any of the output drivers to connect with any of the PLLs. A digital output delay adjustment is possible on each of the Q divider outputs for JESD204B/C applications. The static delay adjustments are programmable and may be stored in NVM so that the desired output configuration is ready at power up.

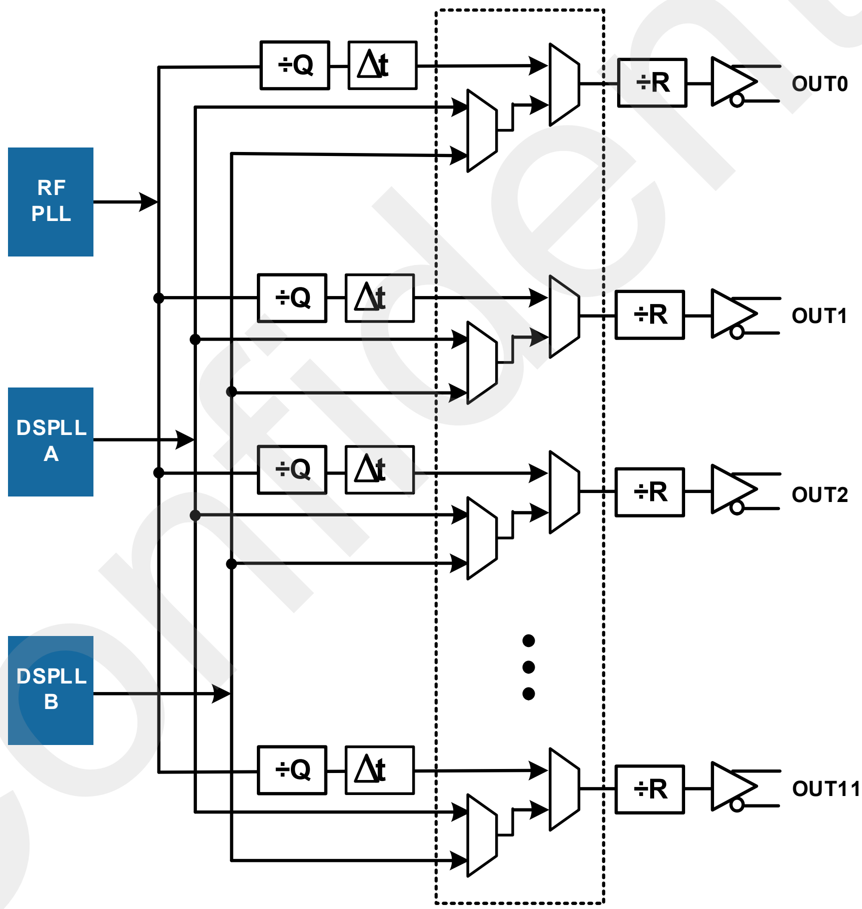

Figure 4. Output Structure

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3.5.2. Differential and LVCMOS Output Terminations

Refer to "AN1293: Si55xx Schematic Design and Board Layout Guidelines" and the "Si5518/12/10/08 Reference Manual" for guidance on output terminations.

3.5.3. Slew Rate Limited (SRL) LVCMOS Outputs

The swing of LVCMOS and SRL LVCMOS outputs is rail-to-rail; so, the swing is determined by the voltage of the corresponding VDDO pin of the LVCMOS or SRL LVCMOS output. Each output driver configured as LVCMOS or SRL LVCMOS has two outputs, OUTx/OUTxb. The polarity of each of the two outputs may be independently configured as a non-inverted or inverted output as well as enabled or disabled.

OUT10/10b and OUT11/11b may be configured as SRL LVCMOS outputs, which have a programmable slew rate and generate significantly less crosstalk than conventional LVCMOS outputs. Less crosstalk than conventional CMOS outputs is useful in jitter-critical applications.

SRL LVCMOS output clocks on OUT10/10b and OUT11/11b are intended only for low frequency clock applications. Refer to the "Si5518/12/10/08 Reference Manual" for the maximum Fout supported for each slew rate selection.

3.5.4. Output Enable/Disable

Each output driver may be enabled/disabled through programmable GPIO pins. There are two output enable groups, OE0 and OE1, which are logically ORd together to determine which outputs are enabled at any point in time. ClockBuilder Pro allows the control and selection of the GPIO pin mapping to the outputs.

Outputs may also be enabled/disabled using the device API. If an output is assigned as GPIO controlled, it cannot be controlled via the API. The API controlled output enable allows for more flexibility than the GPIO control as any of the outputs can be individually enabled/disabled via an API command.

The default output enable/disable behavior is a glitchless enable/disable. For clocks to start or stop as soon as possible, accepting runt pulses or glitches, instant output enable/disable can be used.

3.5.5. State of Disabled Output

The disabled state of an output driver may be configured as stop high, stop low, or Hi-Z. CMOS outputs less than 2 MHz can also be configured as Hi-Z with weak pull-up/pull-down.

Differential outputs, when disabled, will maintain the output common-mode voltage even while the output is not toggling. This minimizes disturbances when disabling and enabling clock outputs.

3.5.6. Output Dividers

The device utilizes both integer Q dividers and fractional NA, NB MultiSynth output dividers. The ClockBuilder Pro software chooses the optimal divide values based on the user-defined frequency plan.

The following list summarizes each class of divider:

1. Output Q Divider: Q0–Q11
   - Integer Only Divide Value
   - Open loop divider taps directly off VCO

2. DSPLL A/B Feedback M Divider: MA, MB
   - Integer or Fractional Divide Value

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3. Output N Divider: NA, NB
- MultiSynth Divider, Integer or Fractional Divide Value

4. Output Divider: R11–R0
- Integer Only Divide Value

5. Synchronized Dual Outputs
- If one N divider is used in a closed loop fashion and the other N divider is used in an open loop fashion, the dividers may be cascaded so that the output of each N-divider is derived from the same input clock source and is capable of having a fractional frequency relationship.

3.5.7. Output Skew Control

Output skew control allows outputs that are derived from the Q dividers to be phase adjusted in steps of 1/fvco or 1/(4*fvco) when the fine adjust is enabled. The exact skew adjustment and step sizes are reported on the Output Skew Control Tab of the ClockBuilder Pro Wizard.

3.6. RFPLL

The RFPLL controls the central VCO which provides many of the essential functions for the device such as generating ultra-low phase noise JESD204B/C clocks and maintaining free-run accuracy and holdover stability for all PLLs (RFPLL, DSPLLA, DSPLLB, PPSPLL). It operates using one of many external frequency sources. In Single-Reference Mode, a simple low-cost fixed frequency crystal (XTAL) provides the phase noise reference and the RFPLL locks to a clock input for jitter attenuation. The option of using a crystal oscillator (XO) is also available. In Dual-Reference Mode, the RFPLL locks to a TCXO or OCXO in addition to the fixed frequency oscillator. Dual-Reference Mode should be used for applications that require low phase noise and highly stable holdover and free-run accuracy output clocks. The benefits and trade-offs of these configurations are covered in the “Si5518/12/10/08 Reference Manual” and ClockBuilder Pro.

3.6.1. JESD204B/C Clock Generation

The RFPLL generates ultra-low phase noise JESD204B/C clocks for Subclass 0 and Subclass 1 operation. Any of the 12 clock outputs can be assigned to generate JESD204B/C output clocks.

JESD204B/C Subclass 1 support is provided with assignable SYSREF/DCLK timing skew, as well as with a SYSREF pulser that supports JESD204B/C “gapped” periodic outputs.

Static delay is assignable with a step size down to 1/4 x VCO period (approximately 20 ps). Exact delay is reported in ClockBuilder Pro.

Each SYSREF output can be configured in Continuous Mode. SYSREFs in Continuous Mode may cause crosstalk with adjacent DCLK outputs. If using SYSREF in Continuous Mode, a gap of one unused output is recommended between SYSREF and DCLK.

The SYSREFs can also be configured in pulsed mode. The SYSREF pulser provides 1, 2, 4, 8, 16, or 32 pulses on user request, with the SYSREF held static between requests. SYSREFs in Pulsed Mode will not couple with other channels since for the majority of operation they are disabled. A gap or unused output between DCLK and SYSREF is not necessary in Pulsed Mode. Each SYSREF can be independently assigned as Continuous or Pulsed Mode with the desired number of pulses in ClockBuilder Pro. A common SYSREF pulse request for all pulsed SYSREF outputs can be initiated either by a rising edge on assignable digital input SRCREQ, or by using the JESD_SYSREF_PULSER API via the serial interface.

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3.7. DSPLL (DSPLL A, DSPLL B)

In general, both DSPLLs have identical performance and flexibility and can be independently configured and controlled through the serial interface. Each of the DSPLLs support Locked, Free-Run, and Holdover modes of operation with an optional DCO Mode for IEEE 1588 applications. The DSPLLs share the stability from the OCXO/ TCXO applied to the RFPLL in Dual Reference Mode in order to support Free-Run and Holdover modes.

DSPLL A also has the option of modulating the RFPLL in Dual Reference Mode to train all clock outputs to the SyncE or IEEE 1588 rate.

3.7.1. DCO Mode

The DCOs in each of the DSPLLs can be frequency controlled in predefined steps ranging from <1 ppt to several ppm. This is a useful feature for IEEE 1588 applications. The DCOs can be controlled when its DSPLL is locked to an external SyncE input (Hybrid SyncE + PTP Mode) or when it's in Free-Run/Holdover Mode. The frequency adjustments are controlled through the serial interface by triggering a Device API command or by pin control using frequency increments (FINC) or decrements (FDEC). Both the FINC and FDEC pins are available through the configurable GPIO pins. Each DSPLL can be assigned to the FINC and FDEC pins. A FINC will add the frequency step word to the DSPLL output frequency, while a FDEC will decrement it. Step sizes are configured in ClockBuilder Pro.

3.8. Zero Delay Mode (ZDM)

Zero Delay Mode (ZDM) is a mode of PLL operation in which more accurate input-to-output phase delay can be achieved by providing an external feedback from one of the clock outputs to one of the clock inputs. ZDM is available on each of the four PLLs (RFPLL, DSPLLA, DSPLLB, PPSPLL) and is required when the PPSPLL is enabled. For more details on implementing ZDM, see "AN1293: Si55xx Schematic Design and Board Layout Guidelines" and the "Si5518/12/10/08 Reference Manual".

3.9. PPSPLL

The PPSPLL allows synchronization of the Si5512 to an external 1PPS (1 Hz) or PP2S (0.5 Hz) input clock and is configurable in ClockBuilder Pro. When a valid input clock to DSPLLA is present the PPSPLL modulates DSPLLA. When DSPLLA is unused or in holdover/free-run, the PPSPLL will automatically modulate the RFPLL as well as DSPLLA. The PPSPLL uses an external feedback loop to guarantee minimal input-to-output delay between the PPS input and the generated PPS output. IN3b is used as the feedback input. To minimize input to output latency in PPSPLL Zero Delay Mode, OUT0 or other low-numbered outputs should be used as the feedback output to reduce the PCB routing distance.

See the "Si5518/12/10/08 Reference Manual" and ClockBuilder Pro for more information and recommendations regarding the PPSPLL and the features it supports.

The PPSPLL supports the features described in the following subsections.

3.9.1. Instant Lock

When an input clock is first applied to the PPSPLL, the PLL will make a measurement of input frequency to lock the PLL frequency. The PPSPLL will then measure the phase difference between the input clock and the ZDM feedback input and apply an open loop phase adjustment (referred to as a phase jam) to zero out the phase difference at a much faster rate than the low bandwidth of the PPSPLL. See the "Si5518/12/10/08 Reference Manual" for an in-depth discussion of PPSPLL instant lock and the phase transients that may result.

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3.9.2. Bandwidth Settings

Three separate loop bandwidths are configurable in ClockBuilder Pro:

- **Initial Lock Bandwidth**—The PPSPLL uses this bandwidth when it exits the Free-Run Mode and attempts to lock to a new input clock.
- **Loop Bandwidth**—This sets the bandwidth of the PPSPLL once lock to an input is achieved.
- **Fastlock Bandwidth**—This sets the bandwidth of the PPSPLL when exiting from holdover.

3.9.3. Auto and Manual Relock

When enabled, this feature allows the PPSPLL to quickly reestablish lock during an input phase step or frequency step by issuing a phase jam to the PPS output. The threshold where auto relock is triggered is definable in ClockBuilder Pro.

An alternative option to auto relock is to use the PHASE_READOUT API to monitor the phase offset seen by the PPSPLL. When the offset exceeds a desired threshold, manually trigger a relock/phase jam via the PPS_RELOCK API command. A manual relock may often be preferred over auto relock in order to power down or reset RF equipment relying on PPS synchronization before issuing the relock, which will cause large disturbances to the outputs synchronized to PPS.

3.9.4. Phase Slope Limit

When enabled, this feature limits the rate of phase change of the output clock(s) when a phase transient occurs at the input. The phase slope limit (PSL) is definable in ClockBuilder Pro in units of ns/s.

3.9.5. Phase Pull-in Rate

When enabled, this feature limits the phase pull-in of the PPSPLL output clock(s) during an input clock switch or exit from holdover. The phase pull-in rate (PPI) is definable in ClockBuilder Pro in units of ns/s.

3.9.6. Holdover History

The PPSPLL automatically enters holdover when its input fails. It uses the average frequency that was collected while locked to an input to prevent any disturbances at the outputs when entering holdover. The length of data collected is configurable in ClockBuilder Pro.

3.9.7. Status Monitoring

The PPSPLL has several status monitors accessible through API commands. These include (but are not limited to):

- Input Status (IN0, IN1, IN2, IN2b, IN3, IN3b)
  - Input Valid
  - Loss of Signal (LOS)
  - Out of Frequency (OOF)
  - Phase Monitor (Phase error, Signal late, Signal early)
- PLL Status
  - Loss of Lock (LOL status accessible through API and GPIO)
  - Out of Phase
  - Out of Frequency
  - In Holdover
  - Phase Slope Limit in Progress
  - Fastlock Bandwidth in Use

Refer to the API documentation and the "Si5518/12/10/08 Reference Manual" for more detailed information.

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3.10. External Reference Clocks (XA/XB, REF_IN)

The Si5512 operates from either an external crystal oscillator (XO) connected to the REF_IN pins or with an optional fixed-frequency crystal (XTAL) connected to the XA, XB pins. The internal oscillator (OSC) combined with a low cost external XTAL produces an ultra-low jitter reference clock for the PLLs (RFPLL, DSPLLA/B, PPSPLL). When using an external XO, it's important to select one that meets the jitter performance requirements of the end application. Operating the device with only an XO or XTAL is referred to as Single-Reference Mode, shown in Figure 5.

The Si5512 can also be configured in a Dual-Reference Mode where a TCXO or OCXO provides improved output frequency accuracy and stability during Free-Run Mode and greater frequency stability in Holdover Mode. In this case, the RFPLL locks to a TCXO or OCXO that is applied to one of the inputs. The low phase noise reference XO or XTAL is connected to REF_IN or XA/XB as described above. This configuration is shown in Figure 6.

Use ClockBuilder Pro to configure the device in either Single-Reference Mode or Dual-Reference Mode.

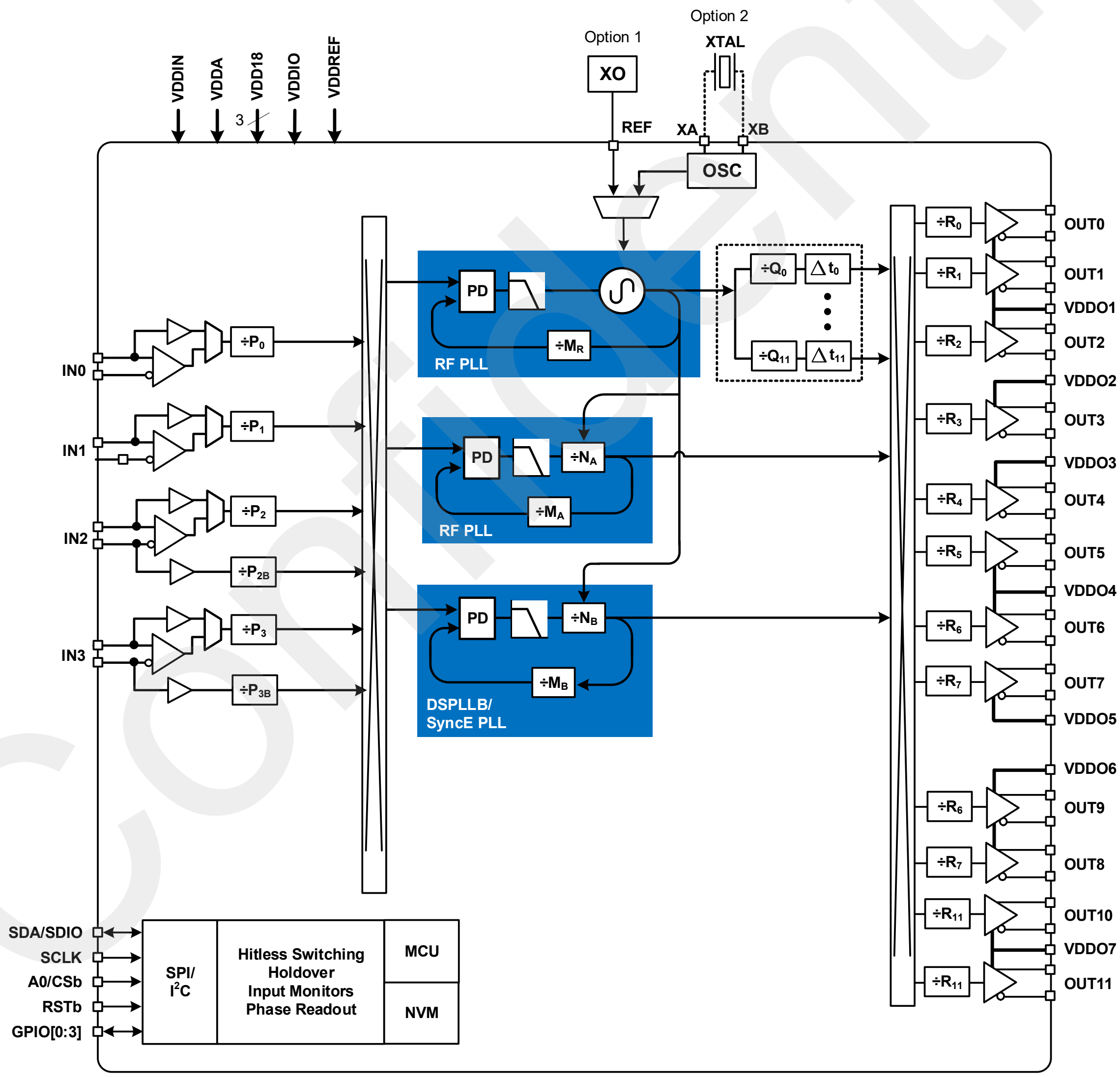

Figure 5. Single-Reference Mode

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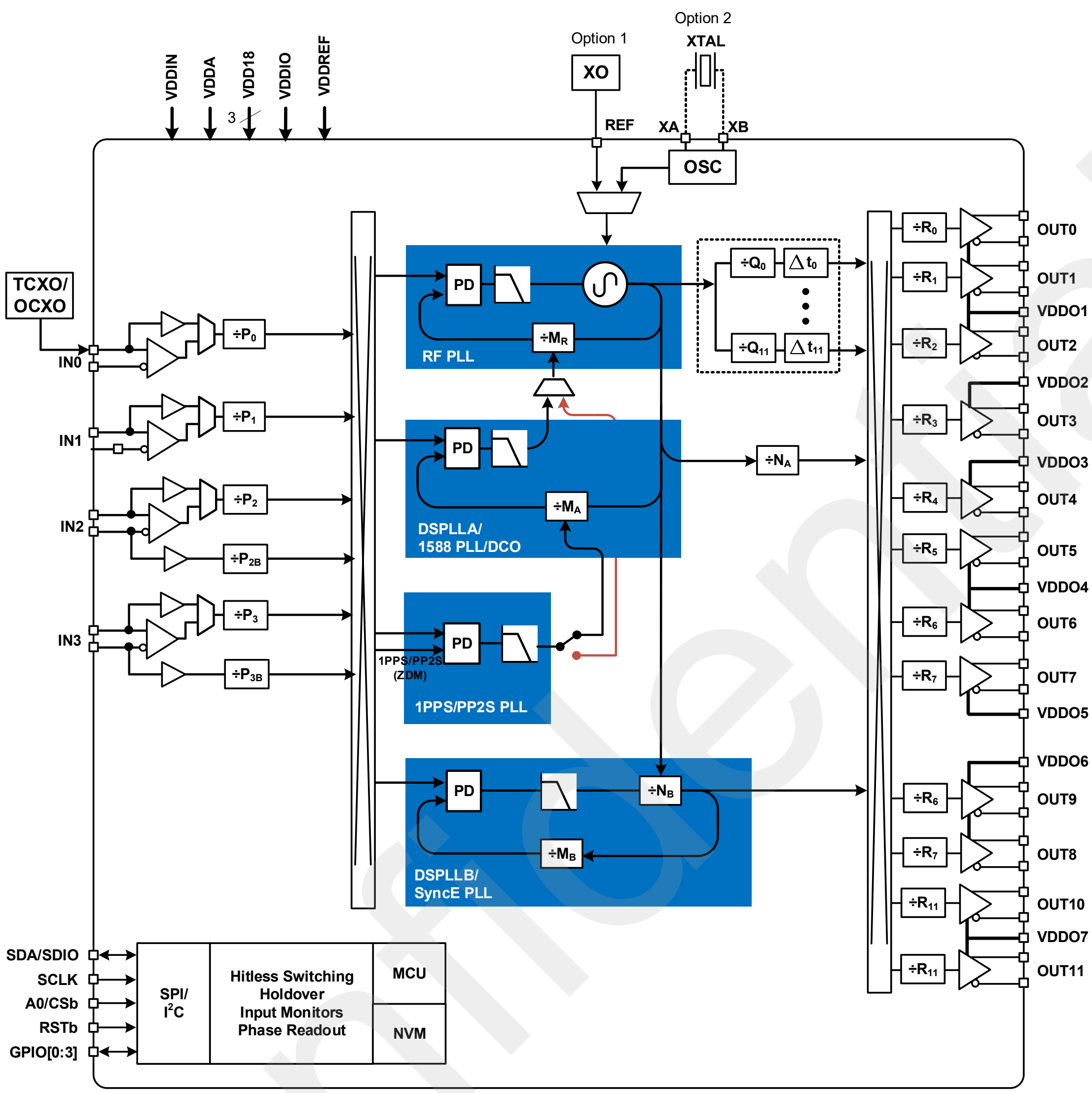

Figure 6. Dual-Reference Mode

3.10.1. XA, XB Inputs

The XA/XB inputs are used to provide a fixed frequency reference for the PLLs (RFPLL, DSPLLA/B, PPSPLL). The device includes internal XTAL loading capacitors which eliminate the need for external capacitors and also has the benefit of reduced noise coupling from external sources. A crystal in the range of 48 to 54 MHz is recommended for best jitter performance.

3.10.2. REF_IN Input

An alternative to using an external XTAL is to connect a crystal oscillator (XO) directly to the REF_IN Input. The REF_IN inputs accommodate both single-ended CMOS as well as differential XOs. See the “Si55xx, Si540x, and Si536x Recommended XTAL, XO, VCXO, TCXO, and OCXO Reference Manual” for more information.

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3.11. GPIO Pins (General Purpose Input or Output)

There are four GPIO pins with programmable functions. They can be assigned as either an input or an output from one of the functions shown in the table below. OUT6/11 can be repurposed as GPIs when they are not being used as clock outputs.

The GPIs are programmable as either active-high or active-low via ClockBuilder Pro. Active low GPIs are indicated by adding a “b” at the end of the function name, e.g., “OEb”, as displayed in ClockBuilder Pro. All GPI pins have a weak pull-up (PU) or pull-down (PD) resistor to set a default state when not externally driven. The default state of the GPI is always de-asserted except for OEx, which is, by default, asserted to enable the outputs. The internal resistance of the PU/PD resistor is 20 kΩ typical.

GPIO selectable status outputs (GPOs) are push-pull and do not require any external pull-up or pull-down resistors.

Table 2. GPIO Pin Descriptions

Function	Description
GPIO selectable control inputs (GPI)	
FINC	DCO frequency increment.
FDEC	DCO frequency decrement.
PLLx_FORCE_HO	Force holdover for RFPLL, or DSPLL A, or DSPLL B.
PLLx_INSEL[0-2]	Input select pins for RFPLL, or DSPLL A, or DSPLL B. There are three bits to select from one of six inputs.
IN[0:5]_FAIL	Force input invalid. A low on this pin indicates to the automatic switching state machine that the associated input is not valid for selection. This is useful in applications that use their own input monitoring.
OE0–OE1	Output enable for specific outputs or group of outputs as defined by the grouping assigned in ClockBuilder Pro.
SRCREQ	JESD204B/C SYSREF pulse request.
GPO selectable status outputs (GPO)	
PLLx_LOL	Loss of lock for RFPLL, DSPLLA, DSPLLB, and PPSPLL.
PLLx_HO	This pin indicates when RFPLL, DSPLL A, DSPLL B has entered the holdover state.
INx_LOS	Loss of Signal status indicator for INx.
INx_OOF	Out of Frequency status indicator for INx.
REF_OOF	Out of Frequency status indicator of the reference.
REF_LOS	Loss of signal at XA/XB and REF pins.
INTR	Interrupt pin for the device. Programmable Boolean combination of PLLx_LOL, INx_LOS, INx_OOF, PLLx_HO, REF_LOS, REF_OOF.
Primary serial interface (I^{2}C/SPI)	
A1/SDO	A1/SDO of Primary SPI Port. **Assignable to GPIO3 only.
A0/CSb	A0/CSb of Primary SPI Port.
SDA/SDIO	SDA/SDIO of Primary SPI Port.
SCLK	SCLK of Primary SPI Port.
Secondary serial interface (3-Wire SPI only)	
CSb2	CSb of secondary SPI Port. **Assignable to GPIO0 only.
SDIO2	SDIO of a secondary SPI Port. **Assignable to GPIO1 only.
SCLK2	SCLK of a secondary SPI port. **Assignable to GPIO2 only.

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3.12. Device Initialization and Reset

Once power is applied and RSTb is de-asserted, the device begins loading preconfigured register values and configuration data from NVM and performs other initialization tasks. Communicating with the device through the serial interface is possible once this initialization period is complete (see t_{RDY}). No output clocks will be generated until the initialization is complete and the device locks to the external (VC)XO/XTAL (see t_{START_XO} and t_{START_XTAL}). A reset, initiated using the RSTb pin or through the Device API RESTART command, restores all registers to the values stored in NVM, and all circuits, including the serial interface, will be restored to their initial state. All clocks will stop during a hard reset. Other feature-specific resets are also available. For more information on different methods of resetting the device, see the Si5518/12/10/08 Reference Manual and AN1360: Serial Communications and API Programming Guide for Si536x, Si540x, and Si55xx Devices.

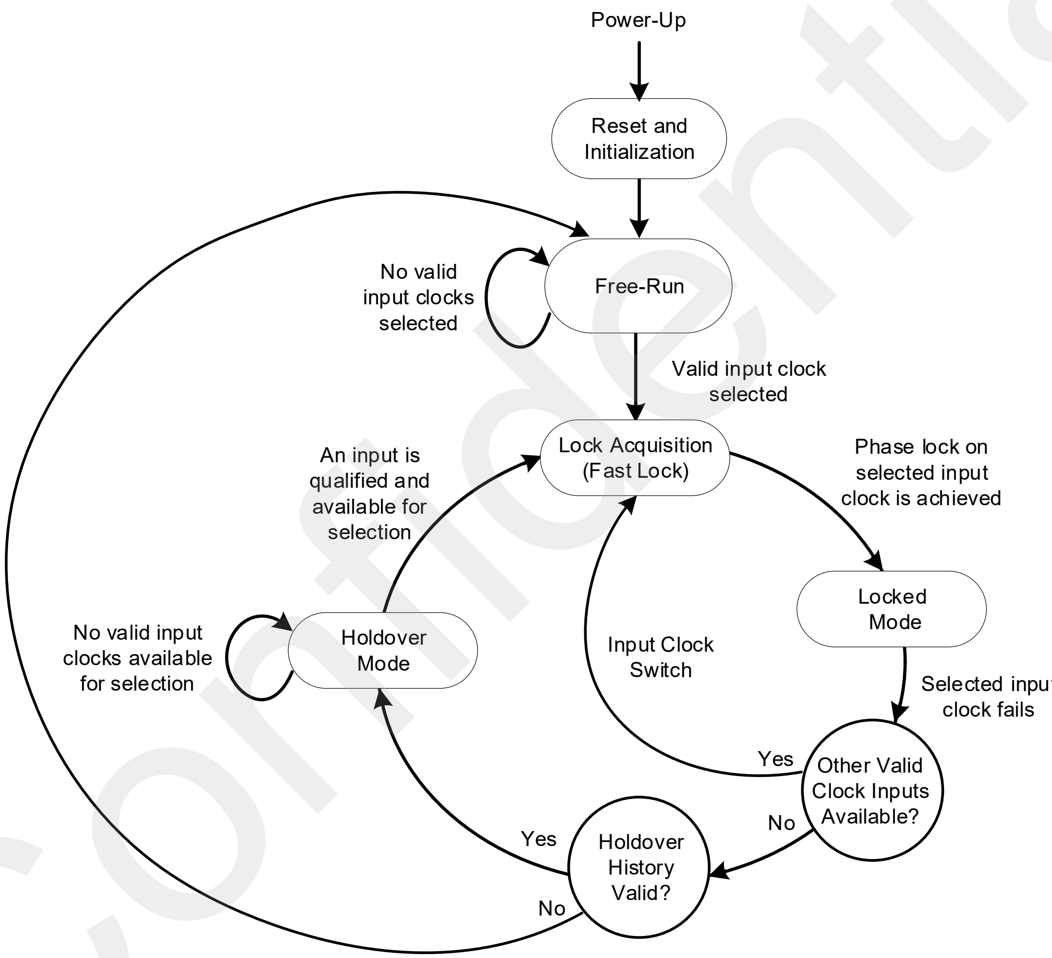

Figure 7. Modes of Operation

3.13. Modes of Operation (RFPLL, DSPLL A, DSPLL B)

Once initialization is complete each PLL independently operates in one of four modes: Free-Run, Lock Acquisition, Locked, or Holdover. A state diagram showing the modes of operation is shown in Figure 7 above. The following sections describe each of these modes in greater detail.

3.13.1. Free-Run Mode

The PLLs will automatically enter Free-Run Mode once power is applied to the device and initialization is complete. In this mode, the frequency accuracy of the generated output clocks is entirely dependent on the frequency accuracy of the reference clock source. If a XTAL is connected to the XA/XB pins then the clock outputs will generate a frequency at the XTAL's accuracy. For example, if a XTAL is operating at –28 ppm then clock outputs will also be –28 ppm. The same is true if a XO is connected at the XO_IN inputs instead of using XTAL at XA/XB. The frequency stability of the outputs will also be determined by the XTAL or XO.

When a TCXO or OCXO is connected to the RFPLL inputs, then the frequency accuracy and stability of the outputs will be determined by the TCXO or OCXO. This is recommended for applications that need better accuracy and stability than what the XTAL or XO can provide.

3.13.2. Lock Acquisition Mode

Each of the PLLs independently monitors its configured inputs for a valid clock. If at least one valid clock is available for synchronization, a PLL will automatically start the lock acquisition process. If the fast lock feature is enabled, they will acquire lock faster than the PLL Loop Bandwidth would provide and then transition to the normal PLL loop bandwidth. During lock acquisition the outputs will generate a clock that follows the VCO frequency change as it pulls-in to the input clock frequency.

The PLL_STATUS Device API command reports the lock status of a PLL. When the PLL output frequency is within the threshold defined on the Frequency LOL (FLOL) page in ClockBuilder Pro, the PLL_OUT_OF_FREQUENCY bit de-asserts. Some time after that, the PLL will pull in the remaining phase defined on the Phase LOL (PLOL) page in ClockBuilder Pro. Once the PLL is frequency and phase locked, the PLL_LOSS_OF_LOCK (LOL) bit de-asserts, and the PLL enters Locked Mode.

3.13.3. Locked Mode

Once locked, the PLL will generate clock outputs that are both frequency and phase locked to their selected input clocks. The PLL loop bandwidths can be independently configured. Any frequency changes (e.g., due to temperature variations) of the reference clock (REF_IN) within the PLL loop bandwidth will be corrected by the loop ensuring 0 ppm lock to its input clock (IN). Any frequency changes of the reference clock (REF_IN) beyond the PLL loop bandwidth will pass through to the clock output.

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3.13.4. Holdover Mode

Any of the PLLs will automatically enter Holdover Mode when the selected input clock becomes invalid, holdover history is valid, and no other valid input clocks are available for selection. Each PLL uses an averaged input clock frequency as its final holdover frequency to minimize the disturbance of the output clock phase and frequency when an input clock suddenly fails. The holdover circuit for each PLL stores historical frequency data while locked to a valid input clock. The final averaged holdover frequency value is calculated from a programmable window within the stored historical frequency data. Both the window size and delay are programmable as shown in the figure below. The window size determines the amount of holdover frequency averaging. The delay value allows ignoring frequency data that may be corrupt just before the input clock failure.

The maximum window size is a function of input frequency and is reported in ClockBuilder Pro for each PLL. 240 seconds is the maximum window size for 1PPS/PP2S inputs as shown in Figure 8 below. For higher-frequency inputs, up to 5000 seconds of holdover history can be stored.

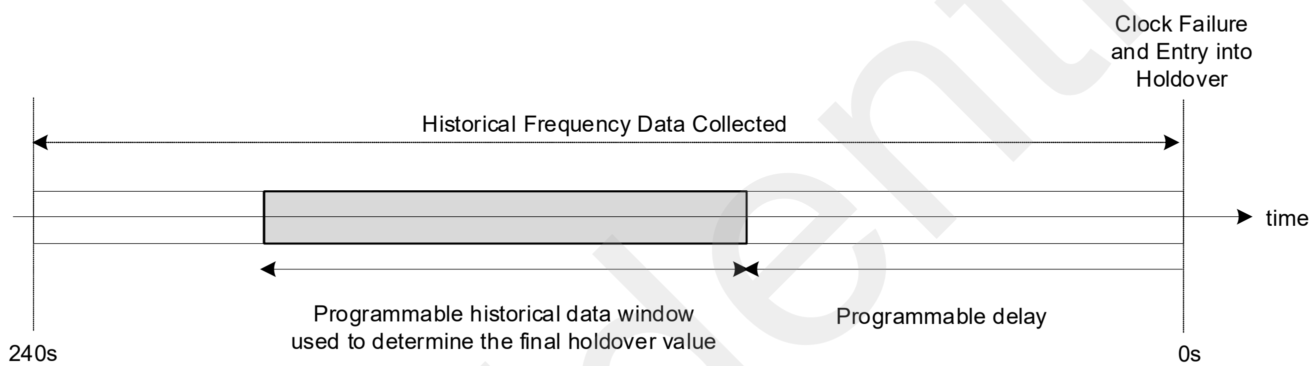

Figure 8. Programmable Holdover Window

When entering holdover, a PLL will pull its output clock frequency to the calculated averaged holdover frequency. While in holdover, the output frequency drift is entirely dependent on the external reference clock connected to the REF_IN input and, if an OCXO/TCXO holdover reference is used, also dependent on the holdover reference. If the input clock becomes valid, a PLL will automatically exit Holdover Mode and reacquire lock to the new input clock. This process involves pulling the output clock frequency to achieve frequency and phase lock with the input clock. This pull-in process is glitchless.

The PLL output frequency when exiting holdover can be ramped. Just before the exit is initiated, the difference between the current holdover frequency and the new desired frequency is measured. Using the calculated difference and a user-selectable ramp rate, the output is linearly ramped to the new frequency. The PLL loop BW does not limit or affect ramp rate selections (and vice versa). ClockBuilder Pro defaults to ramped exit from Holdover and Free-Run. The ramp rate settings are configurable for initial lock (exit from Free-Run), exit from Holdover, and clock switching.

If ramped holdover exit is disabled, the holdover exit is governed either by (1) the PLL loop BW or (2) the PLL Fastlock bandwidth, when enabled.

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3.14. IEEE 1588 Mode

3.14.1. Synchronizing to a Master Clock when in IEEE 1588 Mode

When IEEE 1588 mode is used (see Figure 9), the servo loop software will check the Announce Messages it receives from upstream master nodes (in its clock domain), and, using the BMCA, will choose the master with the best clock (which could be itself). It then begins to synchronize its local clock to that of the master's clock using IEEE 1588 timestamps.

The IEEE 1588 Servo Loop Software will acquire lock using the Startup Time Constant and then transition to the Main Time Constant once the node synchronizes its local clock to that of the selected master's clock. These time constants effectively set the servo loop bandwidth and are user-configurable.

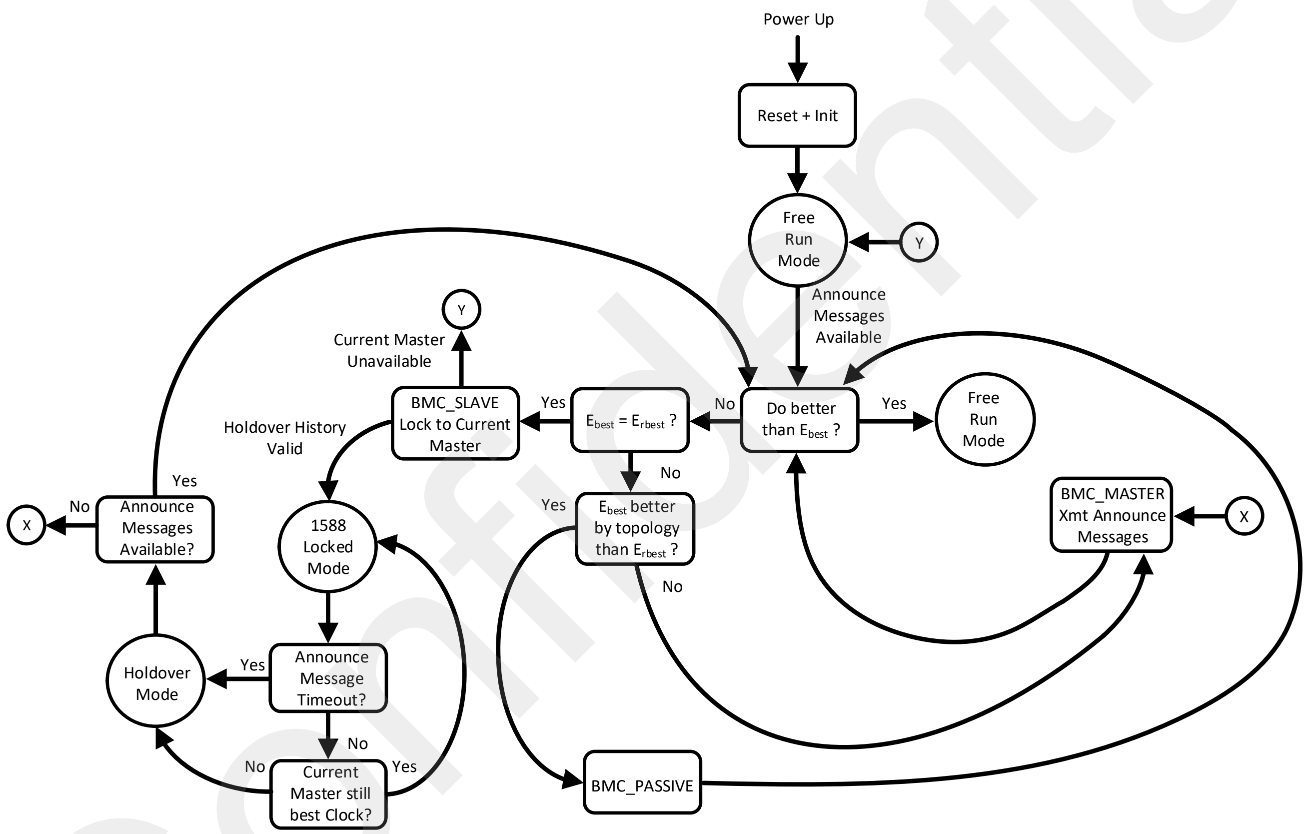

Figure 9. Modes of Operation (IEEE 1588 Mode - BMCA)

3.15. PTP Holdover Mode (IEEE 1588 Holdover Mode)

When timestamps are no longer available (either due to Announce Message timeout from the current master clock or due to selecting a better clock from a remote master via BMCA), the node will enter PTP holdover. In this mode, the accuracy and stability of the output clocks synchronized to PTP will be dependent on the PTP clock average calculation, which is dependent on the "control average" time constant, as well as the stability of the input reference clock. If the reference is from a SyncE input, then this PTP Holdover Mode will be referred to as "PTP holdover with physical layer assist", and the outputs will assume the stability of the SyncE clock.

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If there is no physical layer clock synchronizing the PLL steered by PTP, then it will synchronize to the local reference oscillator, and the outputs will assume the stability of this oscillator. This PTP Holdover Mode is referred to as “holdover without physical layer assist”. Once the connection to an upstream master has been reestablished and the IEEE 1588 timestamps are once again available, the servo loop will exit from PTP holdover and begin synchronizing its local clock to that of the new master.

3.16. Status and Alarms

The Si5512 monitors the input clocks and reference input for status and alarms. The status and alarms provide the internal state machine with real-time phase and frequency monitoring used for making decisions, such as switching inputs or entering holdover.

3.16.1. Input Clock Status

All input clocks are continuously monitored for faults using the Loss-of-Signal (LOS), Out-of-Frequency (OOF), and Phase Monitor (PHMON) alarms. When a differential input is configured as a dual CMOS input, then each CMOS input is independently monitored. Any enabled alarms for an input, such as LOS/OOF/PHMON, are logically ORed together to produce the input invalid alarm.

Any input clock with an alarm is not valid until all alarms are cleared. If a PLL is locked to an input clock and that input clock becomes invalid, then the PLL may either switch to a valid input or enter Holdover Mode, depending on how the device is programmed.

API commands can be used to indicate if an alarm is valid, pending short term fault, under validation or invalid.

3.16.1.1. Loss of Signal (LOS)

The loss of signal alarm measures the period of each input clock cycle to detect phase irregularities or missing clock edges. Each of the input LOS circuits has its own programmable sensitivity, which allows missing edges or intermittent errors to be ignored. Loss of signal sensitivity is configurable using the ClockBuilder Pro utility. The LOS status for each of the monitors is accessible by checking the INPUT_STATUS API.

3.16.1.2. Out of Frequency (OOF) Detection

All inputs are monitored for frequency accuracy with respect to an OOF reference which is selected in Clock-Builder Pro. The OOF reference can be selected as either the XO/XTAL or the OCXO/TCXO in Dual Reference Mode. When available it is recommended to select the OCXO/TCXO as the OOF reference since it will have a tighter frequency accuracy compared to a free-running XTAL or XO.

The OOF set and clear thresholds must be wider than the combined frequency accuracy of the OOF reference plus the stability of the input clock. A valid input clock frequency is one that remains within the OOF frequency range which is configurable from ±0.1 ppm to ±500 ppm in steps of 0.1 ppm. A configurable amount of hysteresis is also available to prevent the OOF status from toggling at the failure boundary. An example is shown in the figure below. In this case, the OOF monitor is configured with a valid frequency range of ±15 ppm with 5 ppm of hysteresis. This OOF configuration will support a Dual Reference Mode with a Stratum 3 level OCXO/TCXO and a SyncE input which both have ±4.6 ppm overall frequency accuracy.

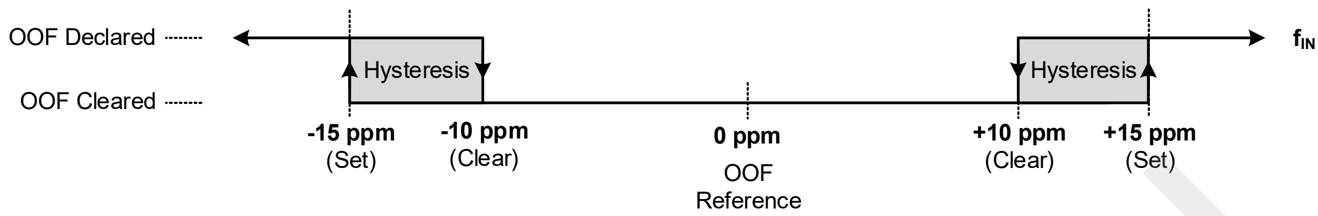

Figure 10. Example of Precise OOF Monitoring Assertion and De-Assertion Triggers

3.16.1.3. Phase Monitor (PHMON)

If a clock input undergoes a phase transient, a PLL locked to that input will filter the transient by its loop bandwidth; however, the transient will propagate to the output. Transients that propagate to the output have the potential to negatively impact downstream devices.

Phase Monitor (PHMON) alarm monitors the input clock phase or accumulated phase, and, if the input transient exceeds the programmable threshold, the PHMON alarm will be asserted. PHMON, like the other alarms, is quick to be asserted when the thresholds are violated yet slower to be de-asserted to prevent chattering around the threshold.

Each input clock has an independent PHMON alarm. Each alarm can be enabled/disabled individually, and its associated threshold may be independently configured. Note that OOF must be enabled and properly configured for PHMON to operate.

A ZDM input may use the PHMON alarm for monitoring purposes. However, it will have no effect on PLL bandwidth selection and will not cause input switching.

3.16.1.4. Short Term Holdover

The Short-Term Holdover (STHO) feature may be used when the input clock is expected to have a short-term fault and then quickly recover.

If an input clock has STHO enabled, and an LOS/OOF/PHMON alarm is asserted, then a PLL locked to that input will enter holdover and wait for a programmable duration until all alarms on the input clock are de-asserted.

If all alarms on the input clock are de-asserted before the programmable amount of time has passed, then the PLL will gracefully relock to the same input clock. If all the alarms on the input clock are not de-asserted before the programmable amount of time has passed, then the PLL will either switch to the next priority input clock or remain in holdover, depending on the input clock selection settings.

If STHO is disabled, then the PLL will skip the short-term holdover time and immediately switch to the next priority input clock or enter holdover, depending on the input clock selection settings.

STHO may be programmed using Clock Builder Pro to set the duration or to enable or disable the feature for each input clock individually. Note that the STHO setting will affect all PLLs assigned to that input.

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3.16.2. PLL Status

RFPLL, DSPLL A, DSPLL B, and PPSPLL are continuously monitored for Loss-of-Lock (LOL). The final LOL status indicator is the logical OR of the Frequency Loss-of-Lock and Phase Loss-of-Lock statuses. See the "Si5518/12/10/08 Reference Manual" for more information.

3.16.2.1. Loss of Lock (LOL)

There is a loss of lock (LOL) monitor for each of the PLLs (RFPLL, DSPLL A, DSPLL B, and PPSPLL). The LOL monitor asserts when a PLL has lost synchronization with its selected input clock. Any of the GPIOs can be programmed as a dedicated loss-of-lock pin that reflects the loss-of-lock condition for each of the PLLs. The LOL monitor measures both the frequency and phase difference between the input and feedback clocks of the phase detector. The frequency monitor gives frequency lock detection (FLOL) while the phase monitor indicates true phase lock PLOL by detecting one or more single slips. Both the phase and frequency LOL monitors have clear and set thresholds and a timer to prevent LOL assertion from toggling or chattering as the DSPLL completes lock acquisition.
The cycle slip detector also has configurable sensitivity.

3.16.2.2. Frequency Loss of Lock (FLOL)

The Frequency Loss-of-Lock (FLOL) monitor measures the frequency difference between the input clock and the feedback clock. The upper and lower LOL thresholds are programmable, which dictates when the alarm will be asserted or de-asserted. It is recommended to program the clear threshold to be less than the set threshold to allow for hysteresis in the FLOL set/clear behavior. This prevents the FLOL alarm from chattering or causing multiple interrupts. FLOL, like the other alarms, is quick to be asserted when the threshold is violated yet slower to be de-asserted. The alarm validates that the frequency difference between the input and feedback clocks has truly settled to within the LOL clear threshold before the FLOL alarm is de-asserted. The time required to validate the frequency difference increases as the loop bandwidth of the PLL decreases.

3.16.2.3. Lock Status Bits

There are four lock status bits that serve as four additional Frequency LOL thresholds. The Status Bit (STB) is asserted if the frequency difference between the input clock and feedback clock exceeds the programmable STB threshold. The assertion or de-assertion of an STB does not contribute to the FLOL or LOL status. Rather, they serve as a way to track the lock acquisition process for DSPLLs with a loop bandwidth of <10 Hz. The lock status bits may be read via the API. In the lock acquisition process, the de-assertion of a STB does not indicate that the PLL is frequency locked. This is because the frequency may chatter around the STB threshold. On the other hand, the deassertion of FLOL requires the frequency difference to truly settle below the LOL clear threshold.

3.16.2.4. Phase Loss of Lock (PLOL)

The Phase Loss-of-Lock (PLOL) alarm measures the phase difference between the input clock and feedback clock. The PLOL set threshold is programmable so the alarm will assert or deassert depending on phase difference between the input and feedback clocks relative to the threshold setting. It is recommended to set the clear threshold below the set threshold to allow for hysteresis. This prevents the alarm from chattering or causing multiple interrupts. During the lock acquisition process, the input clock and feedback clock will likely have a significant frequency mismatch; so, the PLOL is not asserted until FLOL is deasserted. Once FLOL has been de-asserted, the two frequencies are stable with respect to each other. Then the feedback clock phase can be pulled in to within the PLOL clear threshold.

3.16.2.5. Cycle Slip Detection

RFPLL, DSPLLA, and DSPLLB may be monitored for cycle slips. Like the PLOL alarm, cycle slip detection is not enabled until FLOL is de-asserted. Additionally, PLOL must be enabled for cycle slip detection to be enabled. Cycle slips both in the positive and negative direction are monitored. The API can be used to read the total count of positive cycle slips, the total count of negative cycle slips, and the total count of both positive and negative slips.

3.16.3. External Reference Status

An external reference must always be provided to the device. The Si5512 monitors the external reference input for LOS, OOF, and LOL. If a fault is detected on the external reference, then the outputs will be disabled. Any external reference faults may be read via the API.

3.16.4. Interrupt Status

The interrupt flag is asserted when any of the status indicators of the device changes state. The interrupt status may be assigned a GPIO pin, or it may be checked using an API command to show which status indicator caused the interrupt to be asserted.

The Interrupt Configuration page in ClockBuilder Pro lists all the status indicators that can be programmed to activate the interrupt pin.

The status indicators that are enabled are logically OR'd together so that the assertion of any of these status indicators will cause the interrupt pin to assert. The interrupt pin status depends on the sticky versions of the individual status indicators, so the interrupt pin will stay asserted until the sticky status indicators are cleared.

3.17. Serial Interface

Configuration and operation of the Si5512 is controlled by reading and writing API commands using the I^2C or SPI interface. The primary SPI mode operates in either 4-wire or 3- wire modes. A second SPI port, which operates only in 3-wire mode, can also be configured allowing dual port access to the device. An internal arbiter prevents contentions during bus operations so that both ports can be used simultaneously. The following tables define the GPIO pins assigned to the primary and secondary SPI ports, respectively.

Table 3. Primary Serial Interface Pins

Pin Number	3-Wire SPI	4-Wire SPI	I^2C
55	CSb	CSb	A0
52	SDIO	SDI	SDA
53	SCLK	SCLK	SCK
56	Unused	SDO	A1

Table 4. Secondary Serial Interface Pins

Pin Number	SPI Pin	Assignable GPIO Pins
16	CS2b	GPIO0
18	SDIO2	GPIO1
19	SCLK2	GPIO2

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3.18. NVM Programming

At power-up, the device loads its default user configuration and firmware from internal non-volatile memory (NVM). The NVM can be preprogrammed at the factory with a custom frequency plan such that the device starts generating clocks on its first power-up, or the NVM can be programmed in the field using the API command set. NVM programming in the field must be done with VDDA set to 3.3V. NVM programming in the field is not supported in Low-Power mode. For more details on NVM programming options, refer to "AN1360: Serial Communications and API Programming Guide for Si536x, Si540x, and Si55xx Devices" and the "Si5518/12/10/08 Reference Manual".

3.19. Application Programming Interface (API)

Communication between the customer's host processor and the Si5512 internal microcontroller (MCU) is accomplished through the serial interface. The Si5512 MCU contains firmware that allows users to have command-level access to the device API. Internal registers are not accessible through the API because all features of the Si5512 can be accessed through the Device API. The primary serial port (SPI or I^2C) allows programming of the Si5512, and the secondary serial port (SPI 3-wire only) is intended for Phase Readback and status monitoring operations. The Host processor can also communicate with the Si5512 using Skyworks' optional AccuTime IEEE 1588 software and API. The AccuTime software runs on the host processor. See the "Si5518/12/10/08 Reference Manual" for more information and examples of the API. Details of the API commands are available through Clock-Builder Pro. For instructions on using the Device API and for instructions on programming the clock device, see "AN1360: Serial Communications and API Programming Guide for Si536x, Si540x, and Si55xx Devices".

3.20. AccuTime IEEE 1588 Software

The Si5512 may be combined with optional AccuTime IEEE 1588 software to create a complete IEEE 1588 solution for time, phase, and frequency synchronization. AccuTime 1588 software consists of a unique servo algorithm paired with a protocol stack that all runs on the customer's host processor.

The architecture of AccuTime is shown in the simplified figure below. AccuTime is a layered architecture consisting of the customer's hardware platform and the OSAL and OEM at the bottom (system-dependent) layer, including system-dependent configuration files to customize the AccuTime software for the OS and HW platform. Next is the System-Independent Layer consisting of the AccuTime software. The example applications are provided with AccuTime and include the Sync Timing Util application and ESMC handler.

The System-Independent layer interfaces with the user's OS and hardware via API calls through the OSAL and OEM layers. This includes the C API library for controlling and monitoring the Si5512 device.

The OEM Abstraction layer allows low level communications with the Si5512 via SPI or I^2C, GPIO, etc. The OEM layer communicates with the Linux kernel via kernel system calls and IOCTL. Device drivers in the Linux kernel communicate with the hardware devices in the user's hardware platform which includes the Ethernet PHY + MAC, Time of Day (ToD) counter block, serial input/output for transmitting/receiving ToD information, as well as the Si5512.

The OEM and OSAL layers use system calls and rely on the Linux kernel. In the OEM layer case, system calls are used to interact with the hardware, whereas in the OSAL layer case, system calls are used to leverage the software specific functions provided by the kernel (mutexes, semaphores, queues, etc.).

The AccuTime 1588 Protocol Stack provides an application in the user space running on the host processor on top of the Linux OS. The protocol stack processes the PTP messages and passes the necessary data to the PTP servo. The servo loop controls the 1588 DCO operation to the Si5512 device to adjust the system clock it sends to synchronize the ToD counter in the host to align it with the ToD in the master.

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Software setup, configuration, API/CLI command libraries, and porting details are fully documented in the AccuTime Software Release.

AccuTime software is available under a license. Contact your Skyworks Representative for more information.

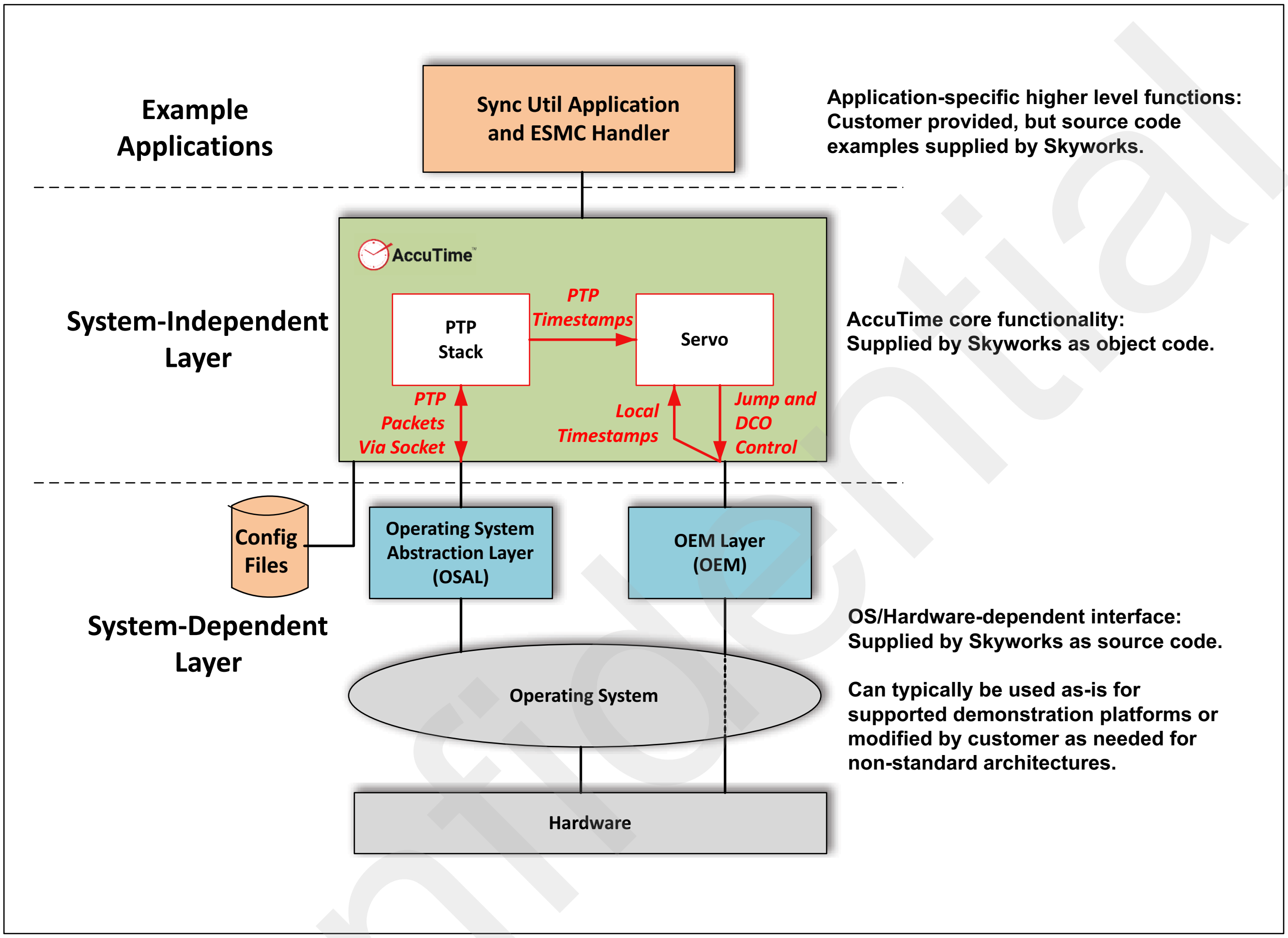

Figure 11. AccuTime Simplified Architecture

3.21. Power Supplies

The Si5512 has 14 power supply pins. The separate power supplies are used for different functions, providing power locally where it is needed on the die to improve isolation. When no outputs are enabled for a particular VDDOx, that supply pin may be left unconnected. Please refer to "AN1293: Si55xx Schematic Design and Board Layout Guide" for more details on power management and filtering recommendations.

3.21.1. Power Supply Sequencing

There are no power sequencing requirements between supplies. VDDA and VDD18 should be powered up before releasing RSTb. VDDA must be equal to the highest voltage supply. See Table 8, "DC Characteristics," on page 31 for the supply ramp rate specification.

3.21.2. Power Supply Ramp Rate

Power supply ramp times must stay within the maximum supply voltage ramp rate as defined in Table 8, "DC Characteristics," on page 31.

3.21.3. Low-Power Mode

In Low-Power Mode, the analog core supply voltage (VDDA) of the Si5512 is set to 1.8 V in order to reduce power consumption. Since VDDA must be equal to the highest voltage applied to the Si5512, in Low-Power Mode, all voltage supplies including VDDO must be 1.8 V. A 1.8 V VDDO restricts the output format to S-LVDS, LVCMOS, or HCSL. If LVPECL or LVDS output format is required, Low-Power Mode cannot be used. NVM programming in the field is not supported in Low-Power Mode since NVM programming requires VDDA to be 3.3 V. Please refer to the "Si5518/12/10/08 Reference Manual" for VDDREF and XO/XTAL connections and terminations for Low-Power Mode.

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4. Electrical Specifications

All minimum and maximum specifications in the following tables are guaranteed and apply across recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise noted.

Table 5. Absolute Maximum Ratings[1,2,3]

Parameter	Symbol	Test Condition	Value	Unit
DC supply voltage	V_{DDIN}		–0.5 to 3.8	V
	V_{DDREF}		–0.5 to 3.8	V
	V_{DD18}		–0.5 to 2.4	V
	V_{DDA}		–0.5 to 3.8	V
	V_{DDO}		–0.5 to 3.8	V
	V_{DDIO}		–0.5 to 3.8	V
Input voltage range	V_{I1}	REF_IN/REF_INb, INx/INxb	–0.85 to 3.8	V
	V_{I2}	GPIO0-3, RSTb, SCLK, SDA/SDIO, A0/CSb	–0.5 to 3.8	V
	V_{I3}	XA/XB	–0.5 to 2.7	V
Latch-up tolerance	LU		JESD78 Compliant	
ESD tolerance	HBM	100 pF, 1.5 kΩ	2.0	kV
Storage range	TSTG		–55 to 150	°C
Maximum junction temperature in operation	T_{JCT}		125	°C
Soldering temperature (Pb-free profile)[4]	T_{PEAK}		260	°C
Soldering time at T_{PEAK} (Pb-free profile)[4]	T_P		20–40	sec

1. Exposure to maximum rating conditions for extended periods may reduce device reliability. Exceeding any of the limits listed here may result in permanent damage to the device.
2. RoHS-6 compliant.
3. For more packaging information, see the Skyworks Certificate of Conformance: Pb-Free & Green.
4. The device is compliant with JEDEC J-STD-020.

ESD Handling: Industry-standard ESD handling precautions must be adhered to at all times to avoid damage to this device.

Table 6. Thermal Conditions

Parameter	Symbol	Test Condition	Typical Value		Unit
			JEDEC[1]	CEVB[2]	
Thermal Resistance Junction-to-Ambient	Θ_{JA}	Still Air	16.15	11.17	°C/W
		1 m/s	10.77	8.10	°C/W
		2 m/s	9.63	7.53	°C/W
Thermal Resistance Junction-to-Board	Ψ_{JB}[3]	Still Air	3.33	3.08	°C/W
Thermal Resistance Junction-to-Top-Center	Ψ_{JC}	Still Air	0.03	0.05	°C/W

1. Based on PCB dimension: 4" x 4.5", PCB thickness: 1.6 mm, Number of Cu Layers: 2.
2. Customer EVB: 8-layer board, board dimensions: “9x9”, all eight layers are copper-poured.
3. ΨJB can be used to calculate the junction temperature based on the board temperature and power dissipation for a given frequency plan, Tj = TPCB + (ΨJB*PD). TPCB should be measured as close to the Si5512 DUT as possible since temperature may vary across the PCB.

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Table 7. Recommended Operating Conditions

VDD18 = 1.8 V ±5%, VDDA = VDDREF = 3.3 V ±5%; All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C.
Low-Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDREF} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient temperature[1]	T_A		–40	25	95	°C
Board temperature	T_B		–40	65	105	°C
Junction temperature	TJ_{MAX}[1]		—	—	125	°C
Core supply voltage	V_{DD18}		1.71	1.80	1.89	V
	V_{DDA}[2]		3.14	3.30	3.47	V
		Low-power mode	1.71	1.80	1.89	V
	V_{DDREF}		3.14	3.30	V_{DDA}[2]	V
		Low-power mode	1.71	1.80	1.89	V
Input supply voltage	V_{DDIN}		3.14	3.30	V_{DDA}[2]	V
			2.38	2.50	2.62	V
			1.71	1.80	1.89	V
GPIO supply voltage	V_{DDIO}		3.14	3.30	V_{DDA}[2]	V
			2.38	2.50	2.62	V
			1.71	1.80	1.89	V
Clock output driver supply voltage	V_{DDO}		3.14	3.30	V_{DDA}[2]	V
			2.38	2.50	2.62	V
			1.71	1.80	1.89	V

1. Ambient temperature of 95 °C may not be possible with all configurations. This is dependent on device configuration. Tj cannot exceed a max of 125 °C.
2. V_{DDA} must be greater than or equal to the highest voltage applied to the device. In low-power mode, all voltage supplies must be set to 1.8 V.

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Table 8. DC Characteristics

V_{DD18} = 1.8 V ±5%, V_{DDA} = V_{DDREF} = 3.3 V ±5%; All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C.
Low-Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDREF} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Core supply current (V_{DD18} + V_{DDA})	I_{DD18}	Si5512[1,2]	—	380	640	mA
	I_{DDA}	Si5512[1,2]	—	210	230	mA
	I_{DD18_PD}	RSTb = 0	—	120	300	mA
	I_{DDA_PD}	RSTb = 0	—	15	16	mA
Periphery supply current (V_{DDIN} + V_{DDIO} + V_{DDREF})	I_{DDIN} + I_{DDIO}	Si5512[1,2]	—	58	76	mA
	I_{DDREF}	Si5512[1,2]	—	12	14	mA
	I_{DDIN_PD} + I_{DDIO_PD} + I_{DDREF_PD}	RSTb = 0	—	2	3	mA
Output Buffer supply current (V_{DDOX})	I_{DDOX} (per output)	LVPECL (2.5 V, 3.3 V) @ 122.88 MHz[3]	—	24	26	mA
		LVDS (2.5 V, 3.3 V) @ 122.88 MHz[3]	—	13	15	mA
		S-LVDS (1.8 V) @ 122.88 MHz[3]	—	12	14	mA
		3.3 V LVCMOS @ 122.88 MHz[4]	—	19	22	mA
		2.5 V LVCMOS @ 122.88 MHz[4]	—	15	17	mA
		1.8 V LVCMOS @ 122.88 MHz[4]	—	11	12	mA
		HSCL Internal Termination (1.8 V, 2.5 V, 3.3 V) @ 122.88 MHz[5]	—	20	23	mA
		CML (1.8 V, 2.5 V, 3.3 V) @ 122.88 MHz[3]	—	14	17	mA
	I_{DDOX_PD}	RSTb = 0	—	0.23	0.3	mA
Total power dissipation	P_D	Si5512[1]	—	1.9	2.6	W
		Si5512 Low-Power Mode[1]	—	1.4	2	W
Supply voltage ramp rate	T_{VDD}	Fastest V_{DD} ramp rate allowed on startup	—	—	100	V/ms

1. Typical test configuration: The following frequencies on 10 LVDS outputs: 2 to 491.52 MHz (Q), 1 to 122.88 MHz (Q), 2 to 1.92 MHz (Q), 1 to 100 MHz (NA), 1 to 50 MHz (NA), 2 to 156.25 MHz (NB), 1 to 125 MHz (NB). Excludes power dissipated in termination resistors. VDDIN = 1.8 V, VDDO = 3.3 V.
2. Typical test configuration: Same as Note 1, except all supplies set to 1.8 V for Low-Power Mode. Output formats changed to S-LVDS format.
3. Differential outputs terminated into an ac-coupled differential 100 Ω load.
4. LVCMOS outputs measured into a 5-inch, 50 Ω PCB trace with 5 pF load.
5. No external termination; amplitude 800 mVpp_se.

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Table 9. Input Specifications

V_{DD18} = 1.8 V ±5%, V_{DDA} = V_{DDREF} = 3.3 V ±5%; All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C.
Low-Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDREF} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C.

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
LVCMOS (XO Applied to REF_IN)						
Input frequency range	f_{IN_CMOS}	Frequencies > 48 MHz are recommended for best performance.	30.72	—	250	MHz
Slew rate[1,2,3]	SR		0.75	—	—	V/ns
Input voltage	V_{IL}		—	—	V_{DDREF} x 0.3	V
	V_{IH}		V_{DDREF} x 0.7	—	—	V
Input resistance	R_{IN}		—	63	—	kΩ
Duty cycle	DC		40	—	60	%
Capacitance	C_{IN_SE}		—	1.25	—	pF
Differential (XO Applied to REF_IN)						
Input frequency range	f_{IN_DIFF}	Frequencies > 48 MHz are recommended for best performance.	30.72	—	983.04	MHz
Voltage swing[2]	V_{IN_DIFF}		200	350 (LVDS) 800 (LVPECL)	1800	mVpp_se
Slew rate[1,2,3]	SR		0.75	—	—	V/ns
Duty cycle	DC		40	—	60	%
Capacitance	C_{IN_DIFF}		—	2.5	—	pF
Crystal (Connected to XA/XB Pins)[4]						
Frequency range	f_{IN_XTAL}		48	54	61.44	MHz
Load capacitance	C_L		—	8	—	pF
Crystal drive level	d_L		—	—	200	µW
Equivalent series resistance	R_{ESR}		Refer to the "Si55xx, Si540x, and Si536x Recommended XTAL, XO, VCXO, TCXO, and OCXO Reference Manual" to determine ESR and Shunt Capacitance Values.			
Shunt capacitance	C0					
Differential (INx/INxb)						
Input frequency range	f_{IN_DIFF}	Differential, AC-coupled	0.008	—	1000	MHz
	f_{IN_SE}	Single-ended, AC-coupled	0.008	—	250	MHz
Voltage swing	V_{IN_DIFF}	Differential, AC-coupled	200	350 (LVDS) 800 (LVPECL)	1800	mVpp_se
	V_{IN_SE}	Single-ended, AC-coupled	400	1600	1800	mVpp_se
Slew rate[3,5]	SR		0.4	—	—	V/ns
Duty cycle	DC		40	—	60	%
Capacitance	C_{IN_DIFF}		—	2.5	—	pF
LVCMOS (INx/INxb)						
Input frequency range	f_{IN_LVCMOS}		PP2S PPS 0.008	—	250	MHz
Slew rate[3,5]	SR		0.2	0.4	—	V/ns
Input voltage	V_{IL}		—	—	V_{DDIN} x 0.3	V
	V_{IH}		V_{DDIN} x 0.7	—	—	V
Input resistance	R_{IN}		—	63	—	kΩ
Duty cycle	DC		40	—	60	%
Capacitance	C_{IN_SE}		—	1.25	—	pF

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Table 9. Input Specifications (Continued)

V_{DD18} = 1.8 V ±5%, V_{DDA} = V_{DDREF} = 3.3 V ±5%; All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C.
Low-Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDREF} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C.

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Other Control Input Pins (RSTb, FINC, FDEC, OE, PLLx_FORCE_HO, PLLx_INSEL[#], IN_FAIL[#])						
Update rate	f_{UR}	RSTb[6]	—	—	1	Hz
		FINC, FDEC	—	—	800	kHz
Input voltage	V_{IL}		—	—	V_{DDIO} x 0.3	V
	V_{IH}		V_{DDIO} x 0.7	—	—	V
Minimum pulse width	PW		150	—	—	ns
Programmable internal pullup, pulldown	R_{IN}		—	20	—	kΩ

1. The minimum slew rate on the XO applied to REF_IN is recommended to meet the specified jitter performance.
2. To achieve this slew rate and voltage swing, use one of the XOs from the "Si55xx, Si540x, and Si536x Recommended XTAL, XO, VCXO, TCXO, and OCXO Reference Manual" placed as close as possible to the REF_IN pins.
3. Slew rate can be estimated using the following simplified equation: SR = ((0.8 – 0.2) x $V_{IN\_VPP\_se}$)/t_r.
4. To meet specified jitter performance use one of the XTALs from the "Si55xx, Si540x, and Si536x Recommended XTAL, XO, VCXO, TCXO, and OCXO Reference Manual".
5. The minimum slew rate on the input clock applied to INx/INxb is recommended to meet the specified input-to-output delay and close-in phase noise (<1 kHz) performance.
6. Glitches and toggles on RSTb more frequent than f_{UR} may cause the device to lock up in reset. Power cycle the device to restore operation.

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Table 10. I^2C Timing Specifications (SCL, SDA)

V_{DD18} = 1.8 V ±5%, V_{DDA} = V_{DDREF} = 3.3 V ±5%; All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C.
Low-Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDREF} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C.

Parameter	Symbol	Test Condition	Standard Mode 100 kbps		Fast Mode 400 kbps		Unit
			Min	Max	Min	Max	
SCL clock frequency	f_{SCL}		—	100	—	400	kHz
SMBus timeout	—		25	35	25	35	ms
Hold time (repeated) START condition	$t_{HD:STA}$		4.0	—	0.6	—	µs
Low period of the SCL clock	t_{LOW}		4.7	—	1.3	—	µs
HIGH period of the SCL clock	t_{HIGH}		4.0	—	0.6	—	µs
Setup time for a repeated START condition	$t_{SU:STA}$		4.7	—	0.6	—	µs
Data hold time	$t_{HD:DAT}$		100	—	100	—	ns
Data setup time	$t_{SU:DAT}$		250	—	100	—	ns
Setup time for STOP condition	$t_{SU:STO}$		4.0	—	0.6	—	µs
Bus free time between a STOP and START condition	t_{BUF}		4.7	—	1.3	—	µs
Data valid time	$t_{VD:DAT}$		—	3.45	—	0.9	µs
Data valid acknowledge time	$t_{VD:ACK}$		—	3.45	—	0.9	µs

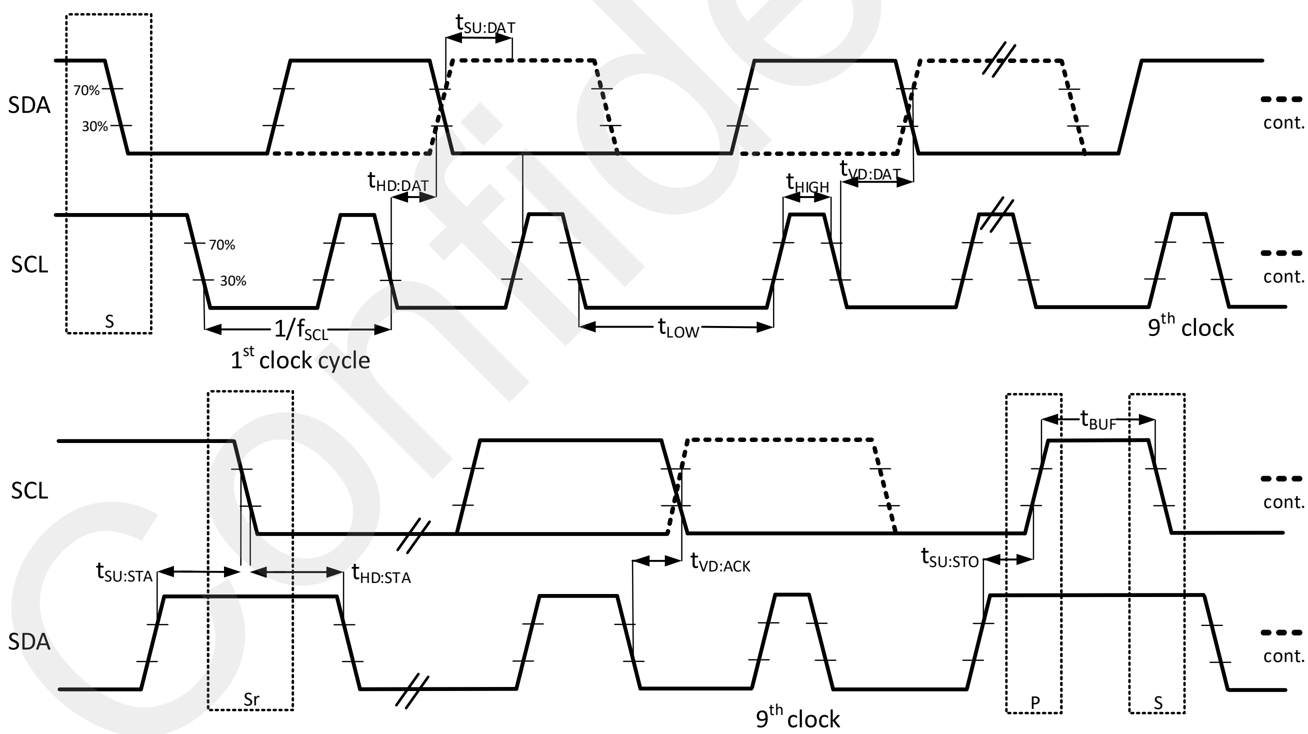

Figure 12. I^2C Serial Port Timing Standard and Fast Modes

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Table 11. SPI Timing Specifications (4-Wire)

V_{DD18} = 1.8 V ±5%, V_{DDA} = V_{DDREF} = 3.3 V ±5%; All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, TA = –40 to 95 °C.
Low-Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDREF} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C.

Parameter	Symbol	Min	Typ	Max	Unit
SCLK frequency	f_{SPI}	—	—	30	MHz
SCLK duty cycle	T_{DC}	40	—	60	%
SCLK period	T_C	33.333	—	—	ns
Delay time, SCLK fall to SDO active	T_{D1}	—	12.5	20	ns
Delay time, SCLK fall to SDO	T_{D2}	—	10	15	ns
Delay time, CSb rise to SDO tri-state	T_{D3}	—	10	20	ns
Setup time, CSb to SCLK	T_{SU1}	5	—	—	ns
Hold time, SCLK Fall to CSb	T_{H1}	5	—	—	ns
Setup time, SDI to SCLK rise	T_{SU2}	5	—	—	ns
Hold time, SDI to SCLK rise	T_{H2}	5	—	—	ns
Delay time between chip selects (CSb)	T_{CS}	5	—	—	µs

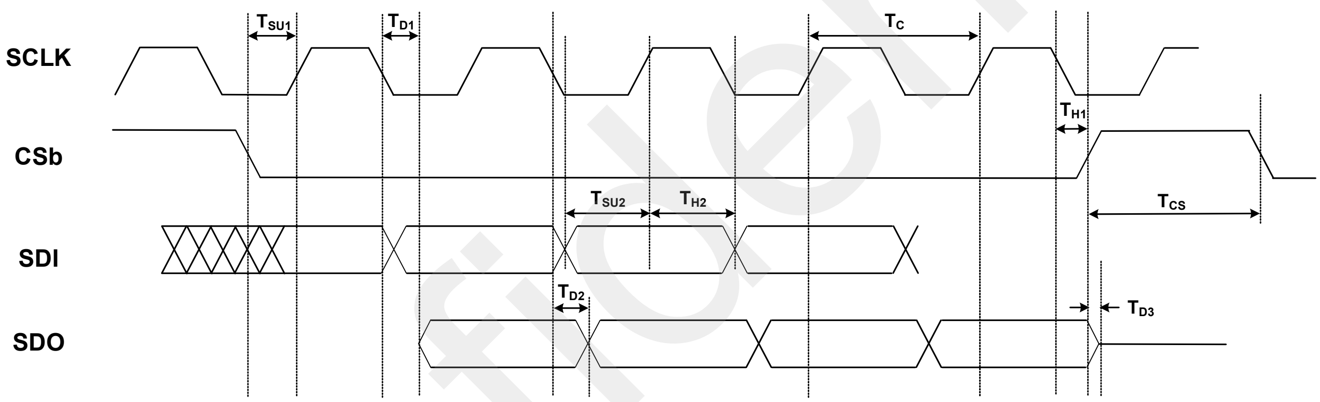

Figure 13. 4-Wire SPI Serial Interface Timing

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Table 12. SPI Timing Specifications (3-Wire)

V_{DD18} = 1.8 V ±5%, V_{DDA} = V_{DDREF} = 3.3 V ±5%; All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C.
Low-Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDREF} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C.

Parameter	Symbol	Min	Typ	Max	Unit
SCLK frequency	f_{SPI}	—	—	30	MHz
SCLK duty cycle	T_{DC}	40	—	60	%
SCLK period	T_C	33.33	—	—	ns
Delay time, SCLK fall to SDIO turn-on	T_{D1}	—	12.5	20	ns
Delay time, SCLK fall to SDIO next-bit	T_{D2}	—	10	15	ns
Delay time, CSb rise to SDIO tri-state	T_{D3}	—	10	20	ns
Setup time, CSb to SCLK	T_{SU1}	5	—	—	ns
Hold time, CSb to SCLK fall	T_{H1}	5	—	—	ns
Setup time, SDI to SCLK rise	T_{SU2}	5	—	—	ns
Hold time, SDI to SCLK rise	T_{H2}	5	—	—	ns
Delay time between chip selects (CSb)	T_{CS}	5	—	—	µs

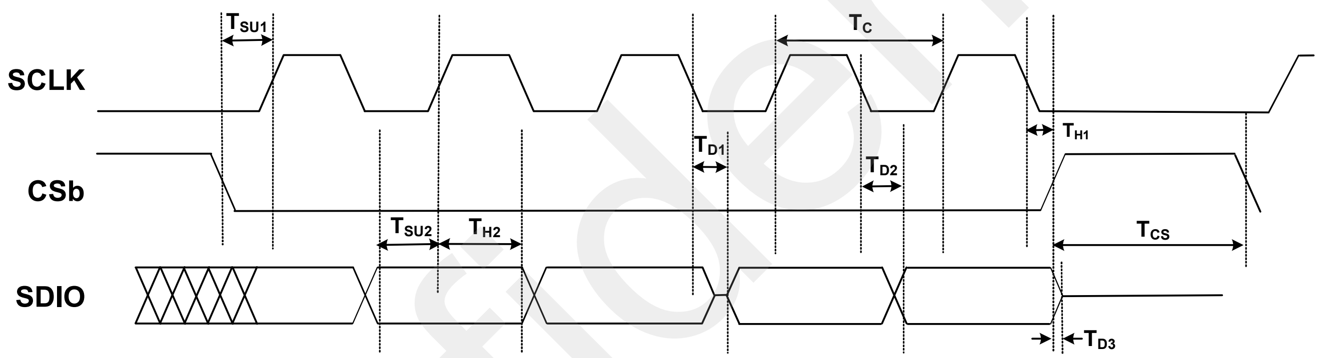

Figure 14. 3-Wire SPI Serial Interface Timing

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Table 13. Differential Clock Output Specifications

V_{DD18} = 1.8 V ±5%, V_{DDIN} = V_{DDIO} = 3.3 V ±5%, 1.8 V ±5%, V_{DDREF} = V_{DDA} = 3.3 V ±5%, V_{DDO} = 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C, Low Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDREF} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C

Parameter	Symbol	Test Condition			Min	Typ	Max	Units
Output frequency	f_{OUT}	Q Divider, Non PPS[1]			0.008	—	1228.8	MHz
		Q Divider, PPS			0.5	—	1	Hz
		NA Divider, Non PPS[2]			0.008	—	650	MHz
		NA Divider, PPS			0.5	—	1	Hz
		NB Divider[2]			0.008	—	650	MHz
Duty cycle	DC	f < 400 MHz			49.5	50	50.5	%
		400 MHz < f < 3.2 GHz			48	50	52	
Output-to-output Skew	T_{SK}	Q divider outputs, same differential format[3]			–50	—	50	ps
		Multisynth (NA or NB) outputs, same differential format, same Multisynth						
		Q divider outputs, Differential SYSCLK to LVCMOS SYNC output			0	—	300	
OUT-OUTb Skew	T_{SK_OUT}	Skew between positive and negative output pins.	VDDO = 3.3 V	LVPECL, LVDS, CML, and custom diff f < 491.52	—	—	10	ps
			VDDO = 2.5 V	LVPECL, LVDS, CML, and custom diff f < 491.52	—	—	25	
			VDDO = 3.3 V/ 2.5 V	LVPECL, LVDS, CML, and custom diff f < 491.52	—	—	25	
			VDDO = 1.8 V	CML, S-LVDS, and custom diff All Frequencies	—	—	35	
Output voltage swing[4]	V_{OUT}	VDDO = 3.3 V/2.5 V		LVDS	330 x SF	360 x SF	380 x SF	mVpp_se
		VDDO = 1.8 V		S-LVDS	350 x SF	370 x SF	410 x SF	
		VDDO = 3.3 V/2.5 V		AC-Coupled LVPECL	780 x SF	840 x SF	910 x SF	
		VDDO = 3.3 V/2.5 V/1.8 V		CML	390 x SF	420 x SF	460 x SF	
		VDDO = 3.3 V/2.5 V		Custom Diff 600 mVpp_se	560 x SF	610 x SF	650 x SF	
Output voltage swing Scaling Factor (SF) OUT0–9	SF	f < 491.52 MHz			1	1	1	SF
		491.52 MHz < f < 983.04 MHz			0.9	0.95	1	
		983.04 MHz < f < 1.47456 GHz			0.8	0.9	1	
		1.47456 GHz < f < 2.47456 GHz			0.7	0.75	0.85	
		f > 2.47456 GHz			0.5	0.6	0.75	
Output voltage swing Scaling Factor (SF) OUT10–11[5]	SF	f < 491.52 MHz			1	1	1	SF
		491.52 MHz < f < 983.04 MHz			0.9	0.95	1	
		983.04 MHz < f < 1.47456 GHz			0.8	0.9	1	
		1.47456 GHz < f < 2.47456 GHz			0.7	0.75	0.85	
		f > 2.47456 GHz			0.5	0.6	0.75	
Common-mode voltage	V_{CM}	VDDO = 3.3 V/2.5 V		LVDS, Custom Differential, CML	1.15	1.2	1.25	V
		VDDO = 1.8 V		S-LVDS, CML	0.85	0.9	0.95	
Rise and fall times (20% to 80%) OUT0–9	t_r/t_f	VDDO = 3.3 V/2.5 V		LVDS, AC Coupled LVPECL, Custom Diff	—	125	260	ps
		VDDO = 1.8 V		S-LVDS	—	150	270	
		VDDO = 3.3 V/2.5 V/1.8 V		CML	—	150	280	
Rise and fall times (20% to 80%) OUT10–11[5]	t_r/t_f	VDDO = 3.3 V/2.5 V		LVDS, AC Coupled LVPECL, Custom Diff	—	140	300	ps
		VDDO = 1.8 V		S-LVDS	—	165	310	
		VDDO = 3.3 V/2.5 V/1.8 V		CML	—	165	320	

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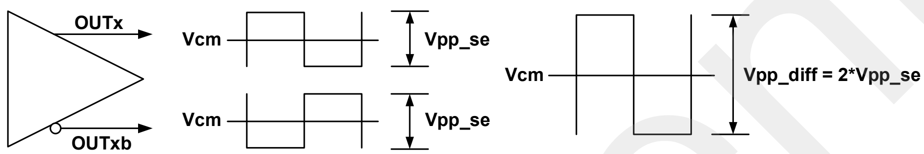
Table 13. Differential Clock Output Specifications (Continued)

V_{DD18} = 1.8 V ±5%, V_{DDIN} = V_{DDIO} = 3.3 V ±5%, 1.8 V ±5%, V_{DDREF} = V_{DDA} = 3.3 V ±5%, V_{DDO} = 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C, Low Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDREF} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Differential output impedance	Z_O	All Differential formats	—	100	—	Ω
Power supply noise rejection[6]	PSR	25 kHz sinusoidal noise	—	–96	—	dBc
		100 kHz sinusoidal noise	—	–97	—	
		500 kHz sinusoidal noise	—	–93	—	
		1 MHz sinusoidal noise	—	–93	—	
Output-to-output crosstalk[7]	$XTALK_{OUT}$	Differential outputs, same format	—	–95	—	dBc
Input-to-output crosstalk[8]	$XTALK_{IN}$	Differential input and output, same format	—	–90	—	dBc

1. Q dividers support output frequencies within the specified range equal to $f_{VCO/Q}$ where Q is an integer.
2. NA, NB Multisynths support any output frequency within the specified range.
3. SYNC outputs are not included in this output-to-output skew specification.
4. Output voltage swing is dependent on frequency range. Scale all voltage swing values by the scaling factor (SF). Voltage swing is specified in mVpp_SE as shown below.



5. OUT10/11 have programmable slew rate limit capability when configured as LVCMOS. This causes additional attenuation for higher frequency outputs. The Output Voltage Swing Scaling Factor (SF) for OUT10/OUT11 is shown below. It is recommended to use OUT0-9 for f_{OUT} > 491.52 MHz.
6. Measured for a 122.88 MHz LVDS output frequency. 100 mVpp sine wave noise added to V_{DDO} = 3.3 V and noise spur amplitude measured.
7. Crosstalk spur measured with the victim running at 153.6 MHz and the aggressor at 156.25 MHz. Victim and aggressor are separated by two unused channels.
8. Crosstalk spur measured with the victim running at 153.6 MHz on OUT0 and the aggressor at 156.25 MHz on IN3.

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Table 14. HCSL Clock Output Specifcations

V_{DD18} = 1.8 V ±5%, V_{DDIN} = V_{DDIO} = 3.3 V ±5%, 1.8 V ±5%, V_{DDREF} = V_{DDA} = 3.3 V ±5%, V_{DDO} = 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C, Low Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDREF} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C

Parameter	Symbol	Test Condition			Min	Typ	Max	Units
Output frequency	f_{OUT}	Q Divider, Non PPS[1]			0.008	—	500	MHz
		Q Divider, PPS			0.5	—	1	Hz
		NA Divider, Non PPS[2]			0.008	—	500	MHz
		NA Divider, PPS			0.5	—	1	Hz
		NB Divider[2]			0.008	—	500	MHz
Duty cycle	DC	f < 400 MHz			49.5	50	50.5	%
		400 MHz < f < 500 MHz			48	50	52	
Output-to-output Skew	T_{SK}	Q divider outputs, same differential format[3]			–50	—	50	ps
		Multisynth (NA or NB) outputs, same differential format, same Multisynth						
		Q divider outputs, Differential SYSCLK to LVCMOS SYNC output			0	—	300	
OUT-OUTb Skew	T_{SK_OUT}	Skew between positive and negative output pins.	VDDO = 3.3 V	LVPECL, LVDS, CML, and custom diff f < 491.52	—	—	15	ps
					—	—	25	
					—	—	10	
			VDDO = 2.5 V	LVPECL, LVDS, CML, and custom diff f < 491.52	—	—	15	
					—	—	30	
					—	—	20	
			VDDO = 1.8 V	CML, S-LVDS, and custom diff All Frequencies	—	—	22	
					—	—	70	
					—	—	36	
Output voltage swing[4,5]	V_{OUT}	VDDO = 3.3 V/2.5 V/1.8 V		HCSL Standard, 800 mVpp_se, int term	740 x SF	810 x SF	960 x SF	mVpp_se
		VDDO = 3.3 V/2.5 V/1.8 V		HCSL Standard, 800 mVpp_se, ext term	730 x SF	810 x SF	960 x SF	
		VDDO = 3.3 V/2.5 V		HCSL Fast, 800 mVpp_se, ext term	730 x SF	810 x SF	960 x SF	
		VDDO = 3.3 V/2.5 V		HCSL Fast, 1200 mVpp_se, ext term	1100 x SF	1175 x SF	1260 x SF	
Output Voltage Swing Scaling Factor (SF) Standard, 800 mVpp_se, int term OUT0-11	SF	f < 10 MHz			1	1	1	SF
		10 MHz < f < 100 MHz			0.91	0.94	0.95	
		100 MHz < f < 200 MHz			0.89	0.91	0.93	
		200 MHz < f < 400 MHz			0.83	0.85	0.92	
		f > 400 MHz			0.74	0.78	0.89	
Output voltage swing Scaling Factor (SF) Standard, 800 mVpp_se, ext term, OUT0-11	SF	f < 10 MHz			1	1	1	SF
		10 MHz < f < 100 MHz			0.97	0.96	0.97	
		100 MHz < f < 200 MHz			0.94	0.93	0.95	
		200 MHz < f < 400 MHz			0.91	0.90	0.88	
		f > 400 MHz			0.68	0.71	0.75	
Output voltage swing Scaling Factor (SF) Fast, 800 or 1200 mVpp_se, ext term OUT0-11	SF	f < 10 MHz			1	1	1	SF
		10 MHz < f < 100 MHz			0.98	0.99	0.99	
		100 MHz < f < 200 MHz			0.94	0.94	0.96	
		200 MHz < f < 400 MHz			0.94	0.95	0.97	
		f > 400 MHz			0.89	0.92	0.95	
Common-mode voltage	V_{CM}	VDDO = 3.3 V/2.5 V/1.8 V		HCSL 800 mVpp_se	0.35	0.425	0.52	V
		VDDO = 3.3 V/2.5 V		HCSL 1200 mVpp_se	0.55	0.6	0.68	

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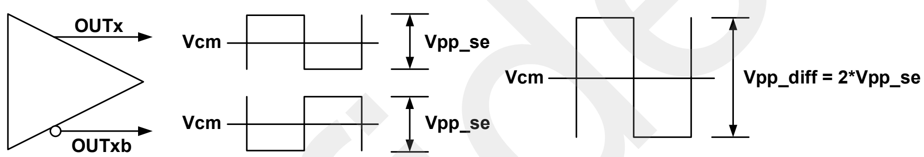
Table 14. HCSL Clock Output Specifcations (Continued)

V_{DD18} = 1.8 V ±5%, V_{DDIN} = V_{DDIO} = 3.3 V ±5%, 1.8 V ±5%, V_{DDREF} = V_{DDA} = 3.3 V ±5%, V_{DDO} = 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C, Low Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDREF} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C

Parameter	Symbol	Test Condition		Min	Typ	Max	Units
Rise and fall times (20% to 80%) OUT0–9	t_r/t_f	VDDO = 3.3 V/2.5 V/1.8 V	LVDS, AC Coupled LVPECL, Custom Diff	—	125	260	ps
		VDDO = 3.3 V/2.5 V/1.8 V	S-LVDS	—	150	270	
		VDDO = 3.3 V/2.5 V/1.8 V	CML	—	150	280	
Rise and fall times (20% to 80%) OUT10–11	t_r/t_f	VDDO = 3.3 V/2.5 V/1.8 V	HCSL Fast, 800 or 1200 mVpp_se, ext term	—	285	400	ps
		VDDO = 3.3 V/2.5 V/1.8 V	HCSL Standard, 800mVpp_se, ext term	—	465	740	
		VDDO = 3.3 V/2.5 V/1.8 V	HCSL Standard, 800mVpp_se, int term	—	285	460	
Differential output impedance	Z_O	HCSL Standard Slew Rate, int term		—	100	—	Ω
		HCSL Standard Slew Rate, ext term		—	Hi-Z	—	
		HCSL Fast Slew Rate, ext term		—	200	—	
Output-to-output crosstalk[6]	$XTALK_{OUT}$	HCSL outputs, same format		—	–95	—	dBc
Input-to-output crosstalk[7]	$XTALK_{IN}$	HCSL input and output, same format		—	–90	—	dBc

1. Q dividers support output frequencies within the specified range equal to $f_{VCO/Q}$ where Q is an integer.
2. NA, NB Multisynths support any output frequency within the specified range.
3. SYNC outputs are not included in this output-to-output skew specification.
4. Output voltage swing is dependent on frequency range. Scale all voltage swing values by the scaling factor (SF). Voltage swing is specified in mVpp_SE as shown below.



5. OUT10/11 have programmable slew rate limit capability when configured as LVCMOS. This causes additional attenuation for higher frequency outputs. The Output Voltage Swing Scaling Factor (SF) for OUT10/OUT11 is shown below. It is recommended to use OUT0-9 for f_{OUT} > 491.52 MHz.
6. Crosstalk spur measured with the victim running at 153.6 MHz and the aggressor at 156.25 MHz. Victim and aggressor are separated by two unused channels.
7. Crosstalk spur measured with the victim running at 153.6 MHz on OUT0 and the aggressor at 156.25 MHz on IN3.

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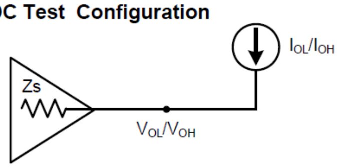
Table 15. LVCMOS Clock Output Specifications

V_{DD18} = 1.8 V ±5%, V_{DDA} = V_{DDREF} = 3.3 V ±5%; All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C.
Low Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDREF} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C.

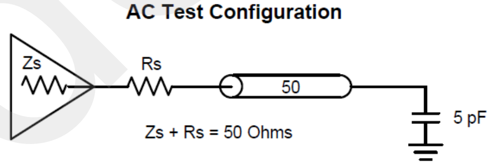
Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Output frequency	f_{OUT}	Q Divider, Non PPS[1]	0.008	—	250	MHz
		Q Divider, PPS	0.5	—	1	Hz
		NA Divider, Non PPS[2]	0.008	—	250	MHz
		NA Divider, PPS	0.5	—	1	Hz
		NB Divider[2]	0.008	—	250	MHz
Duty cycle	DC	f < 100 MHz	49.5	—	50.5	%
		100 MHz < f < 250 MHz	45	—	55	
Output voltage high[3]	V_{OH}	VDDO = 3.3 V/2.5 V/1.8 V I_{OH} = –8/–6/–4 mA, I_{OL} = 8/6/4 mA	V_{DDO} x 0.85	—	—	V
Output voltage low[3]	V_{OL}		—	—	V_{DDO} x 0.15	V
Rise and fall times (20% to 80%)[4,5,6]	t_r/t_f	LVCMOS	0.35	0.8	1.35	ns
		SRL LVCMOS "4 ns rise/fall"	3	4	6	
		SRL LVCMOS "6.5 ns rise/fall"	4	6.5	10	
		SRL LVCMOS "13 ns rise/fall"	7	13	24	
		SRL LVCMOS "25 ns rise/fall"	13	25	42	

1. Q dividers support output frequencies within the specified range equal to $f_{VCO/Q}$ where Q is an integer.
2. NA, NB Multisynths support any output frequency within the specified range.
3. V_{OL} /V_{OH} is measured at I_{OL} /I_{OH} as shown in the DC Test Configuration below.
4. A 15 to 25 Ω series termination resistor (RS) is recommended to help match the source impedance to a 50 Ω PCB trace. A 5 pF capacitive load is assumed as shown in the AC Test Configuration below.

DC Test Configuration



AC Test Configuration



5. Slew Rate Limited (SRL) LVCMOS format only available on OUT10/OUT11.
6. SRL LVCMOS format clocks are intended only for low-frequency clock applications. Refer to the "Si5518/12/10/08 Reference Manual" for the maximum Fout supported for each slew rate selection.

Table 16. Output Status Pin Specifications

V_{DDIO} = 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C.
Low-Power Mode: V_{DDIO} = 1.8 V ±5%.

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Serial and Status Output Pins (GPIO, SDA/SDIO, SDO)						
Output voltage high	V_{OH}[1]	I_{OH} = –2 mA	V_{DDIO} x 0.85	—	—	V
Output voltage low	V_{OL}	I_{OL} = 2 mA	—	—	V_{DDIO} x 0.15	V

1. The V_{OH} specification does not apply to the open-drain SDA output when the serial interface is in I^2C mode. V_{OL} remains valid in all cases.

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Table 17. Performance Characteristics

V_{DD18} = 1.8 V ±5%, V_{DDA} = V_{DDREF} = 3.3 V ±5%; All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C.
Low-Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDREF} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C.

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Initial start-up time	t_{START_XO}	Time from POR to when the device generates free-running clocks from NVM frequency plan	—	25	40	ms
	t_{START_XTAL}		—	120	270	
	t_{RDY}	POR to API ready	—	25	30	
PLL lock time	t_{ACQ_DSPLL}[1]	RFPLL, IN = 19.44 MHz, BW = 100 Hz, FLOL De-assert	—	230	350	ms
		RFPLL, IN = 19.44 MHz, BW = 100 Hz, LOL De-assert	—	1.3	1.6	s
		DSPLLA/B, IN = 156.25 MHz, BW = 3 Hz, FLOL De-assert	—	190	240	ms
		DSPLLA/B, IN = 156.25 MHz, BW = 3 Hz, LOL De-assert	—	1.3	1.6	s
	t_{ACQ_PPS}[2]	PPSPLL, IN = 1PPS, BW = 12.5 mHz, Coarse LOL De-assert	—	26	28	s
		PPSPLL, IN = 1PPS, BW = 12.5 mHz, Fine LOL De-assert	—	35	37	
		PPSPLL, IN = PP2S, BW = 12.5 mHz, Coarse LOL De-assert	—	53	56	
		PPSPLL, IN = PP2S, BW = 12.5 mHz, Fine LOL De-assert	—	69	72	
Output delay adjustment	t_{QDIV}	Range[3]	$–T_{VCO}$ x 127	—	$+T_{VCO}$ x 127	ps
		Resolution		T_{VCO}	—	
		Resolution (fine delay enabled)		$T_{VCO}/4$	—	
Jitter peaking	J_{PK}	All PLLs	—	—	0.1	dB
Max phase transient during hitless switch[4]	t_{SWITCH}		—	35	150	ps
Pull-in range	ω_P		—	±100	—	ppm
Input-to-output delay + variation[5,6]	$t_{IODELAY}$	DSPLL A in Dual-Reference Mode or RFPLL in Single-Reference Mode[7]	–400	—	400	ps
	t_{ZDELAY}	ZDM: 1PPS, PP2S	–200	—	200	
		ZDM: f_{IN} > 8 kHz	–100	—	100	
Input-to-output delay variation[8]	$t_{VIODELAY}$	DSPLL A in Single-Reference Mode or DSPLL B	–500	—	500	
RMS jitter performance[9] 12 kHz to 20 MHz	J_{GEN_XO}[10]	491.52 MHz, Q div	—	47	70	fs
		156.25 MHz, NA or NB div	—	91	135	

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Table 17. Performance Characteristics (Continued)

V_{DD18} = 1.8 V ±5%, V_{DDA} = V_{DDREF} = 3.3 V ±5%; All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C.
Low-Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDREF} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C.

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Phase noise performance[11]	PN_491.52M_XO_Q_Div[10]	10 Hz	—	–79	—	dBc/Hz
		100 Hz	—	–107	—	
		1 kHz	—	–127	—	
		10 kHz	—	–135	—	
		100 kHz	—	–138	—	
		800 kHz	—	–145	—	
		1 MHz	—	–146	—	
		10 MHz	—	–161	—	
		40 MHz	—	–164	—	

1. FLOL de-asserts once frequency lock is achieved. LOL de-asserts once both frequency and phase lock are achieved. Refer to “3.13.2. Lock Acquisition Mode” on page 19 for more details on LOL thresholds.
2. PPSPLL lock time specified for frequency plans with a greatest common divisor of SYSCLK frequencies greater than or equal to 960 kHz. Coarse lock is declared once the PPSPLL has steered the output phase to within 500 ns of the input phase. Fine lock is declared when the output phase is within 30 ns of the input phase. For more details on PPSPLL lock times, see the “Si5518/12/10/08 Reference Manual”.
3. Output delay adjustment range will vary depending on frequency plan. Output delay adjust range (ns) is displayed in the “Output Skew Control” step of the ClockBuilder Pro Wizard. FVCO range is 10.4 GHz to 13 GHz.
4. Phase transient specification only applies to clock switches between two synchronous inputs to a DSPLL configured for a phase build-out clock switching mode in ClockBuilder Pro.
5. Input-to-output (IO) delay is measured at the output driver with respect to the input after the output phase has achieved a steady state value. This spec excludes wander from the OCXO/TCXO.
6. IO delay requires clock switching to be configured for Phase Pull-in in ClockBuilder Pro. IO delay is not specified for phase build-out (hitless) clock switching mode.
7. Input-to-output delay in these modes is only specified for outputs derived from Q dividers or the NA divider.
8. Only IO delay variation is specified for these DSPLL configurations. Absolute delay is dependent on frequency plan.
9. Added jitter and spurs due to crosstalk are frequency-plan-dependent and can be determined using the ClockBuilder Pro Spur Analysis tool.
10. Jitter generation conditions: XO = 54 MHz TXC 7X54070001, f_{IN} = 156.25 MHz, LVPECL output format, RF DSPLL BW = 40 Hz.
11. An SMA-100a low-noise signal generator is used as the input to the RF DSPLL for phase noise performance. Specified phase noise does not include phase noise of an oscillator (TCXO/OCXO) applied to the RFPLL.

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5. Standards Compliance

DSPLL A, DSPLL B, and PPSPLL can be configured to support the requirements of the ITU-T standards shown in the following table.

Table 18. Supported ITU-T Standards

ITU-T Standard	Options	Comment
G.8262	EEC Option 1	SDH. SyncE. Based on G.813 Option 1.
	EEC Option 2	SDH. SyncE. Based on G.812 Type IV.
G.8262.1	eEEC	Enhanced SyncE.
G.8273.1	N/A	Grandmaster T-GM
G.8273.2	N/A	Supported with and without SyncE. T-TSC and T-BC.
G.8273.4	N/A	Assisted Partial Timing Support (APTS). T-TSC-A and T-TBC-A.

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6. Typical Operating Characteristics

The phase noise plots shown in Figure 15 and Figure 16 were taken under the following conditions:
f_{IN} = 156.25 MHz; f_{OUT} LVDS, RF DSPLL BW = 40 Hz, XO = 54 MHz TXC 7X54070001, T_A = 25 °C for XO.

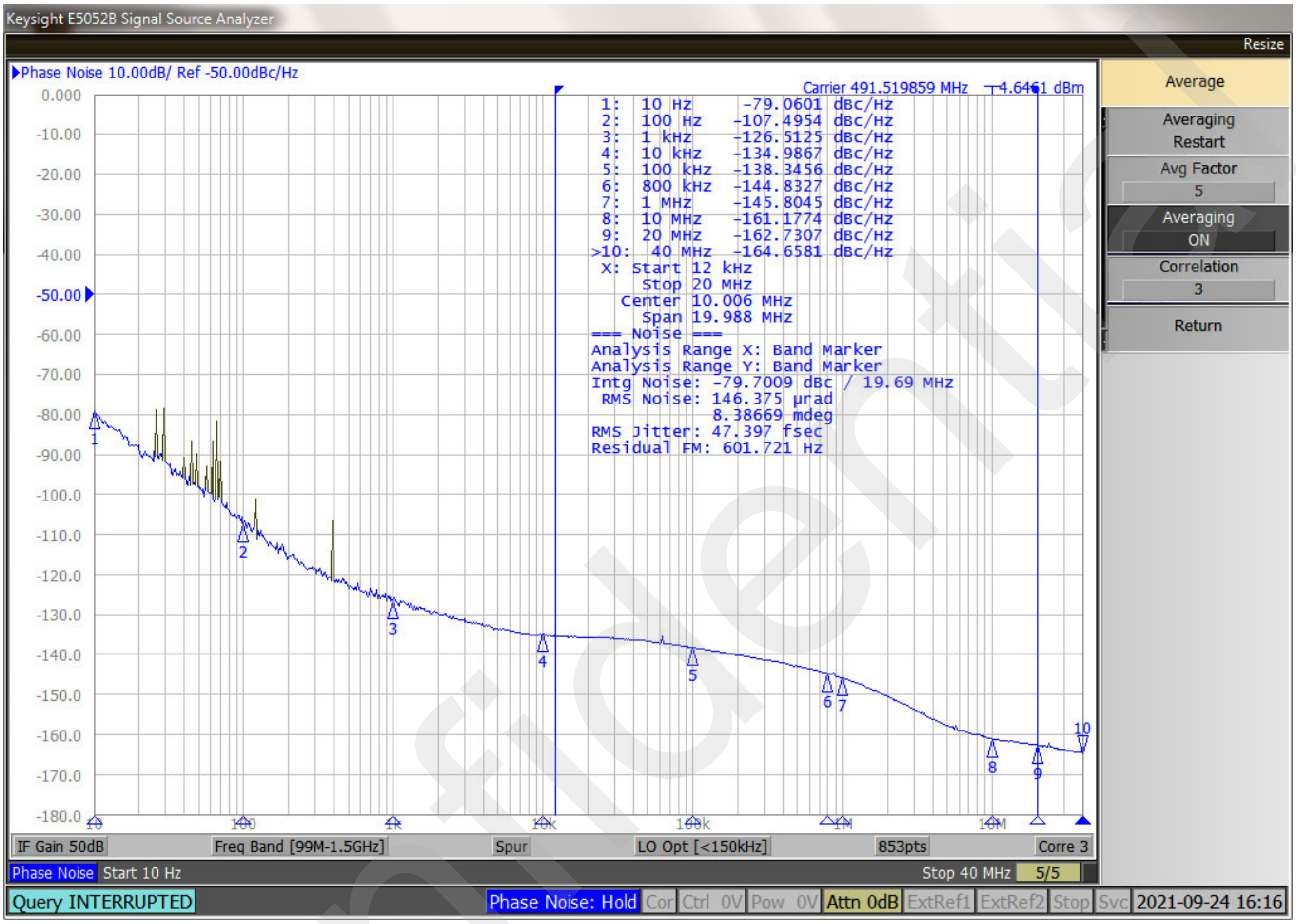

Figure 15. XO Configuration, f_{IN} = 156.25 MHz, f_{OUT} = 491.52 MHz

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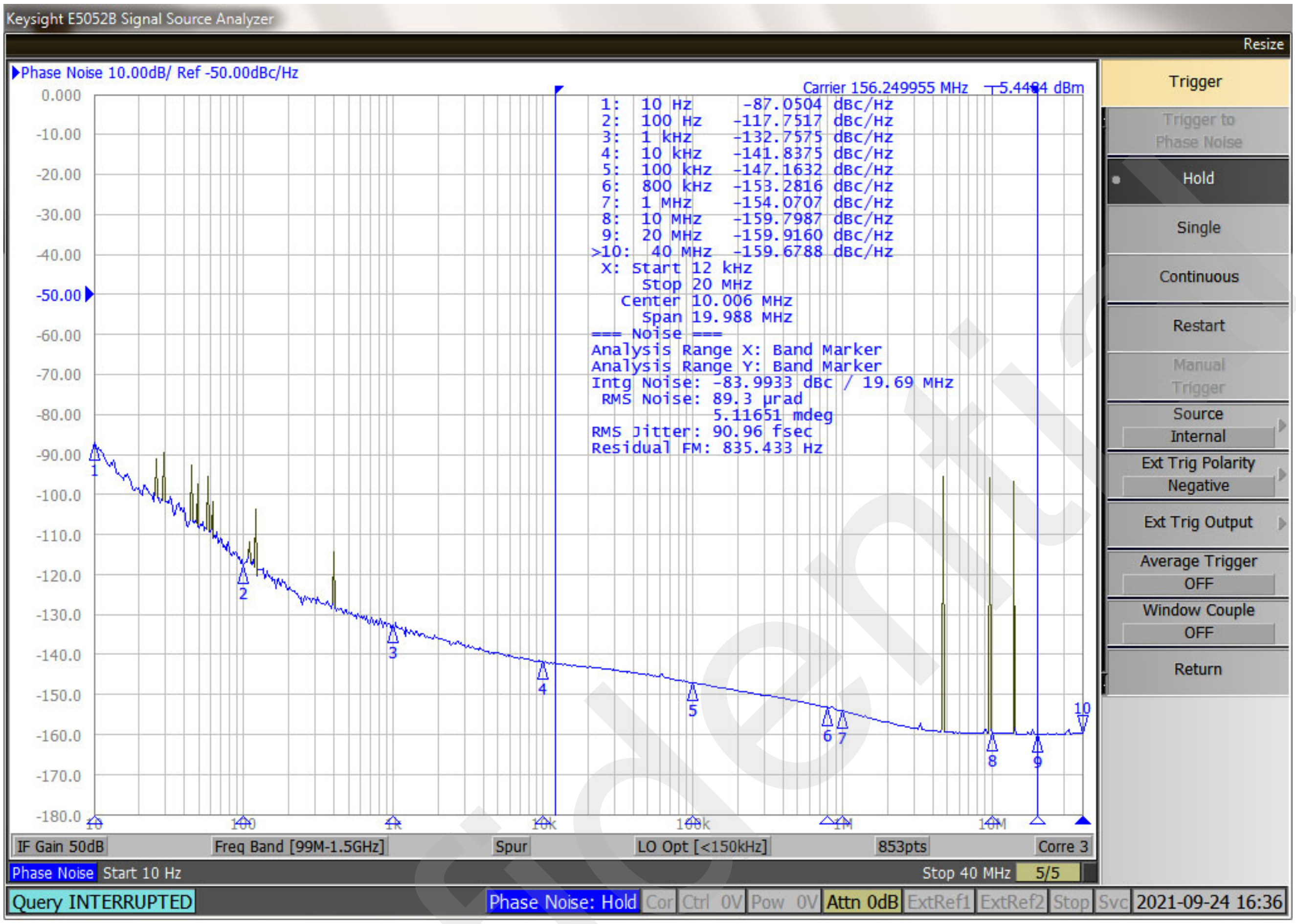

Figure 16. XO Configuration, f_{IN} = 156.25 MHz, f_{OUT} = 156.25 MHz

7. Pin Descriptions

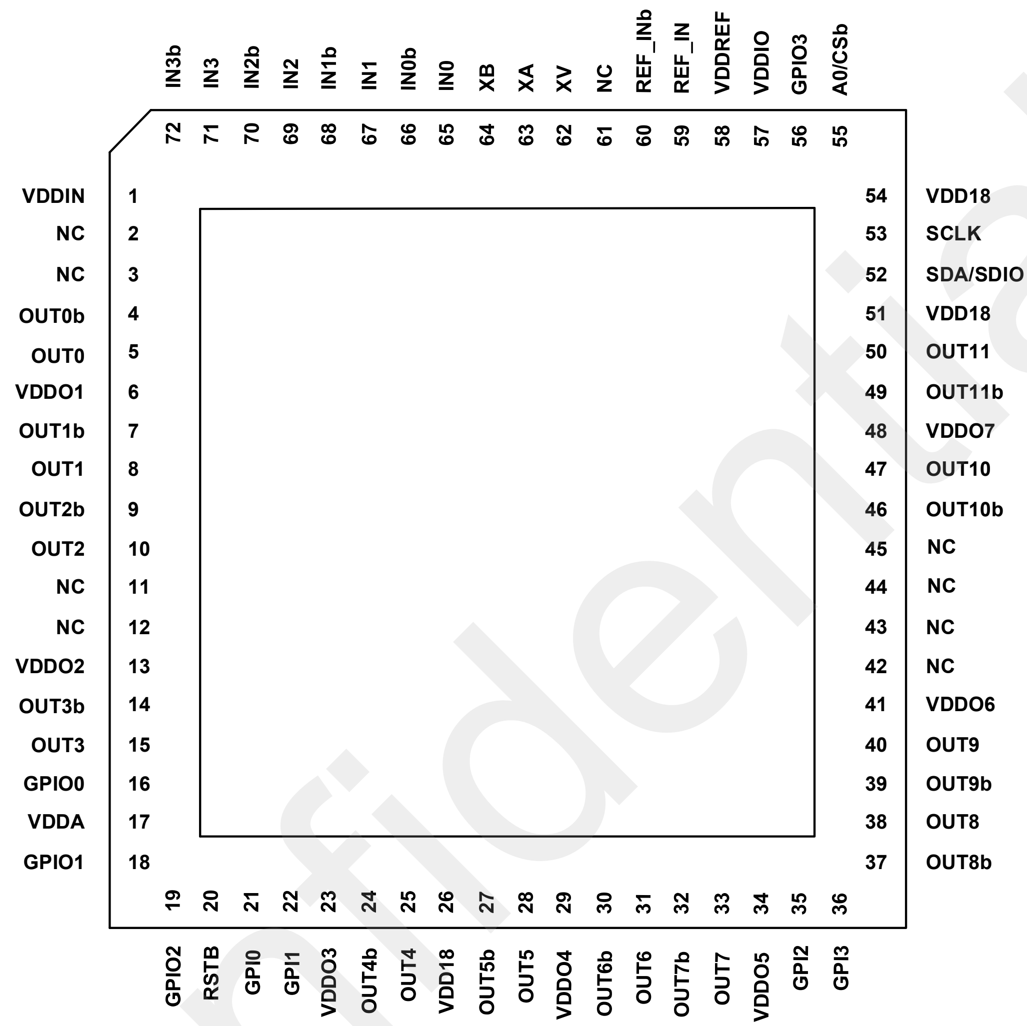

Figure 17. Si5512 72 QFN Pinout

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Table 19. Si5512 72 QFN Pin Descriptions

Pin Name	Pin Number	Pin Type[1]	Function
Inputs			
REF_IN	59	I	Input for external low phase noise reference (XO).
REF_INb	60		
XV	62	I	**XTAL Shield** Connect this pin directly to the XTAL shield. Do not ground the XV pin. XV should be isolated from the PCB ground plane. For layout guidelines, refer to "AN1293: Si55xx Schematic Design and Board Layout Guide".
XA	63	I	**Crystal Input** Input pins for external crystal (XTAL). XA and XB pins can be left unconnected when not in use.
XB	64		
IN0	65	I	**Clock Inputs** IN0–IN3 accept an input clock for synchronizing the device. They support both differential and single-ended clock signals. When operating in Single-Ended Mode, inputs IN2 and IN3 can provide two SE inputs each for a total of six inputs. Refer to the "Si5518/12/10/08 Reference Manual" and "AN1293: Si55xx Schematic Design and Board Layout Guide" for input termination options. These pins are high-impedance and must be terminated externally. IN0–IN3 can be disabled in ClockBuilder Pro and the pins left unconnected if unused.
IN0b	66		
IN1	67		
IN1b	68		
IN2	69		
IN2b	70		
IN3	71		
IN3b	72		
General Purpose Inputs (GPI)			
GPI0	21	I or NC	GPI0–GPI3 are General-Purpose Inputs (GPIs) that can be programmed to have any of the input control functions listed in "3.11. GPIO Pins (General Purpose Input or Output)" on page 17. When unused, these pins can be left unconnected. Power Supply to Pins 21 and 22 is VDDO3, and for Pins 35 and 36 it is VDDO5.
GPI1	22		
GPI2	35		
GPI3	36		
Outputs			
OUT0b	4	O	**Output Clocks** The output clocks can be programmed as single-ended CMOS or differential LVDS, S-LVDS, CML, HCSL or ac-coupled LVPECL and support a programmable signal amplitude and common-mode voltage. Desired output signal format is configurable in ClockBuilder Pro. Termination recommendations are provided in the "Si5518/12/10/08 Reference Manual". **Unused outputs should be left unconnected**.
OUT0	5		
OUT1b	7		
OUT1	8		
OUT2b	9		
OUT2	10		
OUT3b	14		
OUT3	15		
OUT4b	24	O	
OUT4	25		
OUT5b	27		
OUT5	28		
OUT6b	30		
OUT6	31		
OUT7b	32		
OUT7	33		
OUT8b	37		
OUT8	38		
OUT9b	39		
OUT9	40		
OUT10b	46	O	**Output Clocks with Programmable CMOS Slew Rate** When Outputs 10 and 11 are configured as CMOS outputs, they can also have the slew rate adjusted. Because of this, they do not support glitchless pulsed SYSREF Mode. Continuous SYSREF Mode is supported.
OUT10	47		
OUT11b	49		
OUT11	50		
Serial Interface			

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Table 19. Si5512 72 QFN Pin Descriptions

Pin Name	Pin Number	Pin Type[1]	Function
SDA/SDIO	52	I/O	**Serial Data Interface** This is the bidirectional data pin (SDA) for the I^{2}C Mode or the bidirectional data pin (SDIO) in the 3-wire SPI Mode, or the input data pin (SDI) in the 4-wire SPI Mode. When in I^{2}C Mode, this pin must be pulled-up using an external resistor of at least 1 kΩ. No pull-up resistor is needed when in SPI Mode.
SCLK	53	I	**Serial Clock Input** This pin functions as the serial clock input for both I^{2}C and SPI modes. When in I^{2}C Mode, this pin must be pulled-up using an external resistor of at least 1 kΩ. No pull-up resistor is needed when in SPI Mode.
A0/CSb	55	I	**Address Select 0/Chip Select** This pin functions as the hardware controlled lsb of the device address (A0) in I^{2}C Mode. In SPI Mode, this pin functions as the chip select input (active low). This pin is internally pulled-up and can be left floating if unused.
GPIO3 (A1/SDO)	56	O	**Address Select 1/ Serial Data Output/GPIO3** This input pin operates as the hardware controlled next to the lsb portion of the device address (A1) in I^{2}C Mode. In 4-wire SPI Mode this pin operates as the serial data output (SDO). In 3-wire SPI Mode this pin can function as an additional GPIO pin (GPIO3).
Control/Status			
GPIO0	16	I or O	**Programmable General Purpose Input or Outputs** These pins can be programmed to the functions defined in Table 2, "GPIO Pin Descriptions," on page 17.
GPIO1	18		
GPIO2	19		
RSTb	20	I	**Reset Pin** This pin functions as an active-low reset input and is used to generate a device reset when held low for at least the specified Minimum Pulse Width. This resets the device back to a known state and reloads the NVM frequency plan and application. All clocks will stop while the RSTb pin is asserted. If there is no frequency plan in NVM, the reset pin will return the device to the bootloader state in which it is waiting for the frequency plan and application to be downloaded by the host controller. This pin accepts a CMOS input and is internally pulled up with a ~20 kΩ resistor to VDDIO. VDDA and VDD18 must be powered up and stable before releasing RSTb. RSTb must not be toggled faster than the maximum update rate (f_{UR}) specification. Refer to "AN1293: Si55xx Schematic Design and Board Layout Guidelines" for more details on RSTb pin circuitry.
Power			
VDDIN	1	P	**Input Clock Supply Voltage** Supply voltage 3.3 V, 2.5 V or 1.8 V for the input clock buffers.
VDDO1	6	P	**Output Clock Supply Voltage 1–7** Supply voltage 3.3 V, 2.5 V, or 1.8 V for outputs. Leave VDDO pins of unused output drivers unconnected. An alternate option is to connect the VDDO pin to a power supply and disable the output driver to minimize current consumption. A 0402 1 µF capacitor should be placed very near each of these pins. VDDO may not exceed VDDA. The banks of outputs are powered as follows: VDDO1 – OUT[0:2] VDDO2 – OUT[3] VDDO3 – OUT[4 and Pins 21 and 22 when used as GPI] VDDO4 –OUT[5:6] VDDO5 – OUT[7 and Pins 35 and 36 when used as GPI] VDDO6 –OUT[8:9] VDDO7 –OUT[10:11] Data sheet jitter performance requires all outputs in a given bank to operate at a single frequency.
VDDO2	13		
VDDO3	23		
VDDO4	29		
VDDO5	34		
VDDO6	41		
VDDO7	48		
VDDA	17	P	**Core Analog Supply Voltage** This core supply can operate from a 3.3 V or 1.8 V power supply for Low-Power Mode. Note that all other supply voltages must be equal or lower voltage than the VDDA pin; so, in Low-Power Mode, no other supply can exceed 1.8 V. A 0402 1 µF capacitor should be placed very near each of these pins.

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Table 19. Si5512 72 QFN Pin Descriptions

Pin Name	Pin Number	Pin Type[1]	Function
VDD18	26	P	**Core Supply Voltage 1.8 V** The device core operates from a 1.8 V supply. A 0402 1 µF capacitor should be placed very near each of these pins.
VDD18	51		
VDD18	54		
VDDIO	57		**Control, Status IO Clock Supply Voltage** Supply voltage 3.3 V, 2.5 V, or 1.8 V for the serial interface, Control, and Status inputs and outputs.
VDDREF	58		**Reference Supply Voltage** Supply voltage of 3.3 V or 1.8 V supported for the reference. For best performance, VDDREF should be the same voltage as VDD_XO.
GND PAD	Package Bottom	P	**Exposed Die Attach Pad** The exposed die attach pad (ePAD) on the bottom of the package must be connected to electrical ground.
No Connect			
NC	11	NC	No Connect (NC)
NC	12		
NC	42		
NC	43		
NC	44		
NC	45		
NC	61		
NC	62		
NC	63		

1. I = Input; O = Output; P = Power; NC = No Connect.

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8. Package Outline

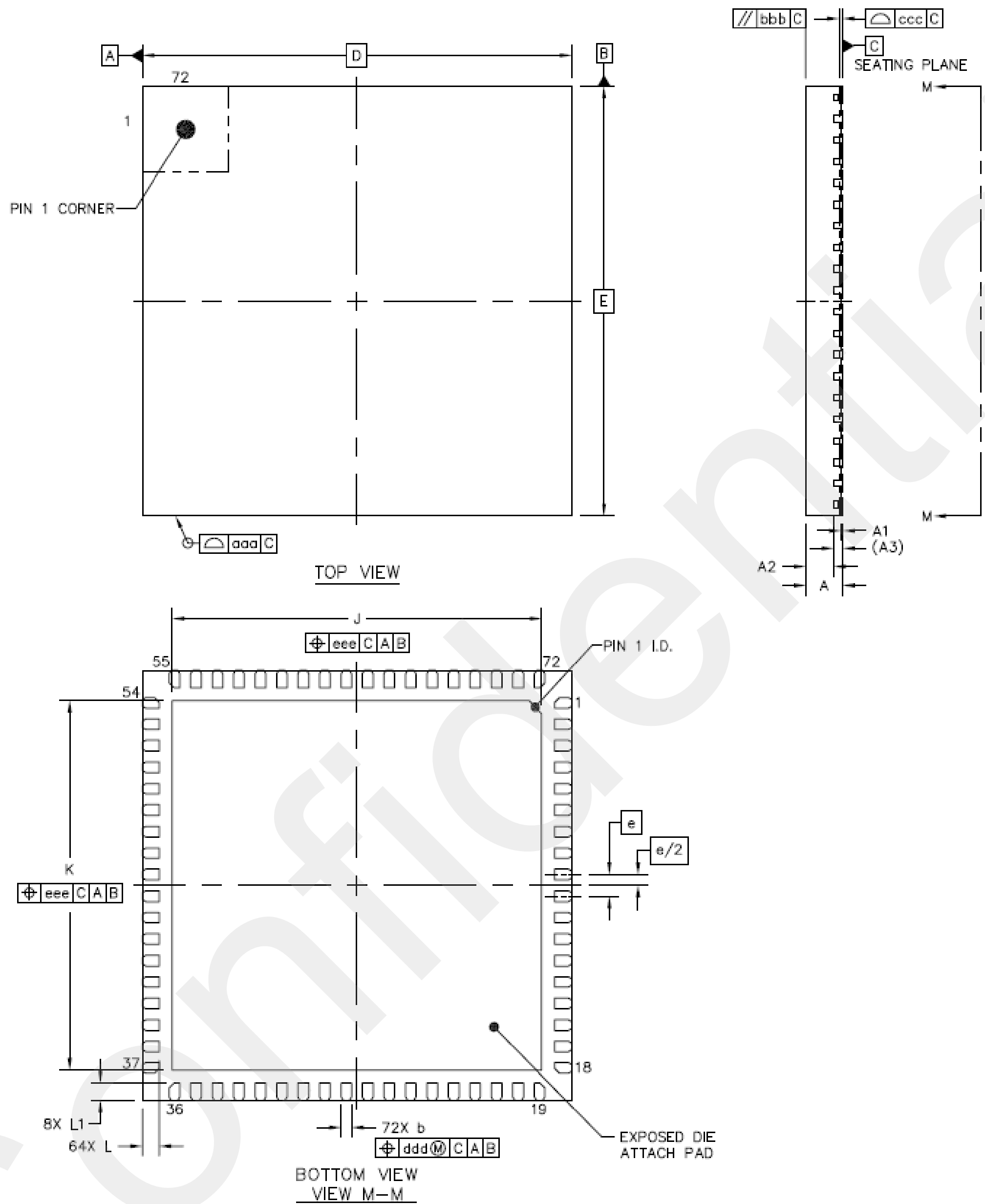

Figure 18. 72-QFN Package Diagram

Table 20. Package Dimensions[1,2,3]

		Symbol	Min	Typ	Max
Total thickness		A	0.8	0.85	0.9
Stand off		A1	0	0.035	0.05
Mold thickness		A2	—	0.65	—
L/F thickness		A3		0.203 REF	
Lead width		b	0.2	0.25	0.3
Body size	X	D		10 BSC	
	Y	E		10 BSC	
Lead pitch		e		0.5 BSC	
EP size	X	J	8.5	8.6	8.7
	Y	K	8.5	8.6	8.7
Lead length		L	0.35	0.4	0.45
		L1	0.3	0.4	0.45
Package edge tolerance		aaa		0.1	
Mold flatness		bbb		0.1	
Coplanarity		ccc		0.08	
Lead offset		ddd		0.1	
Exposed pad offset		eee		0.1	
Weight		N/A	—	0.35 g	—

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Solid State Outline MO-220.

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9. PCB Land Pattern

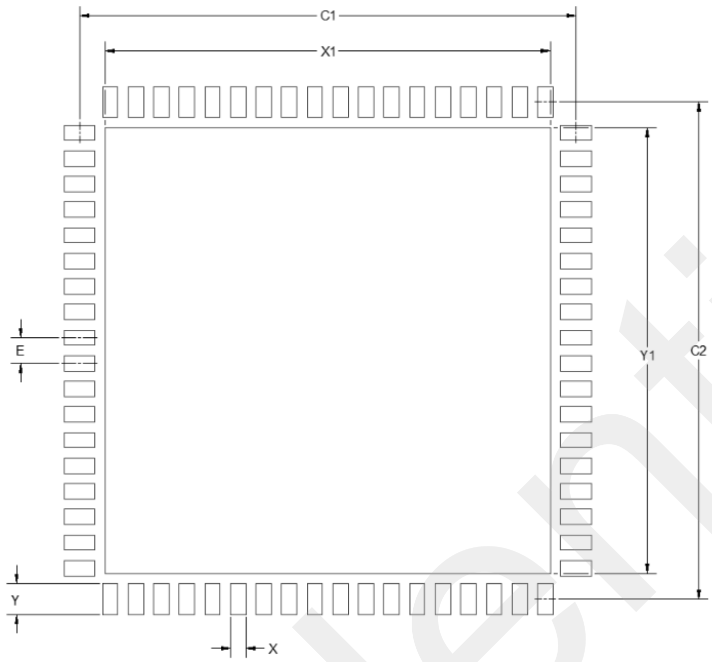

Figure 19. PCB Land Pattern

Table 21. PCB Land Pattern Dimensions

<table>
<tr><th>Dimension</th><th>mm</th><th>Notes</th></tr>
<tr><td>C1</td><td>9.70</td><td rowspan="7">General
1. These notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine tune their SMT process as required for their application and tooling.
2. All dimensions shown are in millimeters (mm).
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.
Solder Mask Design
1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
Stencil Design
1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all pads.
4. A 4x4 array of 1.45 mm square openings on a 2.00 mm pitch should be used for the center ground pad.
Card Assembly
1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.</td></tr>
<tr><td>C2</td><td>9.70</td></tr>
<tr><td>E</td><td>0.50</td></tr>
<tr><td>X</td><td>0.30</td></tr>
<tr><td>Y</td><td>0.60</td></tr>
<tr><td>X1</td><td>8.70</td></tr>
<tr><td>Y1</td><td>8.70</td></tr>
</table>

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10. Top Marking

Figure 20. Si5512 Top Marking

Table 22. Top Marking Explanation

Line	Characters	Description
1	Si5512A-	Base part number and Device Grade: A = Device Grade. (Refer to 2. Ordering Guide for latest device grade information).
2	Rxxxxx-GM	R = Product revision. (Refer to 2. Ordering Guide for latest revision). xxxxx = Customer specific NVM sequence number. Optional NVM code assigned for custom, factory preprogrammed devices. Characters are not included for standard, factory default configured devices. See 2. Ordering Guide for more information. -GM = Package (QFN) and temperature range (–40 to +95 °C)
3	YYWWTTTTTT	YYWW = Characters correspond to the year (YY) and work week (WW) of package assembly. TTTTTT = Manufacturing trace code.
4	Circle w/ 0.6 mm (72-QFN) diameter	Pin 1 indicator; left-justified
	e3 TW	Pb-free symbol; Center-Justified TW = Taiwan; Country of Origin (ISO Abbreviation)

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11. Revision History

Revision	Date	Description
B	November, 2023	• Added watermark
A	November, 2023	• Minor updates to data sheet, including figures and tables each being separately sequential numbering. • Data sheet front page – Key Points. - Removed G.8273.1 from supported ITU standards as it is a supported profile. • "1. Feature List" on page 3. - Changed last bullet of RFPLL (RF DSPLL) text to correct typos: - Selectable jitter attenuation bandwidth: 10 Hz to 400 Hz, 10 Hz to 400 Hz Dual Reference JA. • "2. Ordering Guide" on page 4. - Note 7 - Changed Xilinx to AMD. • "3.3. Inputs" on page 7. - Figure 3, "Input Structure," on page 7. - Added PHMON to Input Monitors. • "3.5.3. Slew Rate Limited (SRL) LVCMOS Outputs" on page 11 - Added last paragraph to incorporate information found in other application notes, reference manuals, and support documents. • "3.12. Device Initialization and Reset" on page 18. - Clarified section by added new sentence "All clocks will stop during a hard reset" after sentence "A hard reset is initiated using RSTb pin or through the Device API RESTART command." And referenced "A hard reset is initiated using RSTb pin or through the Device API RESTART command". • "3.18. NVM Programming" on page 26. - Fixed typos. • "3.19. Application Programming Interface (API)" on page 26. - Clarified that the secondary serial port only supports SPI 3-wire. • "3.21. Power Supplies" on page 27 - Referenced "AN1293: Si55xx Schematic Design and Board Layout Guidelines" instead of the Si55xx Reference Manual. • "3.21.2. Power Supply Ramp Rate" on page 28. - Referenced Table 8, "DC Characteristics," on page 31 for supply voltage ramp rate. • "3.21.3. Low-Power Mode" on page 28. - Added statement in text as a reminder to customers that NVM programming is not possible in low-power mode as VDDA must be at 3.3 V. • Table 8. DC Characteristics. - Core Supply Current (V_{DD18} + V_{DDA}) Parameter. - I_{DD18} Symbol Test Condition - Added Note 2 to Si5512[1,2]. - Deleted Si5512 Low Power Mode row. - I_{DDA} Symbol Test Condition - Added Note 2 to Si5512[1,2]. - Deleted Si5512 Low Power Mode[2] row. - Periphery Supply Current parameter. - I_{DDIN} + I_{DDIO} Symbol Test Condition. - Added Note 2 to Si5512[1,2]. - Deleted Si5512 Low Power Mode row. - I_{DDREF} Symbol Test Condition. - Added Note 2 to Si5512[1,2]. - Deleted Si5512 Low Power Mode row. - Output Buffer supply current (VDDOX) Parameter, following test conditions. - LVPECL (2.5 V, 3.3 V) @ 122.88 MHz footnote changed from 2 to 3. - S-LVDS (1.8 V) @ 122.88 MHz footnote changed from 4 to 3. - 3.3 V LVCMOS @ 122.88 MHz footnote changed from 3 to 4. - 2.5 V LVCMOS @ 122.88 MHz footnote changed from 5 to 4. - 1.8 V LVCMOS @ 122.88 MHz footnote changed from 5 to 4. - HSCL Internal Termination (1.8 V, 2.5 V, 3.3 V) @ 122.88 MHz footnote changed from 4 to 5. - CML (1.8 V, 2.5 V, 3.3 V) @ 122.88 MHz footnote changed from 4 to 3. - Total power dissipation parameter, following test conditions - Si5512 changed footnote from 2 to 1. - Si5512 Low-Power Mode changed footnote from 3 to 2.

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Revision	Date	Description

A	November, 2023	- Updated table notes to match Si5518.
		  - 1. Typical test configuration: The following frequencies on 10 LVDS outputs: 2–491.52 MHz (Q), 1–122.88 MHz (Q), 2–1.92 MHz (Q), 1–100 MHz (NA), 1–50 MHz (NA), 2–156.25 MHz (NB), 1–125 MHz (NB). Excludes power dissipated in termination resistors. VDDIN = 1.8 V, VDDO = 3.3 V.
		  - 2. Typical test configuration: Same as Note 1, except all supplies set to 1.8 V for Low-Power Mode. Output formats changed to S-LVDS format.
		  - 3. Differential outputs terminated into an ac-coupled differential 100Ω load
		  - 4. LVCMOS outputs measured into a 5-inch, 50 Ω PCB trace with 5 pF load.
		  - 5. No external termination; amplitude 800 mVpp_se.
		• Table 9. Input Specifications.
		- Differential (XO/VCXO Applied to REF_IN).
		  - Voltage Swing parameter.
		    - Changed footnote from 3 to 2.
		  - Slew Rate parameter.
		    - Changed footnotes from 2,3,4 to 1,2,3.
		- Differential (INx/INxb).
		  - Slew Rate parameter.
		    - Changed footnote from 4 to 3.
		- Changed footnote from 3 to 2.
		  - Slew Rate parameter.
		    - Changed footnote from 4,6 to 3,5.
		• Table 13. Differential Clock Output Specifications.
		- Parameter OUT-OUTb Skew, Symbol TSK_OUT.
		  - Clarified that this parameter is skew between positive and negative output pins.
		  - Expanded Test Conditions portion of table, which allowed some specs to be tightened without changing the overall spec Min/Max.
		- Removed HCSL line items from the following Table 13 Parameter sections and added new HCSL Output Table 14.
		  - Parameter Output Voltage Swing5, Symbol VOUT.
		  - Parameter Common Mode Voltage, Symbol VCM.
		  - Parameter Differential Output Impedance, Symbol Z_0.
		- Expanded table for Parameter Rise and Fall Times (20% to 80%)
		  - Added Parameter Rise and Fall Times (20% to 80%) OUT0 - 11, Symbol t_r/t_f
		    - Removed HCSL line items from the following Table 13 Parameter sections and added new HCSL Output Table 14.
		    - Added Parameter Rise and Fall Times (20% to 80%) OUT10 to 11, Symbol t_r/t_f.
		    - Outputs 10 and 11 have programmable CMOS Slew Rate so spec tables reflect the Typ and Max for those output types.
		- Power Supply Noise Rejection
		  - Changed note from note 8 to note 7
		- Output-to-Output Crosstalk
		  - Changed note from note 9 to note 8
		- Input-to-Output Crosstalk
		  - Changed note from note 10 to note 9
		- Note 6
		  - Removed Note 6
		    - Removed HCSL line items from Table 13 and added new Table 14.
		    - Renumbered remaining notes.
		• Table 14. HCSL Clock Output Specifcations.
		- Added new Table 14 for HCSL Clock Output Specifications and removed HCSL line items from Table 13.
		  - Separating HCSL outputs into its own table allows the output specifications to be more accurately defined.
		  - Output voltage swing
		    - Maximum specification changed to 960 x SF for:
		HCSL Standard, 800 mVpp_se for both internal termination and external termination, and
		HCSL Fast, 800 mVpp_se external termination.

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<table>
<tr><th>Revision</th><th>Date</th><th>Description</th></tr>
<tr><td>A</td><td>November, 2023</td><td>
• Table 15. LVCMOS Clock Output Specifications.
- Added Note 6 to Parameter Rise and Fall Time (20% to 80%)
- Output frequency parameter.
- Test condition NB Divider changed footnote from 3 to 2.
- Test Condition Output Voltage Low changed footnote from 4 to 3.
- Added new Note 6 to the Notes section to cover SRL outputs.
• Table 17. Performance Characteristics.
- Phase noise performance parameter
- Symbol PN_491.52M_XO_Q_Div
- Changed footnote from 11 to 10.
- Added statement to Note 6 to clarify:
- “after the output phase has achieved a steady state value.”
- Updated Note 10 to clarify based on new ClockBuilder Pro Spur Analysis tool, which helps customers analyze added jitter and spurs due to cross talk.
• Table 19. Si5512 72 QFN Pin Descriptions.
- Pin Name: RSTb, Pin: 20, Pin Type: I
- Added additional text on RSTb operation incorporating information found in other application notes, Reference Manuals and other Si5512 support documents.
• Pin Name XV Pin 62 and input clock Pins 65 through 72.
- Referenced “AN1293: Si55xx Schematic Design and Board Layout Guidelines” instead of Si55xx Reference Manual.
• Table 22. Top Marking Explanation.
- Line: 2, Characters: Rxxxxx-GM.
- Fixed typo on temperature range from –40 to +85 °C to –40 to +95 °C.
</td></tr>
<tr><td>1.0</td><td>July, 2022</td><td>Production release.</td></tr>
</table>

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DATA SHEET

Si5518 NetSync™ Low-Phase-Noise Jitter-Attenuating Clock for 5G/eCPRI/SyncE/IEEE 1588

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The Si5518 utilizes fifth-generation DSPLL™ and Multi-Synth™ technologies and integrates the functions of a low phase noise 5G/eCPRI wireless jitter attenuator supporting JESD204B/C with a SyncE/IEEE 1588 PTP network synchronizer clock into a single IC device.

The Si5518 may also be combined with optional Accu-Time™ IEEE 1588 software offering a complete IEEE 1588v2 solution for phase and frequency synchronization. AccuTime 1588 software consists of a unique servo algorithm paired with a protocol stack that runs on the host processor.

The RFPLL generates high-performance, ultra-low phase noise CPRI clocks for wireless remote radio heads (RRH). Each of the 18 clock outputs are configurable in any combination of DCLK, SYSREF, or other system clocks. The DSPLLs are fully featured network synchronization phase-locked-loops with adjustable DCO for IEEE 1588 Ethernet fronthaul synchronization.

Applications

- LTE-A and 5G Remote Radio Units (RRU)
- JESD204B/C clock generation
- IEEE1588 slave clocks (T-TSC), Telecom Boundary Clocks (T-BC)
- IEEE1588 Assisted Partial Timing support clocks (T-BC-A, T-TSC-A), Partial Timing Support (T-BC-P, T-TSC-P)
- IEEE 1588 Grandmaster clocks (T-GM)
- Remote Access Networks (RAN), picocells, small cells
- Remote Radio Heads (RRH), wireless repeaters, mobile fronthaul and backhaul

Key Points

- Utilizes fifth-generation DSPLL™ and MultiSynth™ technologies
- Ultra high-performance clock generation for LTE-A and 5G RRUs with IEEE 1588/SyncE
- Optional AccuTime™ IEEE 1588 software
- Integer output frequencies up to 3.2 GHz
- Fractional output frequencies up to 650 MHz
- JESD204B/C clock generation (DCLK/SYSREF) with synchronization across multiple devices
- Programmable delay at each output
- Ultra-low jitter: 47 fs RMS typical
- Phase Noise:
  - Noise floor –164 dBc/Hz at 491.52 MHz
  - –145 dBc/Hz at 800 kHz offset for a 491.52 MHz carrier frequency
- Spurs < –95 dBc at 122.88 MHz
- Supports IEEE1588 with DCO adjustable at 1 ppt resolution
- Locks to 1PPS and PP2S
- Full suite of status monitors
- Supports ITU-T G.8273.2 (T-TSC, T-BC), ITU-T G.8273.4 (T-BC-P, T-BC-A, T-TSC-P, T-TSC-A), G.8262 (EEC Options 1 and 2), G.8262.1 (eEEC), G.8261 (TC12-17), and PRTC (T-GM)
- 72 QFN 10 x 10 mm, 6 inputs, 18 outputs
- AccuTime™ IEEE 1588 Software
  - Field tested and proven with compliance reports available
  - Demo platform support
  - O-RAN compatible
  - IEEE 1588 servo loop and protocol stack software runs on host processor

Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to *Skyworks Definition of Green™*, document number SQ04–0074.

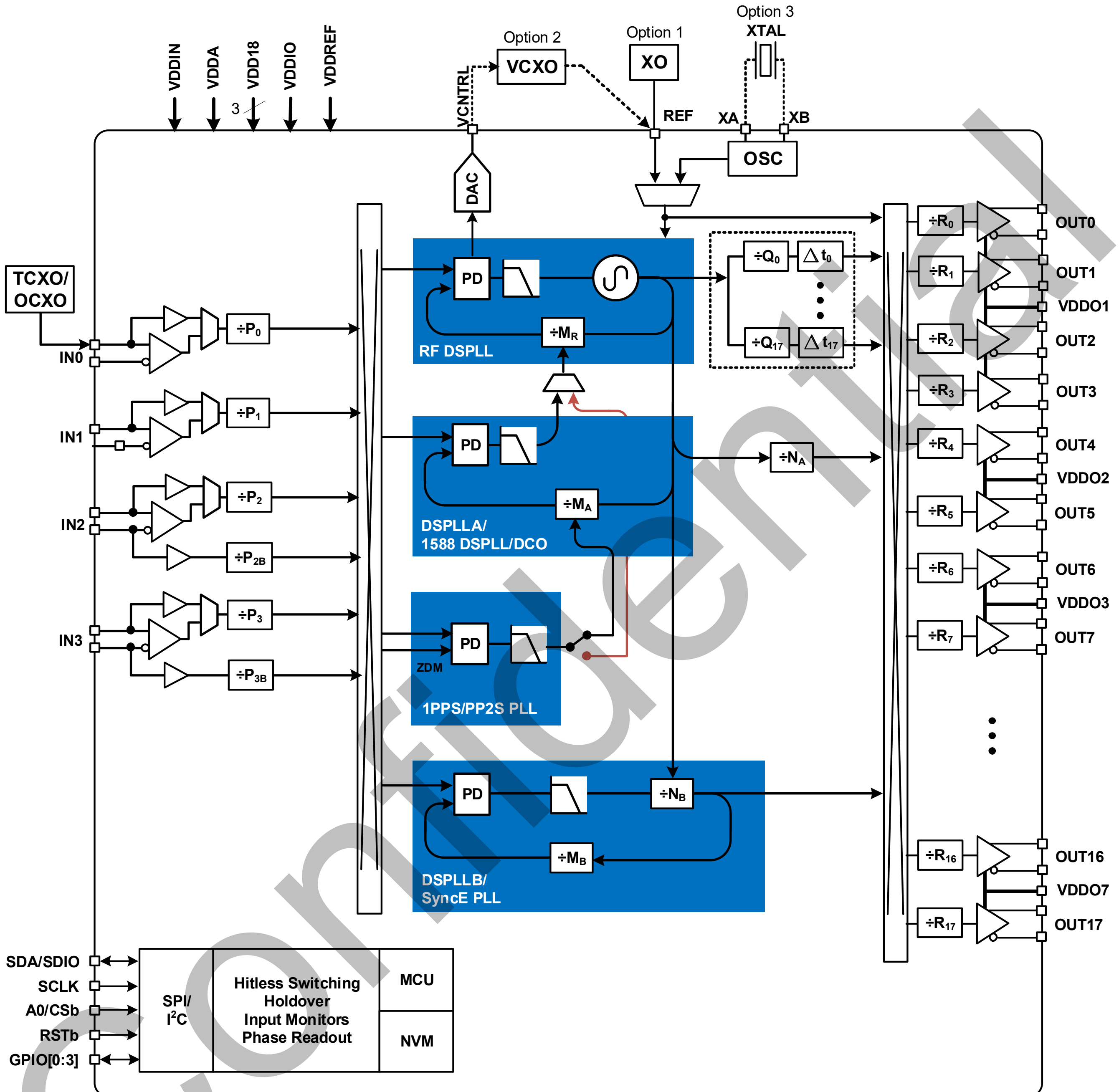

Figure 1. Si5518 Block Diagram

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1. Feature List

- RFPLL (RF DSPLL)
  - Supports JESD204B/C Subclass 0, 1, and 2 Clocking
  - Ultra-low Phase Noise (example at 491.52 MHz carrier):
    - –164 dBc/Hz noise floor
    - –145 dBc/Hz at 800 kHz offset
  - Ultra-low jitter performance:
    - <50 fs typ XO (12 kHz–20 MHz at 491.52 MHz)
    - <45 fs typ VCXO (12 kHz–20 MHz at 491.52 MHz)
  - Selectable jitter attenuation bandwidth: 10 Hz to 400 Hz, 10 Hz to 400 Hz Dual Reference JA
- DSPLL A, DSPLL B
  - Independent network synchronization DSPLLs
  - Supports ITU-T G.8273.2 (T-TSC, T-BC), ITU-T G.8273.4 (T-BC-P, T-BC-A, T-TSC-P, T-TSC-A), and PRTC (T-GM)
  - Programmable loop bandwidth: 1 mHz to 4 kHz
  - Automatic Free-Run, Holdover, and Locked modes
  - Hitless input clock switching: automatic or manual with < 150 ps phase transient
- PPSPLL
  - Instant lock for 1PPS/PP2S
  - Programmable loop bandwidth 1 mHz to 25 mHz
  - Programmable phase slope limiting (PSL) and phase pull-in rate (PPI)
- 18 Programmable Clock Outputs:
  - JESD204B/C DCLK or SYSREF. Up to nine DCLK/SYSREF pairs
  - Integer Q dividers: PP2S/1PPS to 3.2 GHz
  - JESD204B/C SYSREF pulser mode
  - Multisynth Fractional Dividers: PP2S/1PPS to 650 MHz
  - Output-to-Output Static Delay: ±10 ns
  - Output-output skew: ±50 ps
  - LVDS, S-LVDS, AC coupled LVPECL, LVCMOS, Slew Rate Limited (SRL) LVCMOS, HCSL, CML
- Utilizes fifth-generation DSPLL™ and MultiSynth™ technologies
- Zero Delay Mode for all PLLs
- 4/6 clock inputs:
  - Differential: 8 kHz to 1 GHz
  - CMOS: 1 PPS, PP2S, 8 kHz to 250 MHz
- Status monitoring (LOS, OOF, PHMON, FLOL and PLOL)
- Automatically generates free-running clocks at power up
- Automatically locks to a valid clock input
- Automatic holdover mode
- Core voltage: 3.3 V, 1.8 V
- Output driver supply voltages (VDDO): 3.3 V, 2.5 V, 1.8 V
- Serial Interface: I2C or SPI (3 or 4-wire)
- ClockBuilder Pro™ software tool simplifies device configuration
- Package: 72-Lead QFN, 10x10 mm
- Extended temperature range:
  - –40 to +95 °C ambient and –40 to +105 °C board
- Pb-free, RoHS compliant

Note: Specifications are for reference only. See "4. Electrical Specifications" on page 32 for performance.

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2. Ordering Guide

Table 1. Si5518 Ordering Guide

Ordering Part Number (OPN) [1, 2, 3]	Number of DSPLLs	Number of Outputs	Serial Interface	AccuTime™ IEEE 1588 Software Support [4]	Package	Temperature Range
Si5518A-Bxxxxx-GM	1-RFPLL, PPSPLL, 2-DSPLL	18	SPI 4-wire or 3-wire	No	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient [5] –40 to 105 °C Board
Si5518B-Bxxxxx-GM	1-RFPLL, PPSPLL, 2-DSPLL	18	SPI 4-wire only	Yes	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient [5] –40 to 105 °C Board
Si5518C-Bxxxxx-GM	1-RFPLL, PPSPLL, 2-DSPLL	18	I^2C	No	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient [5] –40 to 105 °C Board
Si5518D-Bxxxxx-GM	1-RFPLL, PPSPLL, 2-DSPLL	18	SPI 4-wire only	Yes	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient [5] –40 to 105 °C Board
Si5518E-Bxxxxx-GM[6]	1-RFPLL, PPSPLL, 2-DSPLL	18	SPI 4-wire only	Yes	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient [5] –40 to 105 °C Board
Si5518F-Bxxxxx-GM [6]	1-RFPLL, PPSPLL, 2-DSPLL	18	SPI 4-wire only	Yes	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient [5] –40 to 105 °C Board
Si5518G-Bxxxxx-GM [6]	1-RFPLL, PPSPLL, 2-DSPLL	18	SPI 4-wire only	Yes	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient [5] –40 to 105 °C Board
Si5518H-Bxxxxx-GM [6]	1-RFPLL, PPSPLL, 2-DSPLL	18	SPI 4-wire only	Yes	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient [5] –40 to 105 °C Board
Si5518I-Bxxxxx-GM [6]	1-RFPLL, PPSPLL, 2-DSPLL	18	SPI 4-wire only	Yes	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient [5] –40 to 105 °C Board
Si5518P-Bxxxxx-GM [6]	1-RFPLL, PPSPLL, 2-DSPLL	18	SPI 4-wire or 3-wire	No	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient [5] –40 to 105 °C Board
Si5518Q-Bxxxxx-GM[6]	1-RFPLL, PPSPLL, 2-DSPLL	18	SPI 4-wire only	Yes	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient [5] –40 to 105 °C Board
Si5518R-Bxxxxx-GM [6]	1-RFPLL, PPSPLL, 2-DSPLL	18	I^2C	No	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient [5] –40 to 105 °C Board
Si55xx-A-EVB	1-RFPLL, PPSPLL, 2-DSPLL	18	—	—	Evaluation Board	—
Si5518-A-FMC-EVB [7]	—	—	—	Yes	FPGA Mezzanine Card (FMC)	—

1. Add an "R" at the end of the OPN to denote tape and reel ordering options.
2. Custom, factory preprogrammed devices are available as well as unconfigured base devices. See the figure below for 5-digit numerical sequence nomenclature.
3. Revision B will be the device qualified for mass production and loose samples.
4. AccuTime IEEE 1588 software is only supported on certain part grades. Use this table to determine which grades support AccuTime.
5. Ambient temperature of 95 °C may not be possible with all configurations. This is dependent on device configuration. Tj cannot exceed a max of 125 °C.
6. Grades D, E, F, G, H, I, P, Q, and R are reserved for special factory use and not for general customer use.
7. The Si5518-A-FMC ships with 10GBASE-SR SFP+ transceivers, optical cable along with the required software on an SD card. FMC requires a customer-provided AMD ZCU102, ZCU111 or ZCU216 FPGA eval board. FMC is only for AccuTime evaluation.

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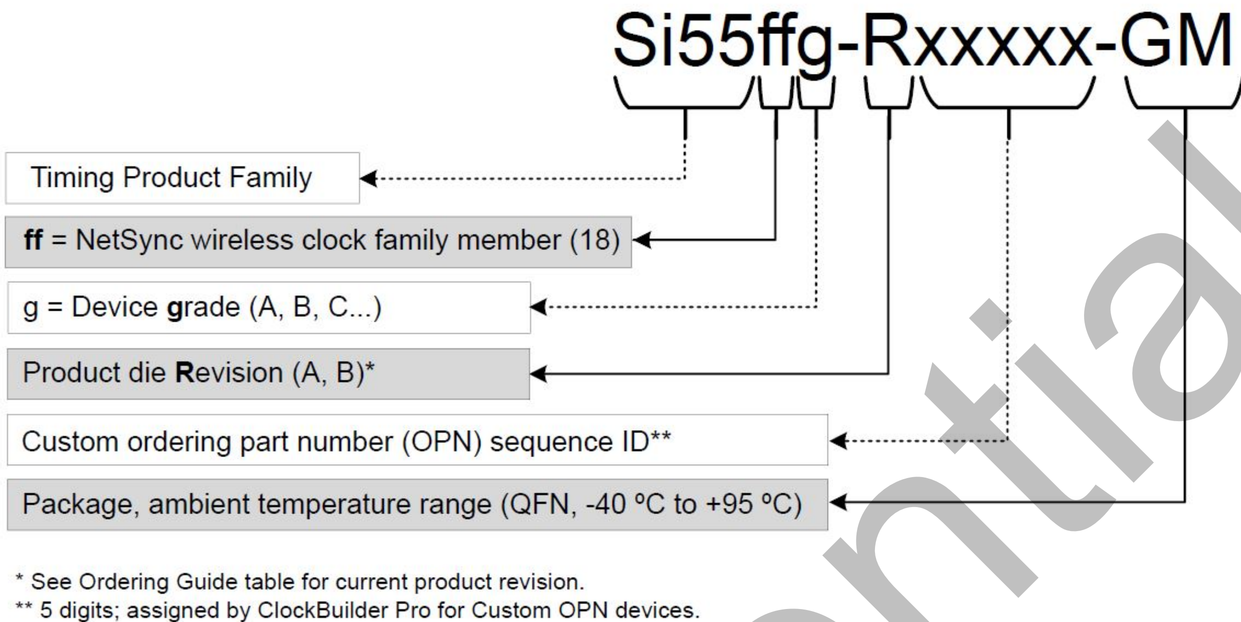

Figure 2. Si5518 Ordering Guide Diagram

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3. Functional Description

The Si5518 combines a high-performance JESD204B/C compatible RF clock jitter attenuator and two 5th generation DSPLLs supporting SyncE/IEEE1588 network synchronization. This provides a highly-integrated synchronization solution for wireless applications where both IEEE 1588 and JESD204B/C clock generation are needed. Only a few external components are required for a complete synchronization function. The RFPLL and DSPLLs can operate from an external VCXO, XO or fixed frequency crystal (XTAL). Both the DSPLLs and RFPLL support Locked, Free-Run, and Holdover modes of operation with an optional DCO mode for IEEE 1588 applications. An optional external TCXO or OCXO provides frequency accuracy and stability for Free-Run and Holdover modes. This is referred to as dual reference mode. The RFPLL is locked to the OCXO/TCXO but is also modulated by the input to DSPLLA. See "3.10. External Reference Clocks (XA/XB, REF_IN)" on page 16 for more details. There are 4 differential/single-ended inputs available to synchronize any of the phase-locked loops. Two of the inputs (IN2, IN3) can be configured as dual single-ended inputs in applications where more than 4 inputs are required. Input selection can be manual or automatically controlled using an internal state machine. Any of the 18 output clocks (OUT0 to OUT17) can be sourced from any of the PLLs using a flexible crosspoint connection.

There is an additional PPSPLL that can be used for synchronization to a 1 PPS/PP2S input. If the application uses AccuTime SW, then the 1PPS from GNSS should instead be timestamped by the host controller in order to have the GNSS assist the PTP servo for smooth transitions when the GNSS is lost and again recovered.

Skyworks offers a comprehensive IEEE 1588 solution for applications in a centralized "pizza box" architecture. It consists of three components: An IEEE 1588 protocol stack, a packet synchronizer servo algorithm (or "servo"), and the Si5518 network synchronizer clock. The IEEE 1588 stack receives Ethernet packets from the host processor MAC, processes IEEE 1588 packets, and sends time stamp data to the IEEE 1588 servo algorithm implemented on the host. The servo statistically processes the time stamps and adjusts a 1588 system clock that runs the Time of Day (ToD) counter in the host.

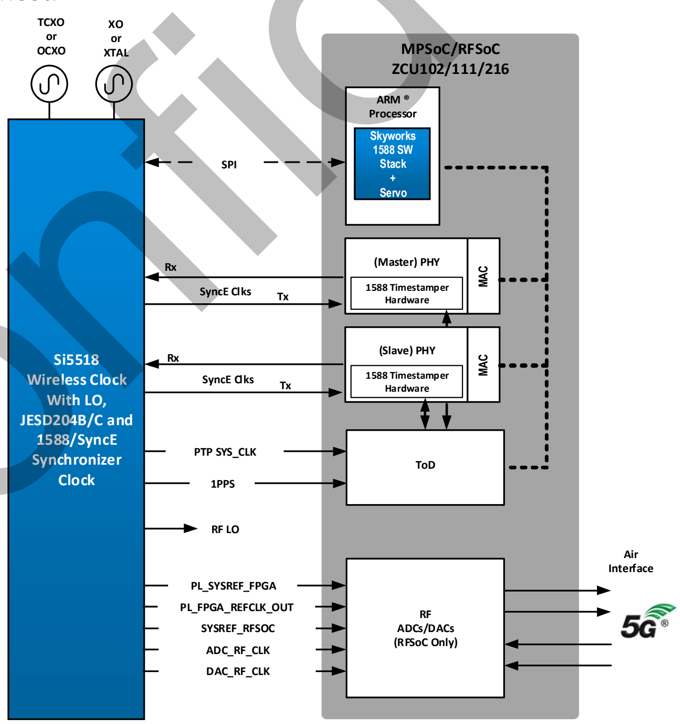

Figure A – Centralized "Pizza Box" Architecture

Figure 3. Si5518 IEEE1588 Demonstration Platform

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3.1. Frequency Configuration

The frequency configuration of the DSPLL is programmable through the serial interface and can also be stored in non-volatile memory. The combination of input dividers (P), fractional frequency multiplication (M), integer output division (Q), fractional output division (N), and integer output division (R) allows the generation of virtually any output frequency on any of the outputs. All divider values for a specific frequency plan are easily determined using the ClockBuilder Pro utility.

3.2. DSPLL Loop Bandwidth, Initial Lock, and Fast Lock Settings

The DSPLL loop bandwidth determines the amount of input clock jitter attenuation. Each DSPLL has a configurable loop bandwidth. The DSPLL will always remain stable with low peaking regardless of the loop bandwidth selection.

Each of the DSPLL's, and the PPSPLL, have configurable loop bandwidths. There are three configurations, each has a separate setting for the loop bandwidth:

- **Initial Lock Bandwidth**: The PLL uses this bandwidth when it exits the free-run mode and attempts to lock to a new input clock.
- **Loop Bandwidth**: This sets the bandwidth of the PLL once lock to an input is achieved.
- **Fastlock Bandwidth**: This sets the bandwidth of the PLL when exiting from holdover.
  - Selecting a low DSPLL loop bandwidth will generally lengthen the lock acquisition time. The Fastlock feature allows setting a temporary Fastlock Loop Bandwidth that is used during the lock acquisition process. The DSPLL will revert to its normal loop bandwidth once lock acquisition has completed.

See the Si5518/12/10/08 Reference Manual and ClockBuilder Pro for more information, recommendations, and limits for setting PLL loop bandwidths for different configurations.

3.3. Inputs

There are four differential inputs which can also be configured as single-ended CMOS inputs. Both IN0 and IN1 can support a single CMOS input, while IN2 and IN3 can be configured as dual CMOS inputs. This allows support for up to 6 CMOS inputs, or any combination of differential and CMOS inputs.

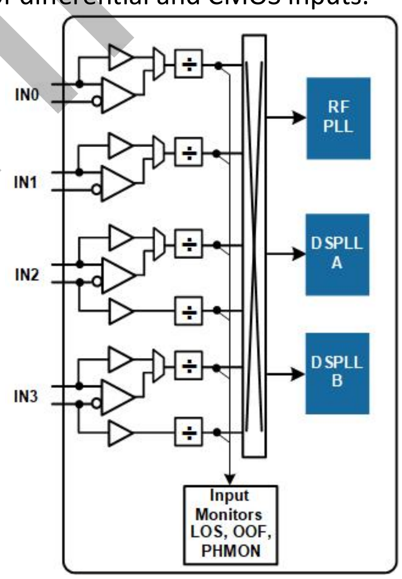

Figure 4. Input Structure

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3.3.1. Input Terminations

Refer to AN1293: Si55xx Schematic Design and Layout Guidelines or Si5518/12/10/08 Reference Manual for guidance on input terminations.

3.3.2. Input Selection

Input selection for any of the PLLs can be controlled manually through pin control, API command, CLI command, or automatically using an internal state machine.

3.3.2.1. Input Divider

The device utilizes both fractional and integer input (P) dividers to lock to any frequency input clock. The ClockBuilder Pro software will choose the optimal divide values based on the user-defined frequency plan. Each input divider (P0, P1, P2, P2b, P3, and P3b) can be configured independently of the others.

3.3.2.2. Manual Input Selection

In manual mode, the input selection is made by defining a GPIO pin as an input select pin and changing the input pin voltage level, or by writing an API or CLI command. Any of the inputs are available to any of the PLLs through a crosspoint input selection switch. If there is no clock signal on the selected input, or if the input is not valid due to LOS/OOF/PHMON input alarms, the PLL will automatically enter Free-Run/Holdover Mode. This applies to both the DSPLLs, RFPLL, and the PPSPLL.

3.3.2.3. Automatic Input Selection

When configured in this mode, each of the PLLs automatically selects a valid input that has the highest configured priority. The priority scheme is independently configurable for each PLL and supports revertive or non-revertive selection. All inputs are continuously monitored for loss of signal (LOS), invalid frequency range (OOF), and phase (PHMON). Only valid inputs that have no LOS, OOF or phase monitor (PHMON) alarms can be selected for synchronization by the automatic state machine. The PLL(s) will enter Free-Run or Holdover Mode if there are no valid inputs available.

3.3.3. Unused Inputs

Unused inputs should be configured as “Unused (Powered Down)”, and the pins may be left unconnected or ac-coupled to ground. See AN1293: Si55xx Schematic Design and Layout Guidelines or Si5518/12/10/08 Reference Manual for recommendations on how to minimize system noise on any CMOS input and/or any differential input configured as “Enabled” but not actively being driven by a clock.

3.3.4. Phase Readout (PHRD)

The Phase Readout Device API can be used to read and measure the phase between multiple input clocks to the Si5518. Unused inputs that are not assigned to a DSPLL can also be configured as phase readout (PHRD) or phase readout feedback (PHRD_FB) inputs. These inputs can be used to measure the phase of an output of the Si5518 to the input(s) of known phase. PHRD and PHRD_FB inputs use the same alarms, such as LOS/OOF/PHMON, as the other clock inputs, but they are not assigned to a DSPLL.

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3.4. Input Clock Switching

Clock inputs applied to the Si5518 can be either from the same source (0 ppm, same nominal frequency) or different sources (non-0 ppm, different nominal frequencies). The Si5518 automatically determines the optimal switching mode depending on the nominal frequency difference between the clocks at the time of the switch. When switching between 0 ppm inputs, the Si5518 performs either a hitless switch with phase buildout (PBO) or a phase pull-in (PPI) switch depending on the user selection in ClockBuilder Pro. When the input clocks have a non-0 ppm offset, the Si5518 performs a frequency-ramped input switch. Automatic input clock switching is not available for PPSPLL.

Refer to AN1293: Si55xx Schematic Design and Layout Guidelines or Si5518/12/10/08 Reference Manual for additional guidance on input clock switching modes. All input clock switches are glitchless, meaning there will be no runt pulses generated at the output during the transition.

3.4.1. Hitless Input Switching for 0 ppm Clocks—Phase Buildout (PBO)

Applications like SyncE/eCPRI require that transients are kept to a minimum when switching between input clocks. Hitless switching with phase buildout (PBO) is a feature that prevents a transient from propagating to the output when switching between two clock inputs that have a fixed phase relationship. A hitless switch can only occur when the two input frequencies are frequency locked, meaning that the nominal frequencies are the same (0 ppm). Due to the nature of hitless switching, the input-to-output delay of the PLL is not preserved. The DSPLL simply absorbs the phase difference between the two input clocks during an input switch. The phase buildout feature supports clock frequencies down to a minimum input frequency of 8 kHz.

3.4.2. Phase Pull-In (PPI) Input Switching for 0 ppm Clocks

In some applications, the output phase must track the input phase with minimal delay. This is particularly common in applications which require synchronization to an external 1PPS such as a GNSS receiver or traditional CPRI fronthaul clocking. When the application requires the input-to-output delay to be preserved after clock switching, the phase pull-in clock switching mode should be selected. In this mode, the output phase will be pulled in at a user-programmable ramp rate referred to as the PPI slope (ns/s). With phase pull-in switching, the output phase always aligns with the newly selected input. PPI is always enabled for zero-delay mode and PPSPLL applications.

3.4.3. Ramped Input Switching for Non-0 ppm Clocks

The ramped switching feature allows the DSPLLs to switch between two input clock frequencies that have a non-0 ppm offset without an abrupt frequency transient at the output. When the two input clock frequencies are not the same nominal frequency, the DSPLL will pull in the frequency difference between inputs at the ramp rate that is programmable in ClockBuilder Pro from ppb/s to ppm/s. The loss-of-lock (LOL) and the LOOP_FILTER_RAMP_IN_PROGRESS indicators (accessible through the Device API) will assert while the DSPLL is ramping to the new clock frequency.

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3.5. Outputs

The Si5518 supports 18 differential output drivers configurable as AC Coupled LVPECL, LVDS, S-LVDS, CML, HCSL, LVCMOS, or SRL LVCMOS. When in LVCMOS mode, the differential pair becomes two single-ended outputs for a maximum of 36 possible outputs. Two of the output drivers (OUT16 and OUT17) have slew rate control when in LVCMOS mode. This allows limiting the rise time of the output signal to reduce the possibility of crosstalk to adjacent output drivers. The outputs have power supply pins (VDDOx) for output driver groups of 4-2-2-2-2-4-2, which can be individually powered by 3.3, 2.5, or 1.8 V. The LVCMOS output voltage is set by the VDDOx pin. Refer to Table 20, “Pin Descriptions,” on page 55.

3.5.1. Output Crosspoint

A crosspoint allows any of the output drivers to connect with any of the PLLs. A digital output delay adjustment is possible on each of the Q divider outputs for JESD204B/C applications. The static delay adjustments are programmable and may be stored in NVM so that the desired output configuration is ready at power up.

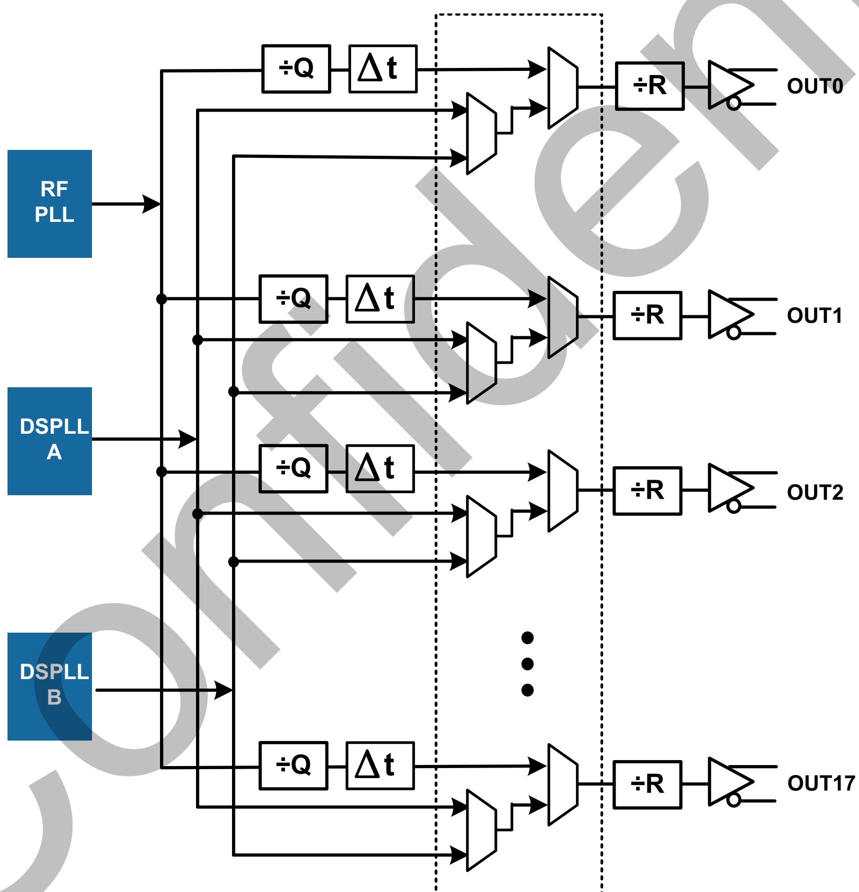

Figure 5. Output Structure

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3.5.2. Differential and LVCMOS Output Terminations

Refer to AN1293: Si55xx Schematic Design and Board Layout Guidelines and Si5518/12/10/08 Reference Manual for guidance on output terminations.

3.5.3. Slew Rate Limited (SRL) LVCMOS Outputs

The swing of LVCMOS and SRL LVCMOS outputs is rail-to-rail; so, the swing is determined by the voltage of the corresponding VDDO pin of the LVCMOS or SRL LVCMOS output. Each output driver configured as LVCMOS or SRL LVCMOS has two outputs, OUTx/OUTxb. The polarity of each of the two outputs may be independently configured as a noninverted or inverted output as well as enabled or disabled.

OUT16/16b and OUT17/17b may be configured as SRL LVCMOS outputs, which have a programmable slew rate and generate significantly less crosstalk than conventional LVCMOS outputs. Less crosstalk than conventional CMOS outputs is useful in jitter-critical applications.

SRL LVCMOS output clocks on OUT16/16b and OUT17/17b are intended only for low frequency clock applications. Refer to the Si5518/12/10/08 Reference Manual for the maximum Fout supported for each slew rate selection.

3.5.4. Output Enable/Disable

Each output driver may be enabled/disabled through programmable GPIO pins. There are two output enable groups, OE0 and OE1, which are logically OR'ed together to determine which outputs are enabled at any point in time. ClockBuilder Pro allows the control and selection of the GPIO pin mapping to the outputs.

Outputs may also be enabled/disabled using the device API. If an output is assigned as GPIO controlled, it cannot be controlled via the API. The API controlled output enable allows for more flexibility than the GPIO control as any of the outputs can be individually enabled/disabled via an API command.

The default output enable/disable behavior is a glitchless enable/disable. For clocks to start or stop as soon as possible, accepting runt pulses or glitches, instant output enable/disable can be used.

3.5.5. State of Disabled Output

The disabled state of an output driver may be configured as stop high, stop low, or Hi-Z. CMOS outputs less than 2 MHz can also be configured as Hi-Z with weak pull-up/pull-down.

Differential outputs, when disabled, will maintain the output common-mode voltage even while the output is not toggling. This minimizes disturbances when disabling and enabling clock outputs.

3.5.6. Output Dividers

The device utilizes both integer Q dividers and fractional NA, NB MultiSynth output dividers. The ClockBuilder Pro software chooses the optimal divide values based on the user-defined frequency plan.

A summary of each class of divider is listed below:

1. Output Q Divider: Q0–Q17
   - Integer Only Divide Value
   - Open loop divider taps directly off VCO
2. DSPLL A/B Feedback M Divider: MA, MB
   - Integer or Fractional Divide Value

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3. Output N Divider: NA, NB
   - MultiSynth Divider, Integer or Fractional Divide Value
4. Output Divider: R17-R0
   - Integer Only Divide Value
5. Synchronized Dual Outputs
   - If one N divider is used in a closed loop fashion and the other N divider is used in an open loop fashion, the dividers may be cascaded so that the output of each N-divider is derived from the same input clock source and is capable of having a fractional frequency relationship.

3.5.7. Output Skew Control

Output skew control allows outputs that are derived from the Q dividers to be phase adjusted in steps of 1/fvco or 1/(4*fvco) when the fine adjust is enabled. The exact skew adjustment and step sizes are reported on the Output Skew Control Tab of the ClockBuilder Pro Wizard.

3.5.8. Output Synchronization (OSYNC)

The OSYNC input is used to align the phases of the integer Q divider output clocks to a SYNC input signal from a logic device (ASIC/FPGA) or a data converter. OSYNC can be used to achieve deterministic latency in a JESD204B/C Subclass 2 application. When asserted, the Q divider outputs will stop low glitch-free. When OSYNC is de-asserted, the first transition of all outputs will be aligned to the OSYNC signal within the data sheet delay from OSYNC de-asserted to output reenabled specification. OSYNC must be assigned to GPIO2.

OSYNC can also be used to align the phases of the Q divider output clocks between multiple Si5518 devices to a SYNC input signal. To achieve the chip-to-chip data sheet specification for output skew, the input clock to the Si5518 must be a CPRI frequency (N*1.92 MHz) and integer-related to the Q divider outputs.

OSYNC can also be initiated through an API command instead of a GPIO input; however, the OSYNC de-asserted to output reenabled specification cannot be guaranteed. The API command should not be used for multichip OSYNC.

3.6. RFPLL

The RFPLL controls the central VCO which provides many of the essential functions for the device such as generating ultra-low phase noise JESD204B/C clocks and maintaining free-run accuracy and holdover stability for all PLLs (RFPLL, DSPLLA, DSPLLB, PPSPLL). It operates using one of many external frequency sources. In single reference mode, a simple low-cost fixed frequency crystal (XTAL) provides the phase noise reference and the RFPLL locks to a clock input for jitter attenuation. Options of using a crystal oscillator (XO) or a voltage-controlled crystal oscillator (VCXO) are also available. In dual reference mode, the RFPLL locks to a TCXO or OCXO in addition to the fixed frequency oscillator. Dual reference mode should be used for applications that require low phase noise and highly stable holdover and free-run accuracy output clocks. The benefits and trade-offs of these configurations are covered in the Si5518/12/10/08 Reference Manual and ClockBuilder Pro.

3.6.1. JESD204B/C Clock Generation

The RFPLL generates ultra-low phase noise JESD204B/C clocks for Subclass 0, Subclass 1, and Subclass 2 operation. Any of the 18 clock outputs can be assigned to generate JESD204B/C output clocks.

JESD204B/C Subclass 0 and Subclass 2 support is provided through the OSYNCb input assignable to GPIO2.

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JESD204B/C Subclass 1 support is provided with assignable SYSREF/DCLK timing skew, as well as with a SYSREF pulser that supports JESD204B/C “gapped” periodic outputs.

Static delay is assignable with a step size down to 1/4*VCO period (approximately 20 ps). Exact delay is reported in ClockBuilder Pro.

Each SYSREF output can be configured in continuous mode. SYSREFs in continuous mode may cause crosstalk with adjacent DCLK outputs. If using SYSREF in continuous mode a gap of one unused output is recommended between SYSREF and DCLK.

The SYSREFs can also be configured in pulsed mode. The SYSREF pulser provides 1, 2, 4, 8, 16, or 32 pulses on user request, with the SYSREF held static between requests. SYSREFs in pulsed mode will not couple with other channels since for the majority of operation they are disabled. A gap or unused output between DCLK and SYSREF is not necessary in pulsed mode. Each SYSREF can be independently assigned as Continuous or Pulsed mode with desired number of pulses in ClockBuilder Pro. A common SYSREF pulse request for all pulsed SYSREF outputs can be initiated either by a rising edge on assignable digital input SRCREQ, or by using the JESD_SYSREF_PULSER API via the serial interface.

3.7. DSPLL (DSPLL A, DSPLL B)

In general, both DSPLLs have identical performance and flexibility and can be independently configured and controlled through the serial interface. Each of the DSPLLs support Locked, Free-Run, and Holdover modes of operation with an optional DCO mode for IEEE 1588 applications. The DSPLLs share the stability from the OCXO/TCXO applied to the RFPLL in dual reference mode in order to support free-run and holdover modes.

DSPLL A also has the option of modulating the RFPLL in a dual reference mode to train all clock outputs to the SyncE or IEEE 1588 rate.

3.7.1. DCO Mode

The DCOs in each of the DSPLLs can be frequency controlled in pre-defined steps ranging from <1 ppt to several ppm. This is a useful feature for IEEE 1588 applications. The DCOs can be controlled when its DSPLL is locked to an external SyncE input (Hybrid SyncE + PTP Mode) or when it is in Free-Run/Holdover Mode. The frequency adjustments are controlled through the serial interface by triggering a Device API command or by pin control using frequency increments (FINC) or decrements (FDEC). Both the FINC and FDEC pins are available through the configurable GPIO pins. Each DSPLL can be assigned to the FINC and FDEC pins. A FINC will add the frequency step word to the DSPLL output frequency, while a FDEC will decrement it. Step sizes are configured in ClockBuilder Pro.

3.8. Zero Delay Mode (ZDM)

Zero Delay Mode (ZDM) is a mode of PLL operation in which more accurate input to output phase delay can be achieved by providing an external feedback from one of the clock outputs to one of the clock inputs. ZDM is available on each of the four PLLs (RFPLL, DSPLLA, DSPLLB, PPSPLL) and is required when the PPSPLL is enabled. For more details on implementing ZDM, see AN1293: Si55xx Schematic Design and Board Layout Guidelines and Si5518/12/10/08 Reference Manual.

3.9. PPSPLL

The PPSPLL allows synchronization of the Si5518 to an external 1PPS (1 Hz) or PP2S (0.5 Hz) input clock and is configurable in ClockBuilder Pro. When a valid input clock to DSPLLA is present the PPSPLL modulates DSPLLA. When DSPLLA is unused or in holdover/free-run, the PPSPLL will automatically modulate the RFPLL as well as DSPLLA.

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The PPSPLL uses an external feedback loop to guarantee minimal input-to-output delay between the PPS input and the generated PPS output. IN3b is used as the feedback input. To minimize input to output latency in PPSPLL zero delay mode, OUT0 or other low numbered outputs should be used as the feedback output to reduce the PCB routing distance.

See the Si5518/12/10/08 Reference Manual and ClockBuilder Pro for more information and recommendations regarding the PPSPLL and the features it supports.

The PPSPLL supports the features described in the following subsections.

3.9.1. Instant Lock

When an input clock is first applied to the PPSPLL, the PLL will make a measurement of input frequency to lock the PLL frequency. The PPSPLL will then measure the phase difference between the input clock and the ZDM feedback input and apply an open loop phase adjustment (referred to as a phase jam) to zero out the phase difference at a much faster rate than the low bandwidth of the PPSPLL. See the Si5518/12/10/08 Reference Manual for an in-depth discussion on PPSPLL instant lock and phase transients that may result.

3.9.2. Bandwidth Settings

Three separate loop bandwidths are configurable in ClockBuilder Pro:

- **Initial Lock Bandwidth**: The PPSPLL uses this bandwidth when it exits the free-run mode and attempts to lock to a new input clock.
- **Loop Bandwidth**: This sets the bandwidth of the PPSPLL once lock to an input is achieved.
- **Fastlock Bandwidth**: This sets the bandwidth of the PPSPLL when exiting from holdover.

3.9.3. Auto and Manual Relock

When enabled, this feature allows the PPSPLL to quickly reestablish lock during an input phase step or frequency step by issuing a phase jam to the PPS output. The threshold where auto relock is triggered is definable in Clock-Builder Pro.

An alternative option to auto re-lock is to use the PHASE_READOUT API to monitor the phase offset seen by the PPSPLL. When the offset exceeds a desired threshold, manually trigger a relock/phase jam via the PPS_RELOCK API command. A manual relock may often be preferred over auto relock in order to power down or reset RF equipment relying on PPS synchronization before issuing the relock, which will cause large disturbances to the outputs synchronized to PPS.

3.9.4. Phase Slope Limit

When enabled, this feature limits the rate of phase change of the output clock(s) when a phase transient occurs at the input. The phase slope limit (PSL) is definable in ClockBuilder Pro in units of ns/s.

3.9.5. Phase Pull-in Rate

When enabled, this feature limits the phase pull-in of the PPSPLL output clock(s) during an input clock switch or exit from holdover. The phase pull-in rate (PPI) is definable in ClockBuilder Pro in units of ns/s.

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3.9.6. Holdover History

The PPSPLL automatically enters holdover when its input fails. It uses the average frequency that was collected while locked to an input to prevent any disturbances at the outputs when entering holdover. The length of data collected is configurable in ClockBuilder Pro.

3.9.7. Status Monitoring

The PPSPLL has several status monitors accessible through API commands. These include (but are not limited to):

- Input Status (IN0, IN1, IN2, IN2b, IN3, IN3b)
  - Input Valid
  - Loss of Signal (LOS)
  - Out of Frequency (OOF)
  - Phase Monitor (Phase error, Signal late, Signal early)
- PLL Status
  - Loss of Lock (LOL status accessible through API and GPIO)
  - Out of Phase
  - Out of Frequency
  - In Holdover
  - Phase Slope Limit in Progress
  - Fastlock Bandwidth in Use

Refer to the API documentation and the Si5518/12/10/08 Reference Manual for more detailed information.

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3.10. External Reference Clocks (XA/XB, REF_IN)

The Si5518 operates from either an external crystal oscillator (XO) connected to the REF_IN pins or with an optional fixed-frequency crystal (XTAL) connected to the XA, XB pins. The internal oscillator (OSC) combined with a low cost external XTAL produces an ultra-low jitter reference clock for the PLLs (RFPLL, DSPLLA/B, PPSPLL). When using an external XO, it's important to select one that meets the jitter performance requirements of the end application. Alternatively, the device can operate with an external voltage-controlled crystal oscillator (VCXO). Operating the device with only an XO or XTAL, or with only a VCXO is the single reference mode as shown below.

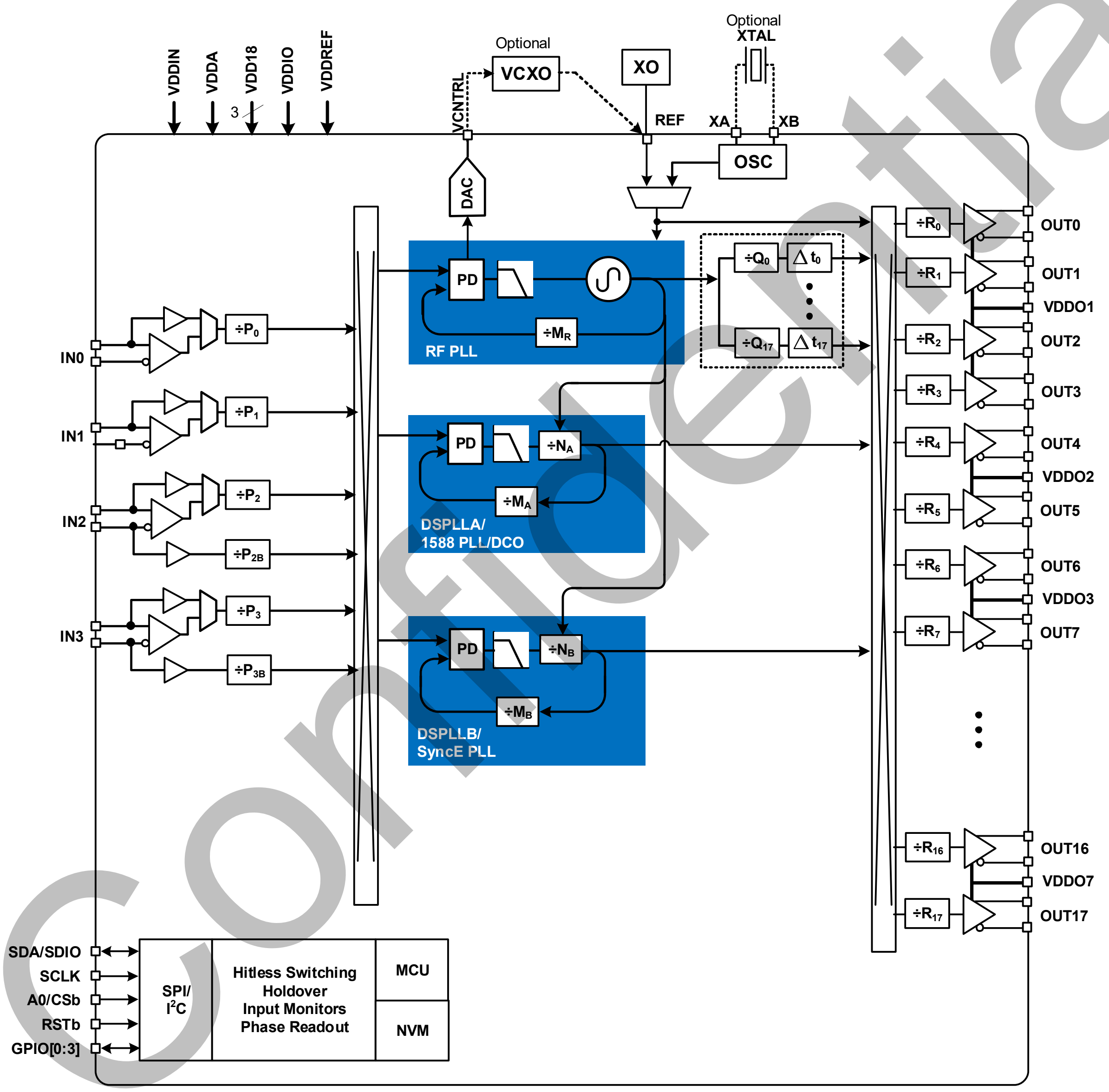

Figure 6. Single Reference Mode

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The Si5518 can also be configured in a dual reference mode where a TCXO or OCXO provides improved output frequency accuracy and stability during Free-Run Mode and greater frequency stability in Holdover Mode. In this case, the RFPLL locks to a TCXO or OCXO that is applied to one of the inputs. The low phase noise reference XO/VCXO or XTAL is connected to REF_IN or XA/XB as described above. This configuration is shown below.

Use ClockBuilder Pro to configure the device in either single reference mode or dual reference mode.

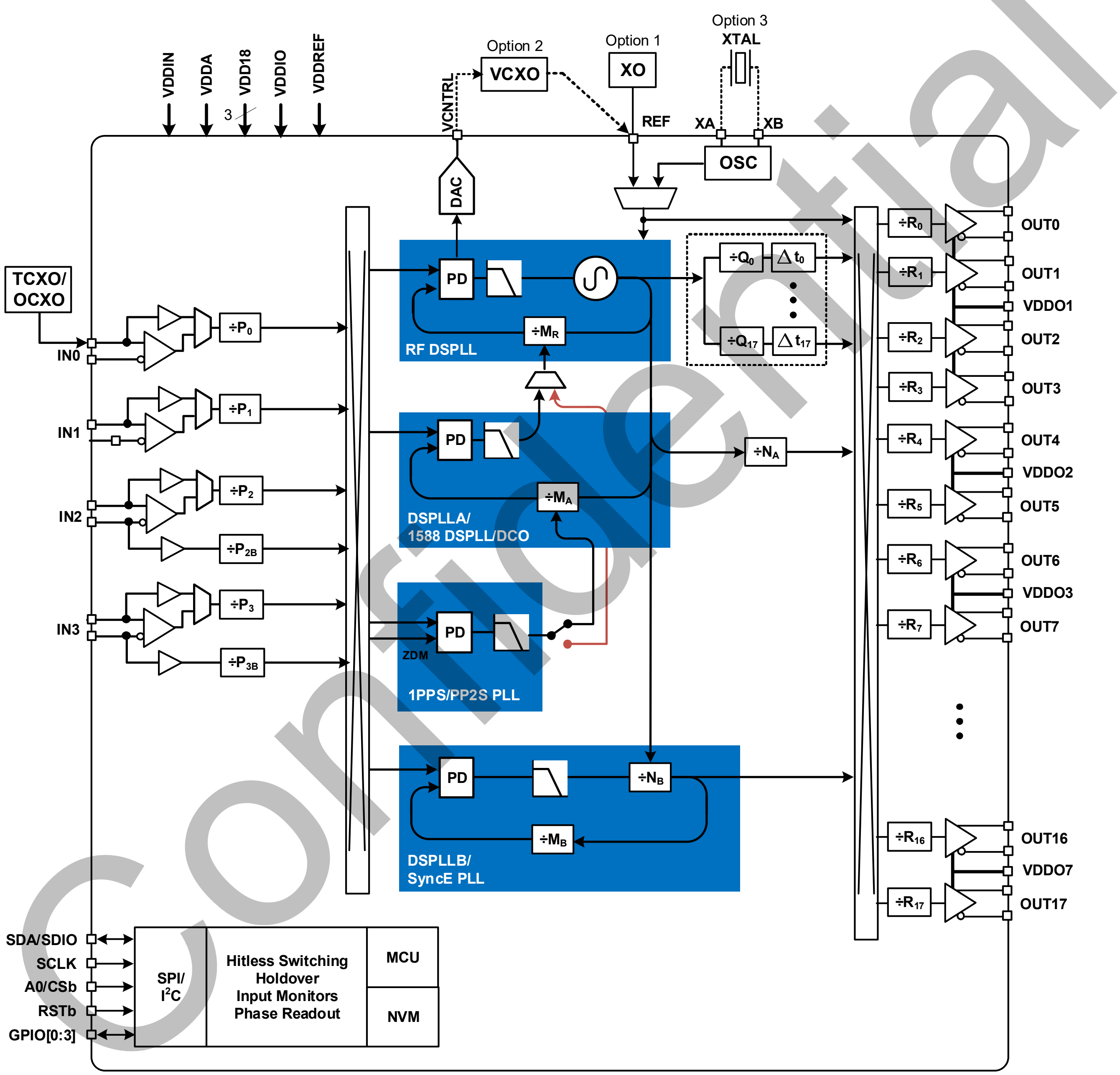

Figure 7. Dual Reference Mode

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3.10.1. XA, XB Inputs

The XA/XB inputs are used to provide a fixed frequency reference for the PLLs (RFPLL, DSPLLA/B, PPSPLL). The device includes internal XTAL loading capacitors which eliminate the need for external capacitors and also has the benefit of reduced noise coupling from external sources. A crystal in the range of 48 to 54 MHz is recommended for best jitter performance.

3.10.2. REF_IN Input

An alternative to using an external XTAL is to connect a crystal oscillator (XO) directly to the REF_IN Input. Another option is using an external voltage controlled crystal oscillator (VCXO). In VCXO mode, the RFPLL produces an analog control voltage which adjusts the VCXO's output frequency. This mode is useful when generating specific integer related output frequencies such as in wireless applications (e.g., 4G/LTE, 5G). The REF_IN inputs accommodate both single-ended CMOS as well as differential XOs/VCXOs. See the Si55xx, Si540x, and Si536x Recommended XTAL, XO, VCXO, TCXO, and OCXO Reference Manual for more information.

3.10.3. VCXO Buffer Output

When the REF_IN input is a VCXO, there is a VCXO buffer output available that can be used to achieve the lowest midband phase noise (10 kHz to 1 MHz). This is often critical for high-end applications, such as mmWave. The VCXO buffer output tracks the phase and frequency of the input clock just as any of the other Si5518 outputs. However, since the VCO and Q dividers are bypassed, the buffer output frequency must equal the frequency of the VCXO. All of the remaining outputs and DSPLLs are still available when using buffer output. The buffer output can be assigned to any of the outputs via the output crosspoint mux. A buffer output is not available when using an XO or XTAL.

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3.11. GPIO Pins (General Purpose Input or Output)

There are four GPIO pins with programmable functions. They can be assigned as either an input or an output from one of the functions shown in the table below. OUT6/11 can be repurposed as GPIs when they are not being used as clock outputs. The GPIs are programmable as either active-high or active-low via ClockBuilder Pro. Active low GPIs are indicated by adding a "b" at the end of the function name, e.g., "OEb", as displayed in ClockBuilder Pro. All GPI pins have a weak pull-up (PU) or pull-down (PD) resistor to set a default state when not externally driven. The default state of the GPI is always deasserted except for OEx, which is, by default, asserted to enable the outputs. The internal resistance of the PU/PD resistor is 20 kΩ typical.

GPIO selectable status outputs (GPOs) are push-pull and do not require any external pull-up or pull-down resistors.

Table 2. GPIO Pin Descriptions

Function	Description
GPIO Selectable Control Inputs (GPI)	
FINC	DCO Frequency Increment
FDEC	DCO Frequency Decrement
PLLx_FORCE_HO	Force holdover for RFPLL, or DSPLL A, or DSPLL B.
PLLx_INSEL[0-2]	Input select pins for RFPLL, or DSPLL A, or DSPLL B. There are three bits to select from one of six inputs.
IN[0:5]_FAIL	Force input invalid. A low on this pin indicates to the automatic switching state machine that the associated input is not valid for selection. This is useful in applications that use their own input monitoring.
OE0–OE1	Output enable for specific outputs or group of outputs as defined by the grouping assigned in ClockBuilder Pro.
SRCREQ	JESD204B/C SYSREF pulse request.
OSYNC	Synchronizes all or a subset of output dividers identified as PPS or SYSCLK in ClockBuilder Pro. **Assignable to GPIO2 only.
GPIO Selectable Status Outputs (GPO)	
PLLx_LOL	Loss of lock for RFPLL, DSPLLA, DSPLLB, and PPSPLL.
PLLx_HO	This pin indicates when RFPLL, DSPLL A, DSPLL B has entered the holdover state.
INx_LOS	Loss of Signal status indicator for INx.
INx_OOF	Out of Frequency status indicator for INx.
REF_OOF	Out of Frequency status indicator of the reference.
REF_LOS	Loss of signal at XA/XB or REF pins.
INTR	Interrupt pin for the device. Programmable Boolean combination of PLLx_LOL, INx_LOS, INx_OOF, PLLx_HO, REF_LOS, REF_OOF.
Primary Serial Interface (I2C/SPI)	
A1/SDO	A1/SDO of Primary SPI Port. **Assignable to GPIO3 only.
A0/CSb	A0/CSb of Primary SPI Port.
SDA/SDIO	SDA/SDIO of Primary SPI Port.
SCLK	SCLK of Primary SPI Port.
Secondary Serial Interface (3-wire SPI Only)	
CSb2	CSb of secondary SPI Port. **Assignable to GPIO0 only.
SDIO2	SDIO of a secondary SPI Port. **Assignable to GPIO1 only.
SCLK2	SCLK of a secondary SPI port. **Assignable to GPIO2 only.

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3.12. Device Initialization and Reset

Once power is applied and RSTb is de-asserted, the device begins loading preconfigured register values and configuration data from NVM, and performs other initialization tasks. Communicating with the device through the serial interface is possible once this initialization period is complete (see t_{RDY}). No output clocks will be generated until initialization is complete, and the device locks to the external (VC)XO/XTAL (see t_{START_XO} and t_{START_XTAL}). A reset, initiated using the RSTb pin or through the Device API RESTART command, restores all registers to the values stored in NVM, and all circuits, including the serial interface, will be restored to their initial state. All clocks will stop during a hard reset. Other feature-specific resets are also available. See the Si5518/12/10/08 Reference Manual and AN1360: Serial Communications and API Programming Guide for Si536x, Si540x, and Si55xx Devices for more information on different methods of resetting the device.

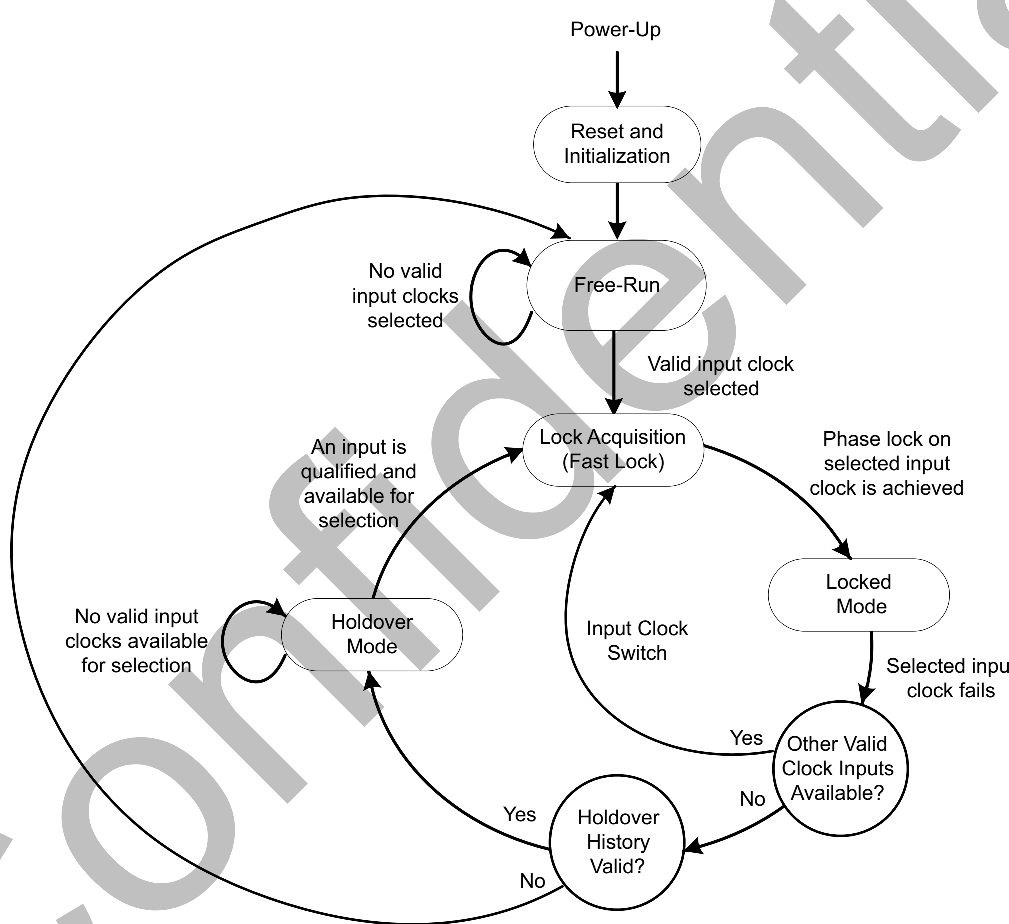

Figure 8. Modes of Operation

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3.13. Modes of Operation (RFPLL, DSPLL A, DSPLL B)

Once initialization is complete each PLL independently operates in one of four modes: Free-Run, Lock Acquisition, Locked, or Holdover. A state diagram showing the modes of operation is shown in Figure 8 on page 20. The following sections describe each of these modes in greater detail.

3.13.1. Free-Run Mode

The PLLs will automatically enter Free-Run Mode once power is applied to the device and initialization is complete. In this mode the frequency accuracy of the generated output clocks is entirely dependent on the frequency accuracy of the reference clock source. If a XTAL is connected to the XA/XB pins then the clock outputs will generate a frequency at the XTAL's accuracy. For example, if a XTAL is operating at –28 ppm then clock outputs will also be –28 ppm. The same is true if a XO is connected at the XO_IN inputs instead of using XTAL at XA/XB. The frequency stability of the outputs will also be determined by the XTAL or XO.

When a TCXO or OCXO is connected to the RFPLL inputs, then the frequency accuracy and stability of the outputs will be determined by the TCXO or OCXO. This is recommended for applications that need better accuracy and stability than what the XTAL or XO can provide.

3.13.2. Lock Acquisition Mode

Each of the PLLs independently monitors its configured inputs for a valid clock. If at least one valid clock is available for synchronization, a PLL will automatically start the lock acquisition process. If the fast lock feature is enabled, they will acquire lock faster than the PLL Loop Bandwidth would provide and then transition to the normal PLL loop bandwidth. During lock acquisition the outputs will generate a clock that follows the VCO frequency change as it pulls-in to the input clock frequency.

The PLL_STATUS Device API command reports the lock status of a PLL. When the PLL output frequency is within the threshold defined on the Frequency LOL (FLOL) page in ClockBuilder Pro, the PLL_OUT_OF_FREQUENCY bit de-asserts. Some time after that, the PLL will pull in the remaining phase defined on the Phase LOL (PLOL) page in ClockBuilder Pro. Once the PLL is frequency and phase locked, the PLL_LOSS_OF_LOCK (LOL) bit de-asserts, and the PLL enters locked mode.

3.13.3. Locked Mode

Once locked, the PLL will generate clock outputs that are both frequency and phase locked to their selected input clocks. The PLL loop bandwidths can be independently configured. Any frequency changes (e.g., because of temperature variations) of the reference clock (REF_IN) within the PLL loop bandwidth will be corrected by the loop ensuring 0 ppm lock to its input clock (IN). Any frequency changes of the reference clock (REF_IN) beyond the PLL loop bandwidth will pass through to the clock output.

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3.13.4. Holdover Mode

Any of the PLLs will automatically enter Holdover Mode when the selected input clock becomes invalid, holdover history is valid, and no other valid input clocks are available for selection. Each PLL uses an averaged input clock frequency as its final holdover frequency to minimize the disturbance of the output clock phase and frequency when an input clock suddenly fails. The holdover circuit for each PLL stores historical frequency data while locked to a valid input clock. The final averaged holdover frequency value is calculated from a programmable window within the stored historical frequency data. Both the window size and delay are programmable as shown in the figure below. The window size determines the amount of holdover frequency averaging. The delay value allows ignoring frequency data that may be corrupt just before the input clock failure.

The maximum window size is a function of input frequency and is reported in ClockBuilder Pro for each PLL. 240 seconds is the maximum window size for 1 PPS/PP2S inputs as shown in the figure below. For higher frequency inputs up to 5000 seconds of holdover history can be stored.

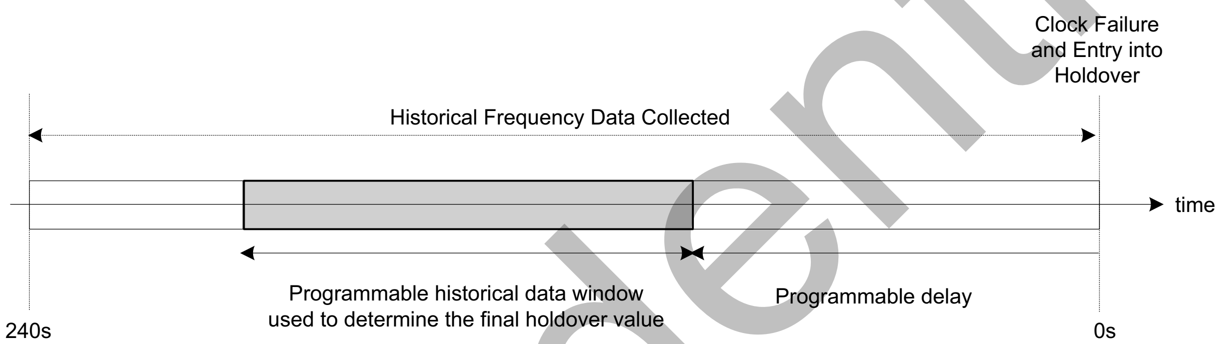

Figure 9. Programmable Holdover Window

When entering holdover, a PLL will pull its output clock frequency to the calculated averaged holdover frequency. While in holdover, the output frequency drift is entirely dependent on the external reference clock connected to the REF_IN input and, if an OCXO/TCXO holdover reference is used, also dependent on the holdover reference. If the input clock becomes valid, a PLL will automatically exit the holdover mode and re-acquire lock to the new input clock. This process involves pulling the output clock frequency to achieve frequency and phase lock with the input clock. This pull-in process is glitchless.

The PLL output frequency when exiting holdover can be ramped. Just before the exit is initiated, the difference between the current holdover frequency and the new desired frequency is measured. Using the calculated difference and a user-selectable ramp rate, the output is linearly ramped to the new frequency. The PLL loop BW does not limit or affect ramp rate selections (and vice versa). ClockBuilder Pro defaults to ramped exit from holdover and free-run. The ramp rate settings are configurable for initial lock (exit from Free-Run), exit from Holdover, and clock switching.

If ramped holdover exit is disabled, the holdover exit is governed either by (1) the PLL loop BW or (2) the PLL Fast-lock bandwidth, when enabled.

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3.14. IEEE 1588 Mode

3.14.1. Synchronizing to a Master Clock when in IEEE 1588 Mode

When IEEE 1588 mode is used (see figure below), the servo loop software will check the Announce Messages it receives from upstream master nodes (in its clock domain), and, using the BMCA, will choose the master with the best clock (which could be itself). It then begins to synchronize its local clock to that of the master's clock using IEEE 1588 timestamps.

The IEEE 1588 Servo Loop Software will acquire lock using the Startup Time Constant and then transition to the Main Time Constant once the node synchronizes its local clock to that of the selected master's clock. These time constants effectively set the servo loop bandwidth and are user configurable.

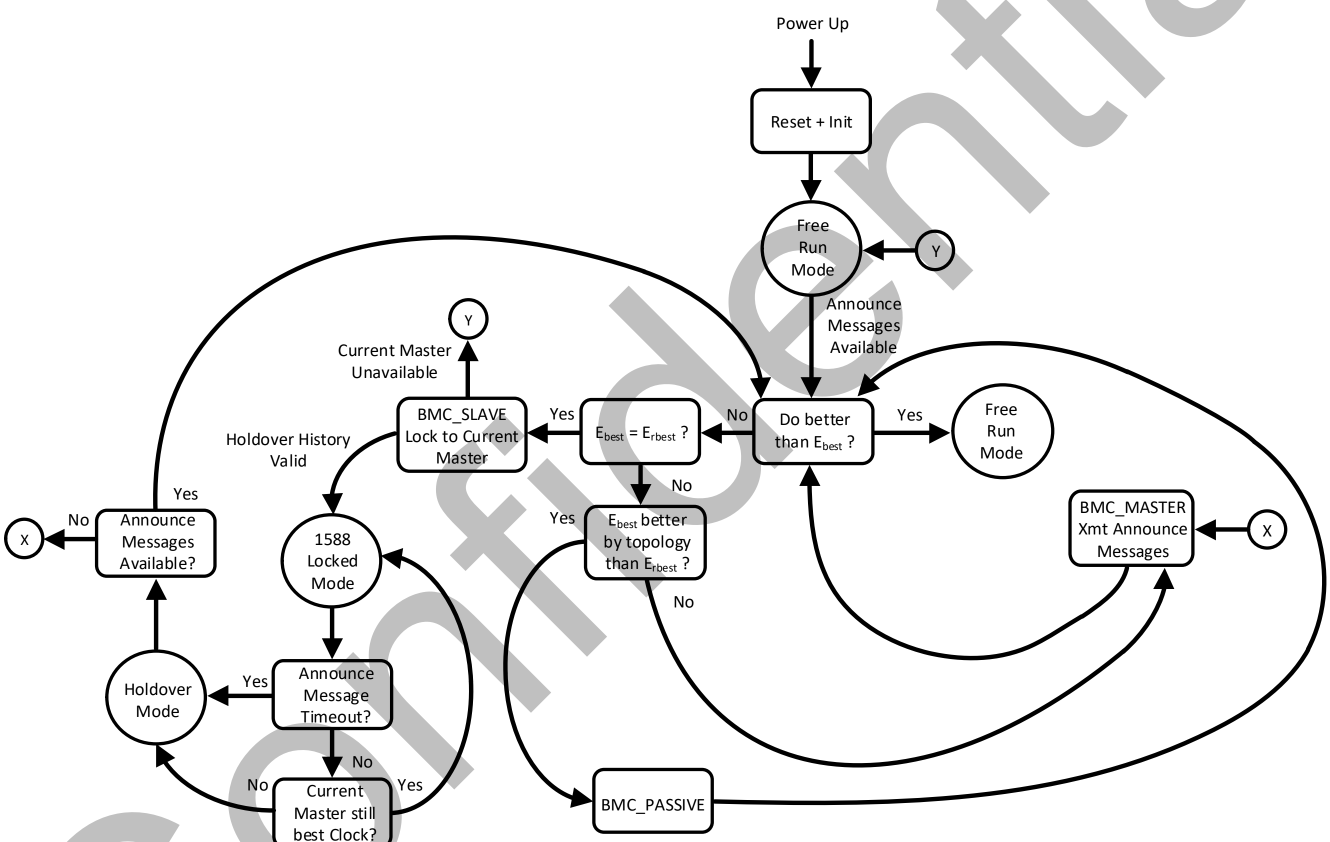

Figure 10. Modes of Operation (IEEE 1588 Mode - BMCA)

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3.15. PTP Holdover Mode (IEEE 1588 Holdover Mode)

When timestamps are no longer available (either due to Announce Message timeout from the current master clock or due to selecting a better clock from a remote master via BMCA), the node will enter PTP holdover. In this mode, the accuracy and stability of the output clocks synchronized to PTP will be dependent on the PTP clock average calculation, which is dependent on the "control average" time constant, as well as the stability of the input reference clock. If the reference is from a SyncE input, then this PTP holdover mode will be referred to as "PTP holdover with physical layer assist", and the outputs will assume the stability of the SyncE clock.

If there is no physical layer clock synchronizing the PLL steered by PTP, then it will synchronize to the local reference oscillator, and the outputs will assume the stability of this oscillator. This PTP holdover mode is referred to as "holdover without physical layer assist". Once the connection to an upstream master has been reestablished and the IEEE 1588 timestamps are once again available, the servo loop will exit from PTP holdover and begin synchronizing its local clock to that of the new master.

3.16. Status and Alarms

The Si5518 monitors the input clocks and reference input for status and alarms. The status and alarms provide the internal state machine with real time phase and frequency monitoring used for making decisions, such as switching inputs or entering holdover.

3.16.1. Input Clock Status

All input clocks are continuously monitored for faults using the Loss-of-Signal (LOS), Out-of-Frequency (OOF), and Phase Monitor (PHMON) alarms. When a differential input is configured as a dual CMOS input, then each CMOS input is independently monitored. Any enabled alarms for an input, such as LOS/OOF/PHMON, are logically ORed together to produce the input invalid alarm.

Any input clock with an alarm is not valid until all alarms are cleared. If a PLL is locked to an input clock and that input clock becomes invalid, then the PLL may either switch to a valid input or enter holdover mode, depending on how the device is programmed.

API commands can be used to indicate if an alarm is valid, pending short term fault, under validation or invalid.

3.16.1.1. Loss of Signal (LOS)

The loss of signal alarm measures the period of each input clock cycle to detect phase irregularities or missing clock edges. Each of the input LOS circuits has its own programmable sensitivity, which allows missing edges or intermittent errors to be ignored. Loss of signal sensitivity is configurable using the ClockBuilder Pro utility. The LOS status for each of the monitors is accessible by checking the INPUT_STATUS API.

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3.16.1.2. Out of Frequency (OOF) Detection

All inputs are monitored for frequency accuracy with respect to an OOF reference which is selected in Clock-Builder Pro. The OOF reference can be selected as either the XO/XTAL/VCXO or the OCXO/TCXO in dual reference mode. When available it is recommended to select the OCXO/TCXO as the OOF reference since it will have a tighter frequency accuracy compared to a free-running XTAL or a VCXO.

The OOF set and clear thresholds must be wider than the combined frequency accuracy of the OOF reference plus the stability of the input clock. A valid input clock frequency is one that remains within the OOF frequency range which is configurable from ±0.1 ppm to ±500 ppm in steps of 0.1 ppm. A configurable amount of hysteresis is also available to prevent the OOF status from toggling at the failure boundary. An example is shown in the figure below. In this case, the OOF monitor is configured with a valid frequency range of ±15 ppm with 5 ppm of hysteresis. This OOF configuration will support a dual reference mode with a Stratum 3 level OCXO/TCXO and a SyncE input which both have ±4.6 ppm overall frequency accuracy.

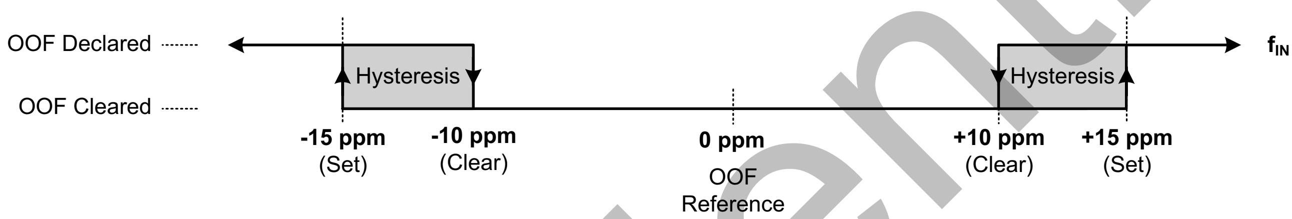

Figure 11. Example of Precise OOF Monitoring Assertion and De-assertion Triggers

3.16.1.3. Phase Monitor (PHMON)

If a clock input undergoes a phase transient, a PLL locked to that input will filter the transient by its loop bandwidth; however, the transient will propagate to the output. Transients that propagate to the output have the potential to negatively impact downstream devices.

Phase Monitor (PHMON) alarm monitors the input clock phase or accumulated phase, and, if the input transient exceeds the programmable threshold, the PHMON alarm will be asserted. PHMON, like the other alarms, is quick to be asserted when the thresholds are violated yet slower to be de-asserted to prevent chattering around the threshold.

Each input clock has an independent PHMON alarm. Each alarm can be enabled/disabled individually, and its associated threshold may be independently configured. Note that OOF must be enabled and properly configured for PHMON to operate.

A ZDM input may use the PHMON alarm for monitoring purposes. However, it will have no effect on PLL bandwidth selection and will not cause input switching.

3.16.1.4. Short Term Holdover

The Short-Term Holdover (STHO) feature may be used when the input clock is expected to have a short-term fault and then quickly recover.

If an input clock has STHO enabled, and an LOS/OOF/PHMON alarm is asserted, then a PLL locked to that input will enter holdover and wait for a programmable duration until all alarms on the input clock are de-asserted.

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If all alarms on the input clock are de-asserted before the programmable amount of time has passed, then the PLL will gracefully relock to the same input clock. If all the alarms on the input clock are not de-asserted before the programmable amount of time has passed, then the PLL will either switch to the next priority input clock or remain in holdover, depending on the input clock selection settings.

If STHO is disabled, then the PLL will skip the short-term holdover time and immediately switch to the next priority input clock or enter holdover, depending on the input clock selection settings.

STHO may be programmed using Clock Builder Pro to set the duration or to enable or disable the feature for each input clock individually. Note that the STHO setting will affect all PLLs assigned to that input.

3.16.2. PLL Status

RFPLL, DSPLL A, DSPLL B, and PPSPLL are continuously monitored for Loss-of-Lock (LOL). The final LOL status indicator is the logical OR of the Frequency Loss-of-Lock and Phase Loss-of-Lock statuses. See the Si5518/12/10/08 Reference Manual for more information.

3.16.2.1. Loss of Lock (LOL)

There is a loss of lock (LOL) monitor for each of the PLLs (RFPLL, DSPLL A, DSPLL B, and PPSPLL). The LOL monitor asserts when a PLL has lost synchronization with its selected input clock. Any of the GPIOs can be programmed as a dedicated loss-of-lock pin that reflects the loss-of-lock condition for each of the PLLs. The LOL monitor measures both the frequency and phase difference between the input and feedback clocks of the phase detector. The frequency monitor gives frequency lock detection (FLOL) while the phase monitor indicates true phase lock PLOL by detecting one or more single slips. Both the phase and frequency LOL monitors have clear and set thresholds and a timer to prevent LOL assertion from toggling or chattering as the DSPLL completes lock acquisition. The cycle slip detector also has configurable sensitivity.

3.16.2.2. Frequency Loss of Lock (FLOL)

The Frequency Loss-of-Lock (FLOL) monitor measures the frequency difference between the input clock and the feedback clock. The upper and lower LOL thresholds are programmable, which dictates when the alarm will be asserted or de-asserted. It is recommended to program the clear threshold to be less than the set threshold to allow for hysteresis in the FLOL set/clear behavior. This prevents the FLOL alarm from chattering or causing multiple interrupts. FLOL, like the other alarms, is quick to be asserted when the threshold is violated yet slower to be de-asserted. The alarm validates that the frequency difference between the input and feedback clocks has truly settled to within the LOL clear threshold before the FLOL alarm is de-asserted. The time required to validate the frequency difference increases as the loop bandwidth of the PLL decreases.

3.16.2.3. Lock Status Bits

There are four lock status bits that serve as four additional Frequency LOL thresholds. The Status Bit (STB) is asserted if the frequency difference between the input clock and feedback clock exceeds the programmable STB threshold. The assertion or de-assertion of an STB does not contribute to the FLOL or LOL status. Rather, they serve as a way to track the lock acquisition process for DSPLL's with a loop bandwidth of <10 Hz. The lock status bits may be read via the API. In the lock acquisition process, the de-assertion of a STB does not indicate that the PLL is frequency locked. This is because the frequency may chatter around the STB threshold. On the other hand, the deassertion of FLOL requires the frequency difference to truly settle below the LOL clear threshold.

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3.16.2.4. Phase Loss of Lock (PLOL)

The Phase Loss-of-Lock (PLOL) alarm measures the phase difference between the input clock and feedback clock. The PLOL set threshold is programmable so the alarm will assert or de-assert depending on phase difference between the input and feedback clocks relative to the threshold setting. It is recommended to set the clear threshold below the set threshold to allow for hysteresis. This prevents the alarm from chattering or causing multiple interrupts. During the lock acquisition process, the input clock and feedback clock will likely have a significant frequency mismatch; so, the PLOL is not asserted until FLOL is de-asserted. Once FLOL has been de-asserted, the two frequencies are stable with respect to each other. Then the feedback clock phase can be pulled in to within the PLOL clear threshold.

3.16.2.5. Cycle Slip Detection

RFPLL, DSPLLA, and DSPLLB may be monitored for cycle slips. Like the PLOL alarm, cycle slip detection is not enabled until FLOL is de-asserted. Additionally, PLOL must be enabled for cycle slip detection to be enabled. Cycle slips both in the positive and negative direction are monitored. The API can be used to read the total count of positive cycle slips, negative cycle slips and the total count or both positive and negative slips.

3.16.3. External Reference Status

An external reference must always be provided to the device. The Si5518 will monitor the external reference input for LOS, OOF, and LOL. If a fault is detected on the external reference, then the outputs will be disabled. Any external reference faults may be read via the API.

3.16.4. Interrupt Status

The interrupt flag is asserted when any of the status indicators of the device changes state. The interrupt status may be assigned a GPIO pin, or it may be checked using an API command to show which status indicator caused the interrupt to be asserted.

The Interrupt Configuration page in ClockBuilder Pro lists all the status indicators that can be programmed to activate the interrupt pin.

The status indicators that are enabled are logically OR’d together so that the assertion of any of these status indicators will cause the interrupt pin to assert. The interrupt pin status depends on the sticky versions of the individual status indicators, so the interrupt pin will stay asserted until the sticky status indicators are cleared.

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3.17. Serial Interface

Configuration and operation of the Si5518 is controlled by reading and writing API commands using the I2C or SPI interface. The primary SPI mode operates in either 4-wire or 3- wire modes. A second SPI port, which operates only in 3-wire mode, can also be configured allowing dual port access to the device. An internal arbiter prevents contentions during bus operations so that both ports can be used simultaneously. The following tables define the GPIO pins assigned to the primary and secondary SPI ports, respectively.

Table 3. Primary Serial Interface Pins

Pin Number	3-Wire SPI	4-Wire SPI	I2C
55	CSb	CSb	A0
52	SDIO	SDI	SDA
53	SCLK	SCLK	SCK
56	Unused	SDO	A1

Table 4. Secondary Serial Interface Pins

Pin Number	SPI Pin	Assignable GPIO Pins
16	CS2b	GPIO0
18	SDIO2	GPIO1
19	SCLK2	GPIO2

3.18. NVM Programming

At power-up, the device loads its default configuration and settings from internal non-volatile memory (NVM). The NVM can be preprogrammed at the factory with a custom frequency plan such that the device starts generating clocks on its first power-up, or the NVM can be programmed in the field using the API command set. NVM programming in the field must be done with VDDA set to 3.3V. NVM programming in the field is not supported in Low-Power mode. For more details on NVM programming options, refer to AN1360: Serial Communications and API Programming Guide for Si536x, SI540x, and Si55xx Devices and Si5518/12/10/08 Reference Manual.

3.19. Application Programming Interface (API)

Communication between the customer's host processor and the Si5518 internal microcontroller (MCU) is accomplished through the serial interface. The Si5518 MCU contains firmware that allows users to have command-level access to the device API. Internal registers are not accessible through the API because all features of the Si5518 can be accessed through the Device API. The primary serial port (SPI or I2C) allows programming of the Si5518, and the secondary serial port (SPI 3-wire only) is intended for Phase Readback and status monitoring operations. The host processor can also communicate with the Si5518 using Skyworks' optional AccuTime IEEE 1588 software and API. The AccuTime software runs on the host processor. See the Si5518/12/10/08 Reference Manual for more information and examples of the API. Details of the API commands are available through ClockBuilder Pro. For instructions to use the Device API, and for instructions on programming the clock device, see AN1360: Serial Communications and API Programming Guide for Si536x, SI540x, and Si55xx Devices.

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3.20. AccuTime IEEE 1588 Software

The Si5518 may be combined with optional AccuTime™ IEEE 1588 software to create a complete IEEE 1588 solution for time, phase, and frequency synchronization. AccuTime 1588 software consists of a unique servo algorithm paired with a protocol stack that all runs on the customer's host processor.

The architecture of AccuTime is shown in the simplified figure below. AccuTime is a layered architecture consisting of the customer's hardware platform and the OSAL and OEM at the bottom (system-dependent) layer, including system-dependent configuration files to customize the AccuTime software for the OS and HW platform. Next is the System-Independent Layer consisting of the AccuTime software. The example applications are provided with AccuTime and include the Sync Timing Util application and ESMC handler.

The System-Independent layer interfaces with the user's OS and hardware via API calls through the OSAL and OEM layers. This includes the C API library for controlling and monitoring the Si5518 device.

The OEM Abstraction layer allows low level communications with the Si5518 via SPI or I2C, GPIO, etc. The OEM layer communicates with the Linux kernel via kernel system calls and IOCTL. Device drivers in the Linux kernel communicate with the hardware devices in the user's hardware platform which includes the Ethernet PHY + MAC, Time of Day (ToD) counter block, serial input/output for transmitting/receiving ToD information, as well as the Si5518.

The OEM and OSAL layers use system calls and rely on the Linux kernel. In the OEM layer case, system calls are used to interact with the hardware, whereas in the OSAL layer case, system calls are used to leverage the software specific functions provided by the kernel (mutexes, semaphores, queues, etc.).

The AccuTime 1588 Protocol Stack provides an application in the user space running on the host processor on top of the Linux OS. The protocol stack processes the PTP messages and passes the necessary data to the PTP servo. The servo loop controls the 1588 DCO operation to the Si5518 device to adjust the system clock it sends to synchronize the ToD counter in the host to align it with the ToD in the master.

Software setup, configuration, API / CLI command libraries, and porting details are fully documented in the AccuTime Software Release.

AccuTime software is available under a license. Contact your Skyworks Representative for more information.

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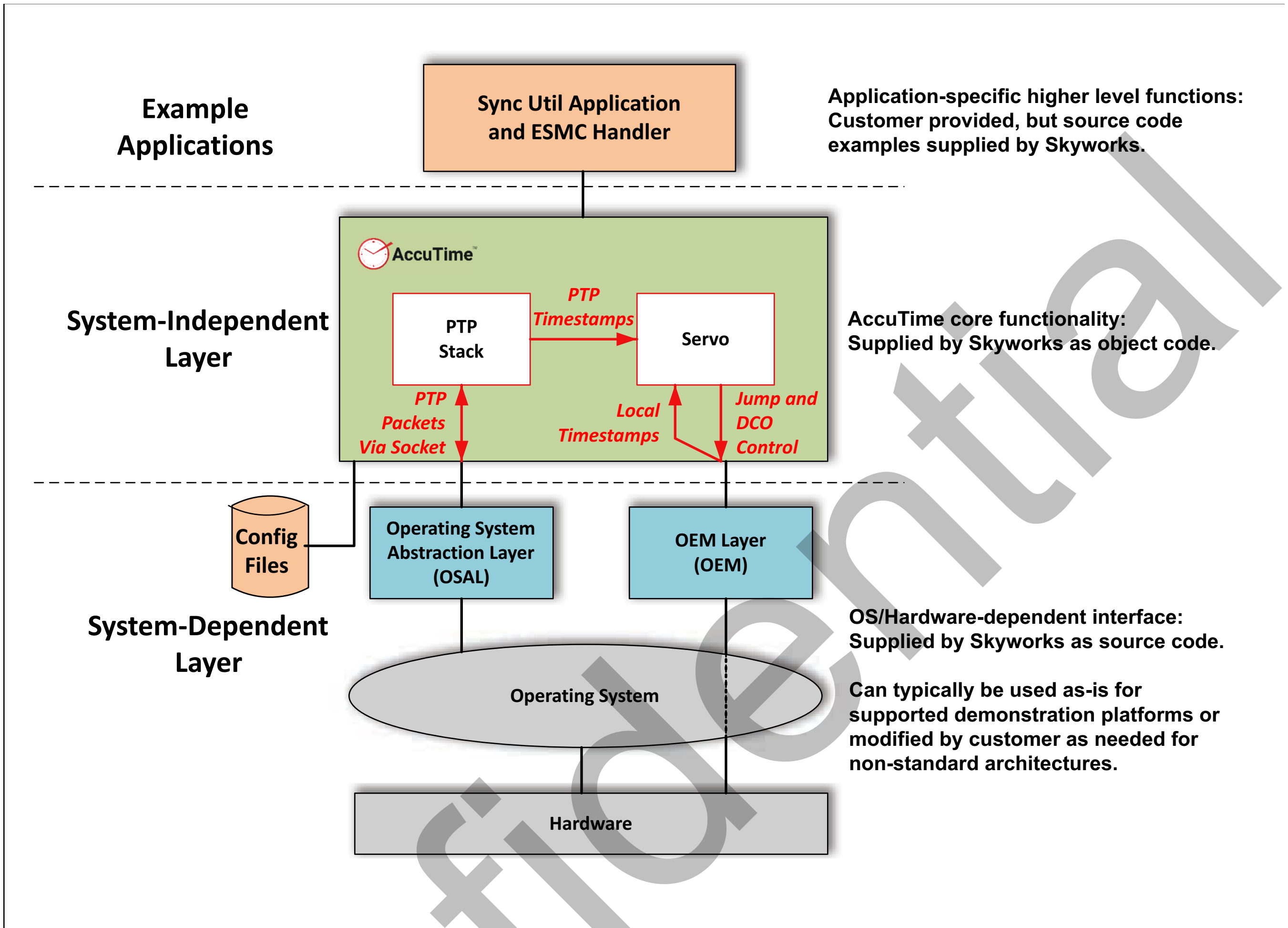

Figure 12. AccuTime Simplified Architecture

3.21. Power Supplies

The Si5518 has 14 power supply pins. The separate power supplies are used for different functions, providing power locally where it is needed on the die to improve isolation. When no outputs are enabled for a particular VDDOx, that supply pin may be left unconnected. Please refer to the AN1293: Si55xx Schematic Design and Board Layout Guide for more details on power management and filtering recommendations.

3.21.1. Power Supply Sequencing

There are no power sequencing requirements between supplies. VDDA and VDD18 should be powered up before releasing RSTb. VDDA must be equal to the highest voltage supply. See Table 8 on page 34 for supply ramp rate specification.

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3.21.2. Power Supply Ramp Rate

Power supply ramp times must stay within the maximum supply voltage ramp rate as defined in Table 8, "DC Characteristics," on page 34.

3.21.3. Low-Power Mode

In Low-Power Mode, the analog core supply voltage (VDDA) of the Si5518 is set to 1.8 V in order to reduce power consumption. Since VDDA must be equal to the highest voltage applied to the Si5518, in Low-Power Mode, all voltage supplies including VDDO must be 1.8 V. A 1.8 V VDDO restricts the output format to S-LVDS, LVCMOS, or HCSL. If LVPECL or LVDS output format is required, Low-Power Mode cannot be used. NVM programming in the field is not supported in Low-Power Mode since NVM programming requires VDDA to be 3.3V. Additionally, the VCXO mode is not supported in Low-Power Mode. See the Si5518/12/10/08 Reference Manual for information on VDDREF and XO/XTAL connections and terminations for Low-Power Mode.

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4. Electrical Specifications

All minimum and maximum specifications in the following tables are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and at an operating temperature of 25 °C, unless otherwise noted.

Table 5. Absolute Maximum Ratings [1, 2, 3, 4]

Parameter	Symbol	Test Condition	Value	Unit
DC Supply Voltage	V_{DDIN}		–0.5 to 3.8	V
	V_{DDREF}		–0.5 to 3.8	V
	V_{DD18}		–0.5 to 2.4	V
	V_{DDA}		–0.5 to 3.8	V
	V_{DDO}		–0.5 to 3.8	V
	V_{DDIO}		–0.5 to 3.8	V
Input Voltage Range	V_{I1}	REF_IN/REF_INb, INx/INxb	–0.85 to 3.8	V
	V_{I2}	GPIO0-3, RSTb, SCLK, SDA/SDIO, A0/CSb	–0.5 to 3.8	V
	V_{I3}	XA/XB	–0.5 to 2.7	V
Latch-up Tolerance	LU		JESD78 Compliant	
ESD Tolerance	HBM	100 pF, 1.5 kΩ	2.0	kV
Storage Range	TSTG		–55 to 150	°C
Maximum Junction Temperature in Operation	T_{JCT}		125	°C
Soldering Temperature (Pb-free profile) [5]	T_{PEAK}		260	°C
Soldering Time at T_{PEAK} (Pb-free profile) [5]	T_P		20–40	sec

1. Exposure to maximum rating conditions for extended periods may reduce device reliability. Exceeding any of the limits listed here may result in permanent damage to the device.
2. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
3. RoHS-6 compliant.
4. For more packaging information, go to https://www.skyworksinc.com/Product_Certificate.aspx.
5. The device is compliant with JEDEC J-STD-020.

Table 6. Thermal Conditions

Parameter	Symbol	Test Condition	Typical Value		Unit
			JEDEC [1]	CEVB [2]	
Thermal Resistance Junction to Ambient	Θ_{JA}	Still Air	16.15	11.17	°C/W
		1 m/s	10.77	8.10	°C/W
		2 m/s	9.63	7.53	°C/W
Thermal Resistance Junction to Board	Ψ_{JB} [3]	Still Air	3.33	3.08	°C/W
Thermal Resistance Junction to Top Center	Ψ_{JC}	Still Air	0.03	0.05	°C/W

1. Based on PCB dimension: 4" x 4.5", PCB thickness: 1.6 mm, Number of Cu Layers: 2.
2. Customer EVB: 8-layer board, board dimensions: ~9x9", all 8-layers are copper poured.
3. Ψ_{JB} can be used to calculate the junction temperature based on the board temperature and power dissipation for a given frequency plan, Tj = TPCB + (Ψ_{JB}*PD). TPCB should be measured as close to the Si5518 DUT as possible since temperature may vary across the PCB.

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Table 7. Recommended Operating Conditions

V_{DD18} = 1.8 V ±5%, V_{DDA} = V_{DDREF} = 3.3 V ±5%; All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C.
Low-Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDREF} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Temperature	T_A		–40	25	95	°C
Board Temperature	T_B		–40	65	105	°C
Junction Temperature	TJ_{MAX} [1]		—	—	125	°C
Core Supply Voltage	V_{DD18}		1.71	1.80	1.89	V
	V_{DDA} [2]		3.14	3.30	3.47	V
		Low-Power Mode	1.71	1.80	1.89	V
	V_{DDREF}		3.14	3.30	V_{DDA} [2]	V
		Low-Power Mode	1.71	1.80	1.89	V
Input Supply Voltage	V_{DDIN}		3.14	3.30	V_{DDA} [2]	V
			2.38	2.50	2.62	V
			1.71	1.80	1.89	V
GPIO Supply Voltage	V_{DDIO}		3.14	3.30	V_{DDA} [2]	V
			2.38	2.50	2.62	V
			1.71	1.80	1.89	V
Clock Output Driver Supply Voltage	V_{DDO}		3.14	3.30	V_{DDA} [2]	V
			2.38	2.50	2.62	V
			1.71	1.80	1.89	V

1. Ambient temperature of 95 °C may not be possible with all configurations. This is dependent on device configuration. Tj cannot exceed a max of 125 °C.
2. V_{DDA} must be greater than or equal to the highest voltage applied to the device. In Low-Power Mode, all voltage supplies must be set to 1.8 V.

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Table 8. DC Characteristics

V_{DD18} = 1.8 V ±5%, V_{DDA} = V_{DDREF} = 3.3 V ±5%; All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C.
Low-Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDREF} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Core Supply Current (V_{DD18} + V_{DDA})	I_{DD18}	Si5518 [1, 2]	—	380	640	mA
	I_{DDA}	Si5518 [1, 2]	—	210	230	mA
	I_{DD18_PD}	RSTb = 0	—	120	300	mA
	I_{DDA_PD}	RSTb = 0	—	15	16	mA
Periphery Supply Current (V_{DDIN} + V_{DDIO} + V_{DDREF})	I_{DDIN} + I_{DDIO}	Si5518 [1, 2]	—	58	76	mA
	I_{DDREF}	Si5518 [1, 2]	—	12	14	mA
	I_{DDIN_PD} + I_{DDIO_PD} + I_{DDREF_PD}	RSTb = 0	—	2	3	mA
Output Buffer Supply Current (V_{DDOX})	I_{DDOX} (per output)	LVPECL (2.5 V, 3.3 V) @ 122.88 MHz [3]	—	24	26	mA
		LVDS (2.5 V, 3.3 V) @ 122.88 MHz [3]	—	13	15	mA
		S-LVDS (1.8 V) @ 122.88 MHz [3]	—	12	14	mA
		3.3 V LVCMOS @ 122.88 MHz [4]	—	19	22	mA
		2.5 V LVCMOS @ 122.88 MHz [4]	—	15	17	mA
		1.8 V LVCMOS @ 122.88 MHz [4]	—	11	12	mA
		HSCL Internal Termination (1.8 V, 2.5 V, 3.3 V) @ 122.88 MHz [5]	—	20	23	mA
		CML (1.8 V, 2.5 V, 3.3 V) @ 122.88 [3]	—	14	17	mA
	I_{DDOX_PD}	RSTb=0	—	0.23	0.3	mA
Total Power Dissipation	P_D	Si5518 [1]	—	1.9	2.6	W
		Si5518 Low-Power Mode [2]	—	1.4	2	W
Supply Voltage Ramp Rate	T_{VDD}	Fastest V_{DD} ramp rate allowed on startup	—	—	100	V/ms

1. Typical test configuration: The following frequencies on 10 LVDS outputs: 2–491.52 MHz (Q), 1–122.88 MHz (Q), 2–1.92 MHz (Q), 1–100 MHz (NA), 1–50 MHz (NA), 2–156.25 MHz (NB), 1–125 MHz (NB). Excludes power dissipated in termination resistors. VDDIN = 1.8 V, VDDO = 3.3 V.
2. Typical test configuration: Same as Note 1, except all supplies set to 1.8 V for Low-Power Mode. Output formats changed to S-LVDS format.
3. Differential outputs terminated into an ac-coupled differential 100Ω load.
4. LVCMOS outputs measured into a 5-inch, 50Ω PCB trace with 5 pF load.
5. No external termination; amplitude 800 mVpp_se.

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Table 9. Input Specifications

V_{DD18} = 1.8 V ±5%, V_{DDA} = V_{DDREF} = 3.3 V ±5%; All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C.
Low-Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDREF} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
LVCMOS (XO/VCXO Applied to REF_IN)						
Input Frequency Range	f_{IN_CMOS}	Frequencies > 48 MHz are recommended for best performance.	30.72	—	250	MHz
Slew Rate [1, 2, 3]	SR		0.75	—	—	V/ns
Input Voltage	V_{IL}		—	—	V_{DDREF} x 0.3	V
	V_{IH}		V_{DDREF} x 0.7	—	—	V
Input Resistance	R_{IN}		—	63	—	kΩ
Duty Cycle	DC		40	—	60	%
Capacitance	C_{IN_SE}		—	1.25	—	pF
Differential (XO/VCXO Applied to REF_IN)						
Input Frequency Range	f_{IN_DIFF}	Frequencies > 48 MHz are recommended for best performance.	30.72	—	983.04	MHz
Voltage Swing [2]	V_{IN_DIFF}		200	350 (LVDS) 800 (LVPECL)	1800	mVpp_se
Slew Rate [1, 2, 3]	SR		0.75	—	—	V/ns
Duty Cycle	DC		40	—	60	%
Capacitance	C_{IN_DIFF}		—	2.5	—	pF
Crystal (Connected to XA/XB Pins)[4]						
Frequency Range	f_{IN_XTAL}		48	54	61.44	MHz
Load Capacitance	C_L		—	8	—	pF
Crystal Drive Level	d_L		—	—	200	µW
Equivalent Series Resistance	R_{ESR}		Refer to the "Si55xx/Si540x/Si536x Recommended XTALs Reference Manual" to determine ESR and Shunt Capacitance Values.			
Shunt Capacitance	C0					
Differential (INx/INxb)						
Input Frequency Range	f_{IN_DIFF}	Differential, AC-coupled	0.008	—	1000	MHz
	f_{IN_SE}	Single-ended, AC-coupled	0.008	—	250	MHz
Voltage Swing	V_{IN_DIFF}	Differential, AC-coupled	200	350 (LVDS) 800 (LVPECL)	1800	mVpp_se
	V_{IN_SE}	Single-ended, AC-coupled	400	1600	1800	mVpp_se
Slew Rate [3, 5]	SR		0.4	—	—	V/ns
Duty Cycle	DC		40	—	60	%
Capacitance	C_{IN_DIFF}		—	2.5	—	pF
LVCMOS (INx/INxb)						
Input Frequency Range	f_{IN_LVCMOS}		PP2S PPS 0.008	—	250	MHz
Slew Rate [3, 5]	SR		0.2	0.4	—	V/ns
Input Voltage	V_{IL}		—	—	V_{DDIN} x 0.3	V
	V_{IH}		V_{DDIN} x 0.7	—	—	V
Input Resistance	R_{IN}		—	63	—	kΩ
Duty Cycle	DC		40	—	60	%
Capacitance	C_{IN_SE}		—	1.25	—	pF

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Table 9. Input Specifications (Continued)

V_{DD18} = 1.8 V ±5%, V_{DDA} = V_{DDREF} = 3.3 V ±5%; All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C.
Low-Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDREF} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Output Synchronization Pin (OSYNC)						
Update Rate	f_{UR}		—	—	150	Hz
Input Voltage	V_{IL}		—	—	V_{DDIO} x 0.3	V
	V_{IH}		V_{DDIO} x 0.7	—	—	V
Minimum Pulse Width [6]	PW		3	—	—	ms
Delay variation from OSYNC de-asserted to output re-enabled [7, 8]	tsync		–1.6	—	1.6	ns
Internal Pull-Up	R_{IN}		—	20	—	kΩ
Other Control Input Pins (RSTb, FINC, FDEC, OE, PLLx_FORCE_HO, PLLx_INSEL[#], IN_FAIL[#])						
Update Rate	f_{UR}	RSTb [9]	—	—	1	Hz
		FINC, FDEC	—	—	800	kHz
Input Voltage	V_{IL}		—	—	V_{DDIO} x 0.3	V
	V_{IH}		V_{DDIO} x 0.7	—	—	V
Minimum Pulse Width	PW		150	—	—	ns
Programmable Internal Pullup, Pulldown	R_{IN}		—	20	—	kΩ

1. The minimum slew rate on the XO/VCXO applied to REF_IN is recommended to meet the specified jitter performance.
2. To achieve this slew rate and voltage swing, use one of the XOs or VCXOs from the "Si55xx/Si540x/Si536x Recommended XTALs Reference Manual" placed as close as possible to the REF_IN pins.
3. Slew rate can be estimated using the following simplified equation: SR = ((0.8 – 0.2) x VIN_VPP_se)/tr.
4. To meet specified jitter performance use one of the XTALs from the "Si55xx/Si540x/Si536x Recommended XTALs Reference Manual".
5. The minimum slew rate on the input clock applied to INx/INxb is recommended to meet the specified input-to-output delay and close-in phase noise (<1 kHz) performance.
6. No API commands can be sent to the device while the OSYNC pin is asserted.
7. Nominal delay is reported in ClockBuilder Pro and will vary based on configuration.
8. OSYNC delay variation is not specified for SYNC outputs.
9. Glitches and toggles on RSTb more frequent than fUR may cause the device to lock up in reset. Power cycle the device to restore operation.

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Table 10. I²C Timing Specifications (SCL, SDA)

V_{DD18} = 1.8 V ±5%, V_{DDA} = V_{DDREF} = 3.3 V ±5%; All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C. Low-Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDREF} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A= –40 to 95 °C

Parameter	Symbol	Test Condition	Standard Mode 100 kbps		Fast Mode 400 kbps		Unit
			Min	Max	Min	Max	
SCL Clock Frequency	f_{SCL}		—	100	—	400	kHz
SMBus Timeout	—		25	35	25	35	ms
Hold time (Repeated) START condition	$t_{HD:STA}$		4.0	—	0.6	—	µs
Low Period of the SCL Clock	t_{LOW}		4.7	—	1.3	—	µs
HIGH Period of the SCL Clock	t_{HIGH}		4.0	—	0.6	—	µs
Setup Time for a Repeated START Condition	$t_{SU:STA}$		4.7	—	0.6	—	µs
Data Hold Time	$t_{HD:DAT}$		100	—	100	—	ns
Data Setup Time	$t_{SU:DAT}$		250	—	100	—	ns
Setup Time for STOP Condition	$t_{SU:STO}$		4.0	—	0.6	—	µs
Bus Free Time between a STOP and START Condition	t_{BUF}		4.7	—	1.3	—	µs
Data Valid Time	$t_{VD:DAT}$		—	3.45	—	0.9	µs
Data Valid Acknowledge Time	$t_{VD:ACK}$		—	3.45	—	0.9	µs

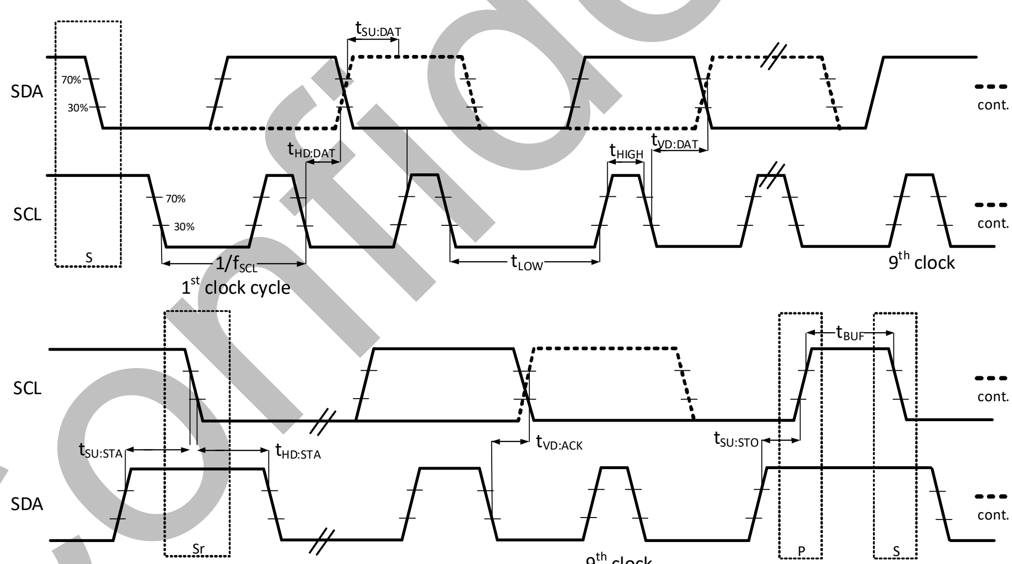

Figure 13. I²C Serial Port Timing Standard and Fast Modes

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Table 11. SPI Timing Specifications (4-Wire)

V_{DD18} = 1.8 V ±5%, V_{DDA} = V_{DDREF} = 3.3 V ±5%; All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, TA = –40 to 95 °C.
Low-Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDREF} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C

Parameter	Symbol	Min	Typ	Max	Unit
SCLK Frequency	f_{SPI}	—	—	30	MHz
SCLK Duty Cycle	T_{DC}	40	—	60	%
SCLK Period	T_C	33.333	—	—	ns
Delay Time, SCLK Fall to SDO Active	T_{D1}	—	12.5	20	ns
Delay Time, SCLK Fall to SDO	T_{D2}	—	10	15	ns
Delay Time, CSb Rise to SDO Tri-State	T_{D3}	—	10	20	ns
Setup Time, CSb to SCLK	T_{SU1}	5	—	—	ns
Hold Time, SCLK Fall to CSb	T_{H1}	5	—	—	ns
Setup Time, SDI to SCLK Rise	T_{SU2}	5	—	—	ns
Hold Time, SDI to SCLK Rise	T_{H2}	5	—	—	ns
Delay Time Between Chip Selects (CSb)	T_{CS}	5	—	—	µs

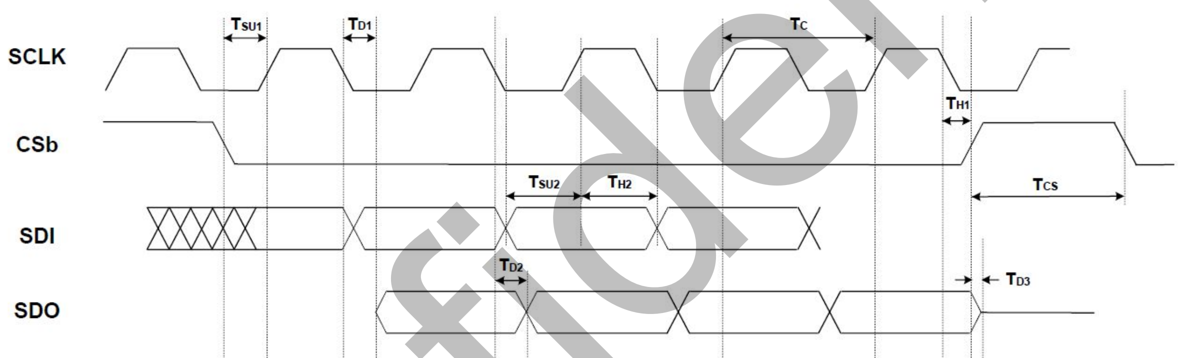

Figure 14. 4-Wire SPI Serial Interface Timing

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Table 12. SPI Timing Specifications (3-Wire)

V_{DD18} = 1.8 V ±5%, V_{DDA} = V_{DDREF} = 3.3 V ±5%; All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, TA = –40 to 95 °C. Low-Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDREF} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C.

Parameter	Symbol	Min	Typ	Max	Unit
SCLK Frequency	f_{SPI}	—	—	30	MHz
SCLK Duty Cycle	T_{DC}	40	—	60	%
SCLK Period	T_C	33.33	—	—	ns
Delay Time, SCLK Fall to SDIO Turn-on	T_{D1}	—	12.5	20	ns
Delay Time, SCLK Fall to SDIO Next-bit	T_{D2}	—	10	15	ns
Delay Time, CSb Rise to SDIO Tri-State	T_{D3}	—	10	20	ns
Setup Time, CSb to SCLK	T_{SU1}	5	—	—	ns
Hold Time, CSb to SCLK Fall	T_{H1}	5	—	—	ns
Setup Time, SDI to SCLK Rise	T_{SU2}	5	—	—	ns
Hold Time, SDI to SCLK Rise	T_{H2}	5	—	—	ns
Delay Time Between Chip Selects (CSb)	T_{CS}	5	—	—	µs

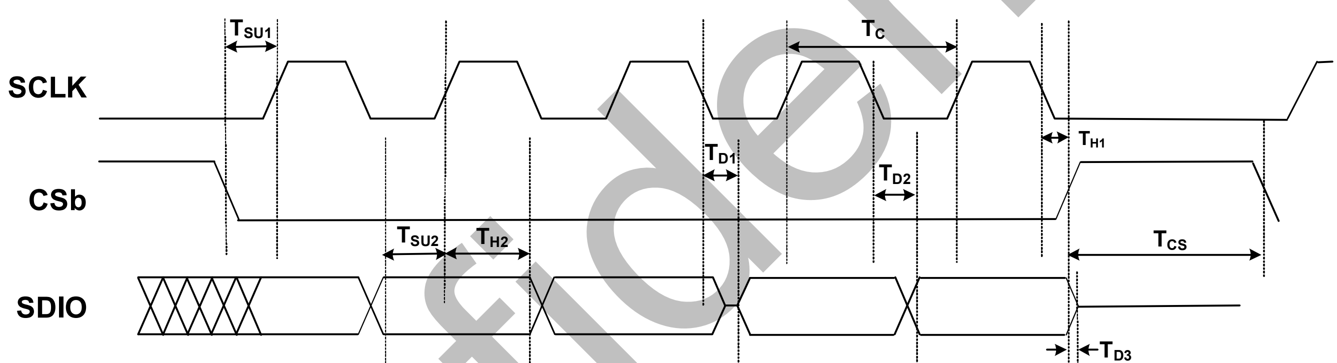

Figure 15. 3-Wire SPI Serial Interface Timing

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Table 13. Differential Clock Output Specifications

V_{DD18} = 1.8 V ±5%, V_{DDA} = V_{DDREF} = 3.3 V ±5%; All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95°C.
Low Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDREF} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95°C

Parameter	Symbol	Test Condition			Min	Typ	Max	Units
Output Frequency	f_{OUT}	Q Divider, Non PPS [1]			0.008	-	3200	MHz
		Q Divider, PPS			0.5	-	1	Hz
		NA Divider, Non PPS [2]			0.008	-	650	MHz
		NA Divider, PPS			0.5	-	1	Hz
		NB Divider[2]			0.008	-	650	MHz
Duty Cycle	DC	f < 400 MHz			49.5	50	50.5	%
		400 MHz < f < 3.2 GHz			48	50	52	
Output-to-Output Skew	T_{SK}	Q divider outputs, same differential format [3]			–50	-	50	ps
		MultiSynth (NA or NB) outputs, same differential format, same MultiSynth				-		
		VCXO buffered outputs, same differential format				-		
		Q divider outputs, differential SYSCLK to LVCMOS SYNC			0	-	300	
		Q divider to VCXO buffered outputs, same differential format [4]			–1200	-	1200	
OUT-OUTb Skew	T_{SK_OUT}	Skew between positive and negative output pins	VDDO=3.3V	LVPECL, LVDS, CML, and custom diff f < 491.52 MHz	-	-	10	ps
			VDDO=2.5V	LVPECL, LVDS, CML, and custom diff f < 491.52 MHz	-	-	25	
			VDDO=3.3V/2.5V	LVPECL, LVDS, CML, and custom diff f > 491.52 MHz	-	-	25	
			VDDO=1.8V	CML, S-LVDS, and custom diff All Frequencies	-	-	35	
Output Voltage Swing [5]	V_{OUT}	VDDO = 3.3 V/2.5 V		LVDS	330*SF	360*SF	380*SF	mVpp_se
		VDDO = 1.8 V		S-LVDS	350*SF	370*SF	410*SF	
		VDDO = 3.3 V/2.5 V		AC Coupled LVPECL	780*SF	840*SF	910*SF	
		VDDO = 3.3 V/ 2.5 V/1.8 V		CML	390*SF	420*SF	460*SF	
		VDDO = 3.3 V/2.5 V		Custom Diff 600 mVpp_se	560*SF	610*SF	650*SF	
Output Voltage Swing Scaling Factor (SF) OUT0-15	SF	f < 491.52 MHz			1	1	1	SF
		491.52 MHz < f < 983.02 MHz			0.9	0.95	1	
		983.04 MHz < f < 1.47456 GHz			0.8	0.9	1	
		1.47456 GHz < f < 2.47456 GHz			0.7	0.75	0.85	
		f > 2.47456 GHz			0.5	0.6	0.75	
Output Voltage Swing Scaling Factor (SF) OUT16/17 [6]	SF	f <491.52 MHz			1	1	1	
		491.52 MHz < f < 983.02 MHz			0.9	0.95	1	
		983.04 MHz < f < 1.47456 GHz			0.8	0.9	1	
		1.47456 GHz < f < 2.47456 GHz			0.7	0.75	0.85	
		f > 2.4576 GHz			0.5	0.6	0.75	
Common Mode Voltage	V_{CM}	VDDO = 3.3 V/2.5 V		LVDS, Custom Differential, CML	1.15	1.2	1.25	V
		VDDO = 1.8 V		S-LVDS, CML	0.85	0.9	0.95	
Rise and Fall Times (20% to 80%) OUT0-15	t_r/t_f	VDDO = 3.3 V/2.5 V		LVDS, AC Coupled LVPECL, Custom Diff	-	125	260	ps
		VDDO = 1.8 V		S-LVDS	-	150	270	
		VDDO = 3.3 V/ 2.5 V/1.8 V		CML	-	150	280	
Rise and Fall Times (20% to 80%) OUT16-17	t_r/t_f	VDDO = 3.3 V/2.5 V		LVDS, AC Coupled LVPECL, Custom Diff	-	140	300	
		VDDO = 1.8 V		S-LVDS	-	165	310	
		VDDO = 3.3 V/ 2.5 V/1.8 V		CML	-	165	320	
Differential Output Impedance	Z_O	All differential formats			-	100	-	Ω

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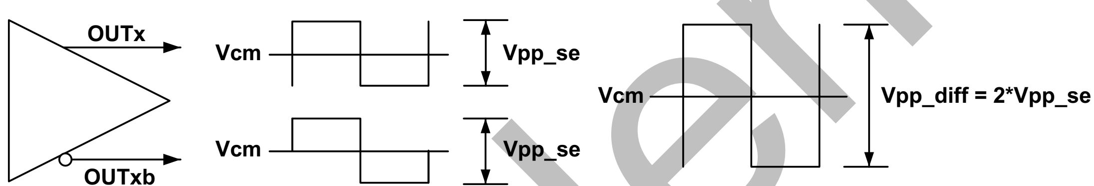
Table 13. Differential Clock Output Specifications (Continued)

V_{DD18} = 1.8 V ±5%, V_{DDA} = V_{DDREF} = 3.3 V ±5%; All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95°C.
Low Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDREF} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95°C

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Power Supply Noise Rejection [7]	PSR	25 kHz sinusoidal noise	-	–96	-	dBc
		100 kHz sinusoidal noise	-	–97	-	
		500 kHz sinusoidal noise	-	–93	-	
		1 MHz sinusoidal noise	-	–93	-	
Output-to-Output Crosstalk [8]	$XTALK_{OUT}$	Differential outputs, same format	-	–95	-	dBc
Input-to-Output Crosstalk [9]	$XTALK_{IN}$	Differential input and output, same format	-	–90	-	dBc

1. Q dividers support output frequencies within the specified range equal to fVCO/Q where Q is an integer.
2. NA, NB MultiSynths support any output frequency within the specified range.
3. SYNC outputs are not included in this output-to-output skew specification.
4. “Align Qdivs to VCXO buffered output(s)" must be selected on the "Output Skew Control" page of ClockBuilder Pro. When Q divider outputs are aligned to the VCXO buffered output the input-to-output-delay is no longer specified unless using zero-delay mode. Additionally, the delay variation from OSYNC de-asserted to output re-enabled is no longer specified.
5. Output voltage swing is dependent on frequency range. Scale all values by the Output Voltage Swing Scaling Factor (SF). Voltage swing is specified in mVpp_SE as shown below.



6. OUT16/17 have programmable slew rate limit capability when configured as SRL LVCMOS. This causes additional attenuation for higher frequency outputs. The Output Voltage Swing Scaling Factor (SF) for OUT16/OUT17 is shown below. It is recommended to use OUT0-15 for fOUT > 491.52 MHz.
7. Measured for a 122.88 MHz output frequency. 100 mVpp sinewave noise added to V_{DDO} = 3.3 V and noise spur amplitude measured.
8. Crosstalk spur measured with the victim running at 153.6 MHz and the aggressor at 156.25 MHz. Victim and aggressor are separated by two unused channels.
9. Crosstalk spur measured with the victim running at 153.6 MHz on OUT0 and the aggressor at 156.25 MHz on IN3.

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Table 14. HCSL Clock Output Specifications

V_{DD18} = 1.8 V ±5%, V_{DDA} = V_{DDREF} = 3.3 V ±5%; All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95°C. Low Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDREF} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95°C

Parameter	Symbol	Test Condition			Min	Typ	Max	Units
Output Frequency	f_{OUT}	Q Divider, Non PPS[1]			0.008	-	500	MHz
		Q Divider, PPS			0.5	-	1	Hz
		NA Divider, Non PPS[2]			0.008	-	500	MHz
		NA Divider, PPS			0.5	-	1	Hz
		NB Divider[2]			0.008	-	500	MHz
Duty Cycle	DC	f < 400 MHz			49.5	50	50.5	%
		400 MHz < f < 500 MHz			48	50	52	
Output-to-Output Skew	T_{SK}	Q divider outputs, same differential format[3]						ps
		Multisynth (NA or NB) outputs, same differential format, same Multisynth			-50	-	50	
		VCXO buffered outputs, same differential format						
		Q divider outputs, Differential SYSCLK to LVCMOS SYNC output			0	-	300	
		Q divider to VCXO buffered outputs, same differential format[4]			-1200	-	1200	
OUT-OUTb Skew	T_{SK_OUT}	Skew between positive and negative output pins.	VDDO=3.3V	HCSL Standard, 800 mVpp_se, int term	-	-	15	ps
				HCSL Standard, 800 mVpp_se, ext term	-	-	25	
				HCSL Fast, 800mV or 1200mV, ext term	-	-	10	
			VDDO=2.5V	HCSL Standard, 800 mVpp_se, int term	-	-	15	
				HCSL Standard, 800 mVpp_se, ext term	-	-	30	
				HCSL Fast, 800mV or 1200mV, ext term	-	-	20	
			VDDO=1.8V	HCSL Standard, 800 mVpp_se, int term	-	-	22	
				HCSL Standard, 800 mVpp_se, ext term	-	-	70	
				HCSL Fast, 800mV, ext term	-	-	36	
Output Voltage Swing[5]	V_{OUT}	VDDO=3.3V/2.5V/1.8V		HCSL Standard, 800 mVpp_se, int term	740*SF	810*SF	960*SF	mVpp_se
		VDDO=3.3V/2.5V/1.8V		HCSL Standard, 800 mVpp_se, ext term	730*SF	810*SF	960*SF	
		VDDO=3.3V/2.5V		HCSL Fast, 800 mVpp_se, ext term	730*SF	810*SF	960*SF	
		VDDO=3.3V/2.5V		HCSL Fast, 1200 mVpp_se, ext term	1100*SF	1175*SF	1260*SF	
Output Voltage Swing Scaling Factor (SF) Standard, 800mVpp_se, int term OUT0-17	SF	f < 10 MHz			1	1	1	SF
		10 MHz < f < 100 MHz			0.91	0.94	0.95	
		100 MHz < f < 200 MHz			0.89	0.91	0.93	
		200 MHz < f < 400 MHz			0.83	0.85	0.92	
		f > 400 MHz			0.74	0.78	0.89	
Output Voltage Swing Scaling Factor (SF) Standard, 800mVpp_se, ext term OUT0-17	SF	f < 10 MHz			1	1	1	SF
		10 MHz < f < 100 MHz			0.97	0.96	0.97	
		100 < f < 200 MHz			0.94	0.93	0.95	
		200 MHz < f < 400 MHz			0.91	0.90	0.88	
		f > 400 MHz			0.68	0.71	0.75	

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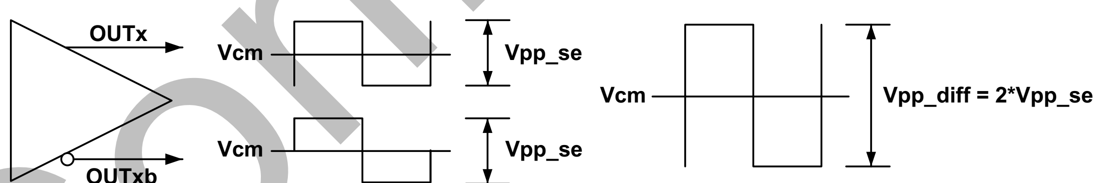
Table 14. HCSL Clock Output Specifications (Continued)

V_{DD18} = 1.8 V ±5%, V_{DDA} = V_{DDREF} = 3.3 V ±5%; All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95°C. Low Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDREF} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95°C

Parameter	Symbol	Test Condition		Min	Typ	Max	Units
Output Voltage Swing Scaling Factor (SF) Fast, 800 or 1200mVpp_se, ext term OUT0-17	SF	f < 10 MHz		1	1	1	SF
		10 MHz < f < 100 MHz		0.98	0.99	0.99	
		100 < f < 200 MHz		0.94	0.94	0.96	
		200 MHz < f < 400 MHz		0.94	0.95	0.97	
		f > 400 MHz		0.89	0.92	0.95	
Common Mode Voltage	V_{CM}	VDDO=3.3V/2.5V/1.8V	HCSL 800 mVpp_se	0.35	0.425	0.52	V
		VDDO=3.3V/2.5V	HCSL 1200 mVpp_se	0.55	0.6	0.68	
Rise and Fall Times (20% to 80%) OUT0 - 15	t_r/t_f	VDDO=3.3V/2.5V/1.8V	HCSL Fast, 800 or 1200 mVpp_se, ext term	-	270	360	ps
		VDDO=3.3V/2.5V/1.8V	HCSL Standard, 800mVpp_se, ext term	-	450	700	
		VDDO=3.3V/2.5V/1.8V	HCSL Standard, 800mVpp_se, int term	-	270	420	
Rise and Fall Times (20% to 80%) OUT16-17[6]	t_r/t_f	VDDO=3.3V/2.5V/1.8V	HCSL Fast, 800 or 1200 mVpp_se, ext term	-	285	400	ps
		VDDO=3.3V/2.5V/1.8V	HCSL Standard, 800mVpp_se, ext term	-	465	740	
		VDDO=3.3V/2.5V/1.8V	HCSL Standard, 800mVpp_se, int term		285	460	
Differential Output Impedance	Z_O	HCSL Standard Slew Rate, int term		-	100	-	Ω
		HCSL Standard Slew Rate, ext term		-	Hi-Z	-	
		HCSL Fast Slew Rate, ext term		-	200	-	
Output-to-Output Crosstalk[7]	$XTALK_{OUT}$	HCSL outputs, same format		-	-95	-	dBc
Input-to-Output Crosstalk[8]	$XTALK_{IN}$	HCSL input and output, same format		-	-90	-	dBc

1. Q dividers support output frequencies within the specified range equal to fVCO/Q where Q is an integer.
2. NA, NB MultiSynths support any output frequency within the specified range.
3. SYNC outputs are not included in this output-to-output skew specification.
4. "Align Qdivs to VCXO buffered output(s)" must be selected on the "Output Skew Control" page of CBPro. When Q divider outputs are aligned to the VCXO buffered output the input-to-output-delay is no longer specified unless using zero-delay mode.



5. Output voltage swing is dependent on frequency range, HCSL slew rate and HCSL termination settings. Scale all voltage swing values by the scaling factor (SF). Voltage swing is specified in mVpp_SE as shown below.
6. OUT16/17 have programmable slew rate limit capability when configured as LVCMOS. This causes additional attenuation for higher frequency outputs. The Output Voltage Swing Scaling Factor (SF) for OUT16/OUT17 is shown below. It is recommended to use OUT0-15 for fOUT > 491.52 MHz.
7. Crosstalk spur measured with the victim running at 153.6 MHz and the aggressor at 156.25 MHz. Victim and aggressor are separated by two unused channels.
8. Crosstalk spur measured with the victim running at 153.6 MHz on OUT0 and the aggressor at 156.25 MHz on IN3.

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Table 15. LVCMOS Clock Output Specifications

VDD18 = 1.8 V ±5%, V_{DDA} = V_{DDREF} = 3.3 V ±5%; All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C.
Low Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDREF} = V_{DDA} = V_{DDO} = 1.8 V ±5%, TA = –40 to 95 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Output Frequency	f_{OUT}	Q Divider, Non PPS [1]	0.008	—	250	MHz
		Q Divider, PPS	0.5	—	1	Hz
		NA Divider, Non PPS [2]	0.008	—	250	MHz
		NA Divider, PPS	0.5	—	1	Hz
		NB Divider [2]	0.008	—	250	MHz
Duty Cycle	DC	f < 100 MHz	49.5	—	50.5	%
		100 MHz < f < 250 MHz	45	—	55	
Output Voltage High [3]	V_{OH}	VDDO= 3.3 V/2.5 V/1.8 V I_{OH}= –8/–6/–4 mA, I_{OL} = 8/6/4 mA	V_{DDO} x 0.85	—	—	V
Output Voltage Low [3]	V_{OL}		—	—	V_{DDO} x 0.15	V
Rise and Fall Times (20% to 80%)[4, 5, 6]	t_r/t_f	LVCMOS	0.35	0.8	1.35	ns
		SRL LVCMOS 4 ns rise/fall	3	4	6	
		SRL LVCMOS 6.5 ns rise/fall	4	6.5	10	
		SRL LVCMOS 13 ns rise/fall	7	13	24	
		SRL LVCMOS 25 ns rise/fall	13	25	42	

1. Q dividers support output frequencies within the specified range equal to fVCO/Q where Q is an integer.
2. NA, NB MultiSynths support any output frequency within the specified range.
3. VOL /VOH is measured at IOL /IOH as shown in the DC Test Configuration.
4. A 15-25Ω series termination resistor (RS) is recommended to help match the source impedance to a 50Ω PCB trace. A 5 pF capacitive load is assumed as shown in the AC Test Configuration.

5. Slew Rate Limited (SRL) LVCMOS format only available on OUT16/OUT17.
6. SRL LVCMOS format clocks are intended only for low frequency clock applications. Refer to the Si5518/12/10/08 Reference Manual for the maximum Fout supported for each slew rate selection.

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Table 16. VCNTRL Output Pin Specifications

$V_{DDREF} = V_{DDA}$ = 3.3 V ±5%, T_A = –40 to 95 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Output Voltage High	V_{OH}	V_{DDREF} = 3.3 V [1] R_{LOAD} > 20 kΩ	V_{DDREF} x 0.9	—	—	V
Output Voltage Low	V_{OL}		—	—	V_{DDREF} x 0.1	V

1. VCXO is not supported in Low-Power Mode.

Table 17. Output Status Pin Specifications

V_{DDIO} = 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A= –40 to 95 °C. Low-Power Mode: V_{DDIO} = 1.8 V ±5%

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Serial and Status Output Pins (GPIO, SDA/SDIO, SDO)						
Output Voltage High	V_{OH} [1]	I_{OH} = –2 mA	V_{DDIO} x 0.85	—	—	V
Output Voltage Low	V_{OL}	I_{OL} = 2 mA	—	—	V_{DDIO} x 0.15	V

1. The VOH specification does not apply to the open-drain SDA output when the serial interface is in I2C mode. VOL remains valid in all cases.

Table 18. Performance Characteristics

V_{DD18} = 1.8 V ±5%, $V_{DDA} = V_{DDREF}$ = 3.3 V ±5%; All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C. Low-Power Mode: $V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDREF} = V_{DDA} = V_{DDO}$ =1.8 V ±5%, T_A = –40 to 95 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Initial Start-Up Time	t_{START_XO}	Time from POR to when the device generates free-running clocks from NVM frequency plan	—	25	40	ms
	t_{START_XTAL}		—	120	270	
	t_{RDY}	POR to API ready	—	25	30	
PLL Lock Time	t_{ACQ_DSPLL} [1]	RFPLL, IN = 19.44 MHz, BW = 100 Hz, FLOL De-assert	—	230	350	ms
		RFPLL, IN = 19.44 MHz, BW = 100 Hz, LOL De-assert	—	1.3	1.6	s
		DSPLLA/B, IN = 156.25 MHz, BW = 3 Hz, FLOL De-assert	—	190	240	ms
		DSPLLA/B, IN = 156.25 MHz, BW = 3 Hz, LOL De-assert	—	1.3	1.6	s
	t_{ACQ_PPS} [2]	PPSPLL, IN = 1PPS, BW = 12.5 mHz, Coarse LOL De-assert	—	26	28	s
		PPSPLL, IN = 1PPS, BW = 12.5 mHz, Fine LOL De-assert	—	35	37	
		PPSPLL, IN = PP2S, BW = 12.5 mHz, Coarse LOL De-assert	—	53	56	
		PPSPLL, IN = PP2S, BW = 12.5 mHz, Fine LOL De-assert	—	69	72	
Output Delay Adjustment	t_{QDIV}	Range [3]	$-T_{VCO}$ x 127	—	$+T_{VCO}$ x 127	ps
		Resolution		T_{VCO}	—	
		Resolution - fine delay enabled		$T_{VCO}/4$	—	
Jitter Peaking	J_{PK}	All PLLs	—	—	0.1	dB
Max Phase Transient during Hitless Switch [4]	t_{SWITCH}		—	35	150	ps
Pull-in Range [5]	ω_P		—	±100	—	ppm

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Table 18. Performance Characteristics

V_{DD18} = 1.8 V ±5%, V_{DDA} = V_{DDREF} = 3.3 V ±5%; All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C. Low-Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDREF} = V_{DDA} = V_{DDO} =1.8 V ±5%, T_A = –40 to 95 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Input-to-Output Delay + Variation [6, 7]	$t_{IODELAY}$	DSPLLA in dual ref mode or RFPLL in single ref mode [8]	–400	—	400	ps
	t_{ZDELAY}	ZDM: 1PPS, PP2S	–200	—	200	
		ZDM: f_{IN} > 8 kHz	–100	—	100	
Input-to-Output Delay Variation [9]	$t_{VIODELAY}$	DSPLLA in single ref mode or DSPLLB	–500	—	500	
RMS Jitter Performance [10] 12 kHz to 20 MHz	J_{GEN_VCXO} [11]	491.52 MHz, Q div	—	43	65	fs
		156.25 MHz, NA or NB div	—	81	135	
	$J_{GEN\_VCXO\_BUFF\_OUT}$ [11]	122.88 MHz, buffer output	—	38	—	
	J_{GEN_XO} [12]	491.52 MHz, Q div	—	47	70	
		156.25 MHz, NA or NB div	—	91	135	
Phase Noise Performance [13]	PN_491.52M_VCXO_Q_Div [11]	10 Hz	—	–79	—	dBc/Hz
		100 Hz	—	–99	—	
		1 kHz	—	–124	—	
		10 kHz	—	–135	—	
		100 kHz	—	–141	—	
		800 kHz	—	–146	—	
		1 MHz	—	–146	—	
		10 MHz	—	–162	—	
		40 MHz	—	–164	—	
	PN_122.88M_VCXO_BUFF_OUT [11]	10 Hz	—	–92	—	dBc/Hz
		100 Hz	—	–108	—	
		1 kHz	—	–136	—	
		10 kHz	—	–153	—	
		100 kHz	—	–163	—	
		800 kHz	—	–167	—	
		1 MHz	—	–167	—	
		10 MHz	—	–167	—	
		40 MHz	—	–168	—	
	PN_491.52M_XO_Q_Div [12]	10 Hz	—	–79	—	dBc/Hz
		100 Hz	—	–107	—	
		1 kHz	—	–127	—	
		10 kHz	—	–135	—	
		100 kHz	—	–138	—	
		800 kHz	—	–145	—	
		1 MHz	—	–146	—	
		10 MHz	—	–161	—	
		40 MHz	—	–164	—	

1. FLOL de-asserts once frequency lock is achieved. LOL de-asserts once both frequency and phase lock are achieved. Refer to "3.13.2. Lock Acquisition Mode" on page 21 for more details on LOL thresholds.
2. PPSPLL lock time specified for frequency plans with a greatest common divisor of SYSCLK frequencies greater than or equal to 960 kHz. Coarse lock is declared once the PPSPLL has steered the output phase to within 500 ns of the input phase. Fine lock is declared when the output phase is within 30 ns of the input phase. For more details on PPSPLL lock times, see the "Si5518/12/10/08 Reference Manual".
3. Output delay adjustment range will vary depending on frequency plan. Output delay adjust range (ns) is displayed in the "Output Skew Control" step of the ClockBuilder Pro Wizard. FVCO range is 10.4 GHz–13 GHz.
4. Phase transient specification only applies to clock switches between two synchronous inputs to a DSPLL configured for a phase buildout clock switching mode in ClockBuilder Pro.
5. When using a VCXO reference, the pull-in range for RFPLL will be limited by the APR of the VCXO. For more information, please see the Si5518/12/10/08 Reference Manual".
6. Input-to-output delay is measured at the output driver with respect to the input after the output phase has achieved a steady state value. This spec excludes wander from the OCXO/TCXO.
7. IO delay requires clock switching to be configured for Phase Pull-in in ClockBuilder Pro. IO delay is not specified for Phase Buildout (hitless) clock switching mode.

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8. Input-to-output delay in these modes is only specified for outputs derived from Q dividers or the NA divider.
9. Only IO delay variation is specified for these DSPLL configurations. Absolute delay is dependent on frequency plan.
10. Added jitter and spurs due to crosstalk is frequency-plan-dependent and can be determined using the ClockBuilder Pro Spur Analysis tool.
11. Jitter generation conditions: VCXO = 122.88 MHz Rakon RVX1490U-V4104, fIN = 156.25 MHz, LVPECL output format, RF DSPLL BW = 40 Hz. VCXO buffer output jitter and phase noise specifications include the jitter and phase noise of the VCXO.
12. Jitter generation conditions: XO = 54 MHz TXC 7X54070001, fIN = 156.25 MHz, LVPECL output format, RF DSPLL BW = 40 Hz.
13. An SMA-100a low-noise signal generator is used as the input to the RF DSPLL for phase noise performance. Specified phase noise does not include phase noise of an oscillator (TCXO/OCXO) applied to the RFPLL.

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5. Standards Compliance

DSPLLA, DSPLLB, and PPSPLL can be configured to support the requirements of the ITU-T standards shown in the following table.

Table 19. Supported ITU-T Standards

ITU-T Standard	Options	Comment
G.8262	EEC Option 1	SDH. SyncE. Based on G.813 Option 1.
	EEC Option 2	SDH. SyncE. Based on G.812 Type IV.
G.8262.1	eEEC	Enhanced SyncE
G.8273.1	N/A	Grandmaster T-GM
G.8273.2	N/A	Supported with and without SyncE. T-TSC and T-BC.
G.8273.4	N/A	Assisted Partial Timing Support (APTS). T-TSC-A and T-TBC-A.

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6. Typical Operating Characteristics

The phase noise plots shown in Figure 16, "VCXO Configuration, fIN = 156.25 MHz, fOUT = 491.52 MHz," on page 49 and Figure 17, "VCXO Configuration, fIN = 156.25 MHz, fOUT = 156.25 MHz," on page 50 were taken under the following conditions: fIN =156.25 MHz, fOUT LVDS, RF DSPLL BW = 40 Hz, VCXO = 122.88 MHz Rakon RVX1490U-V4104, TA = 25 °C for VCXO.

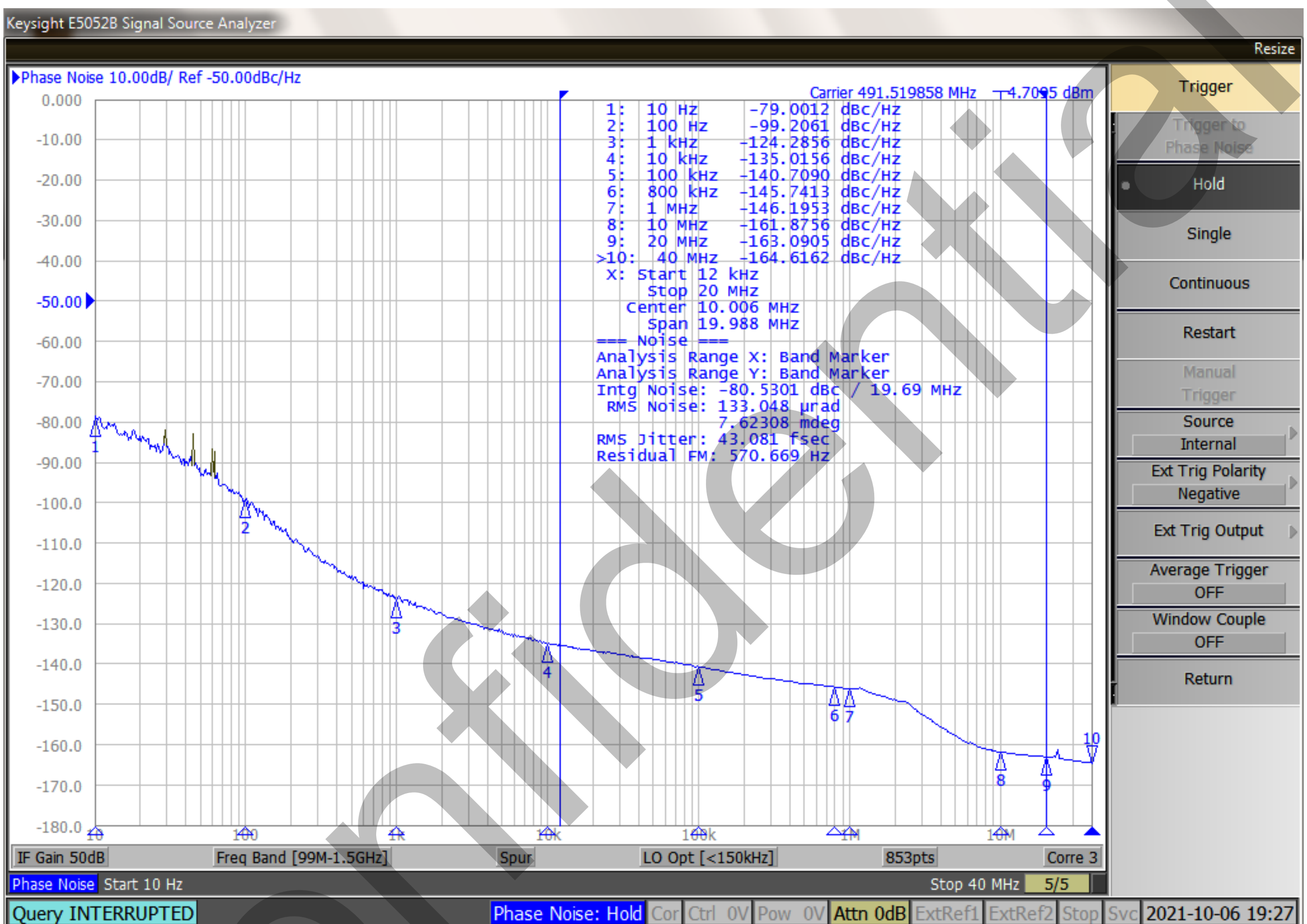

Figure 16. VCXO Configuration, f_{IN} = 156.25 MHz, f_{OUT} = 491.52 MHz

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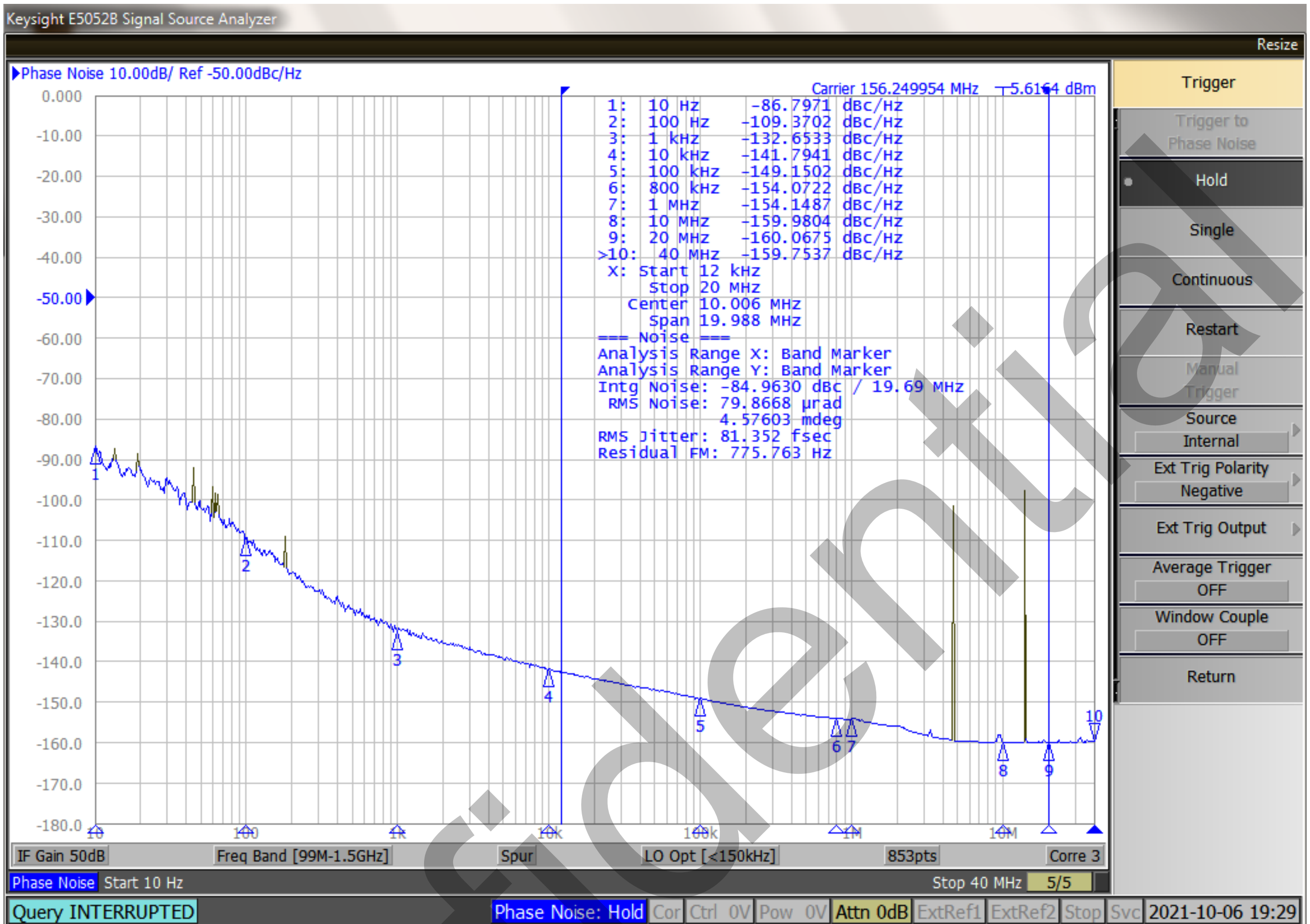

Figure 17. VCXO Configuration, f_{IN} = 156.25 MHz, f_{OUT} = 156.25 MHz

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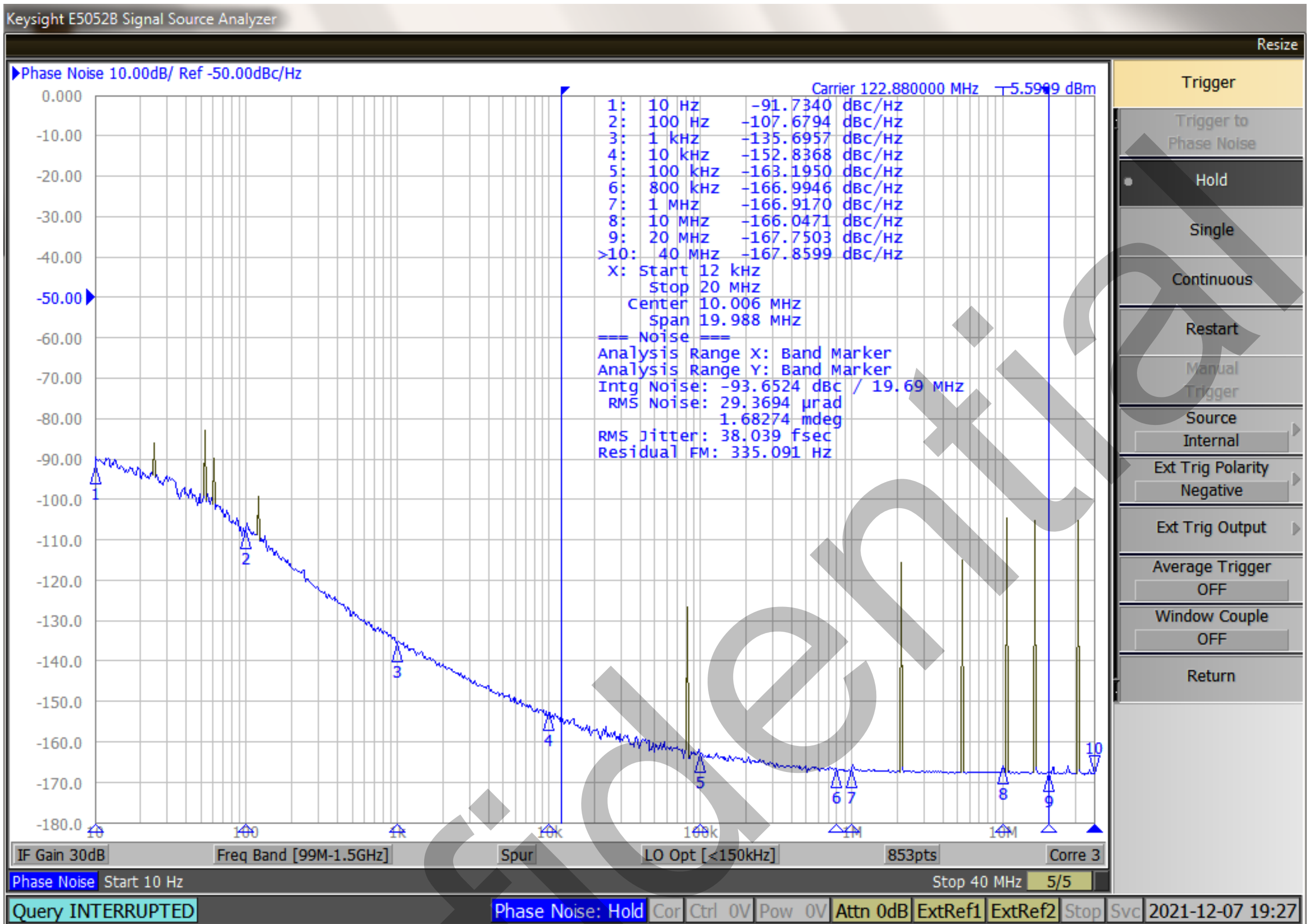

Figure 18. VCXO Buffer Output Configuration, f_{IN} = 156.25 MHz, f_{OUT} = 122.88 MHz

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The phase noise plots shown in Figure 19, "XO Configuration, fIN = 156.25 MHz, fOUT = 491.52 MHz," on page 52 and Figure 20, "XO Configuration, fIN = 156.25 MHz, fOUT = 156.25 MHz," on page 53 were taken under the following conditions: f_{IN} =156.25 MHz, f_{OUT} LVDS, RF DSPLL BW = 40 Hz, XO = 54 MHz TXC 7X54070001, T_A = 25 °C for XO.

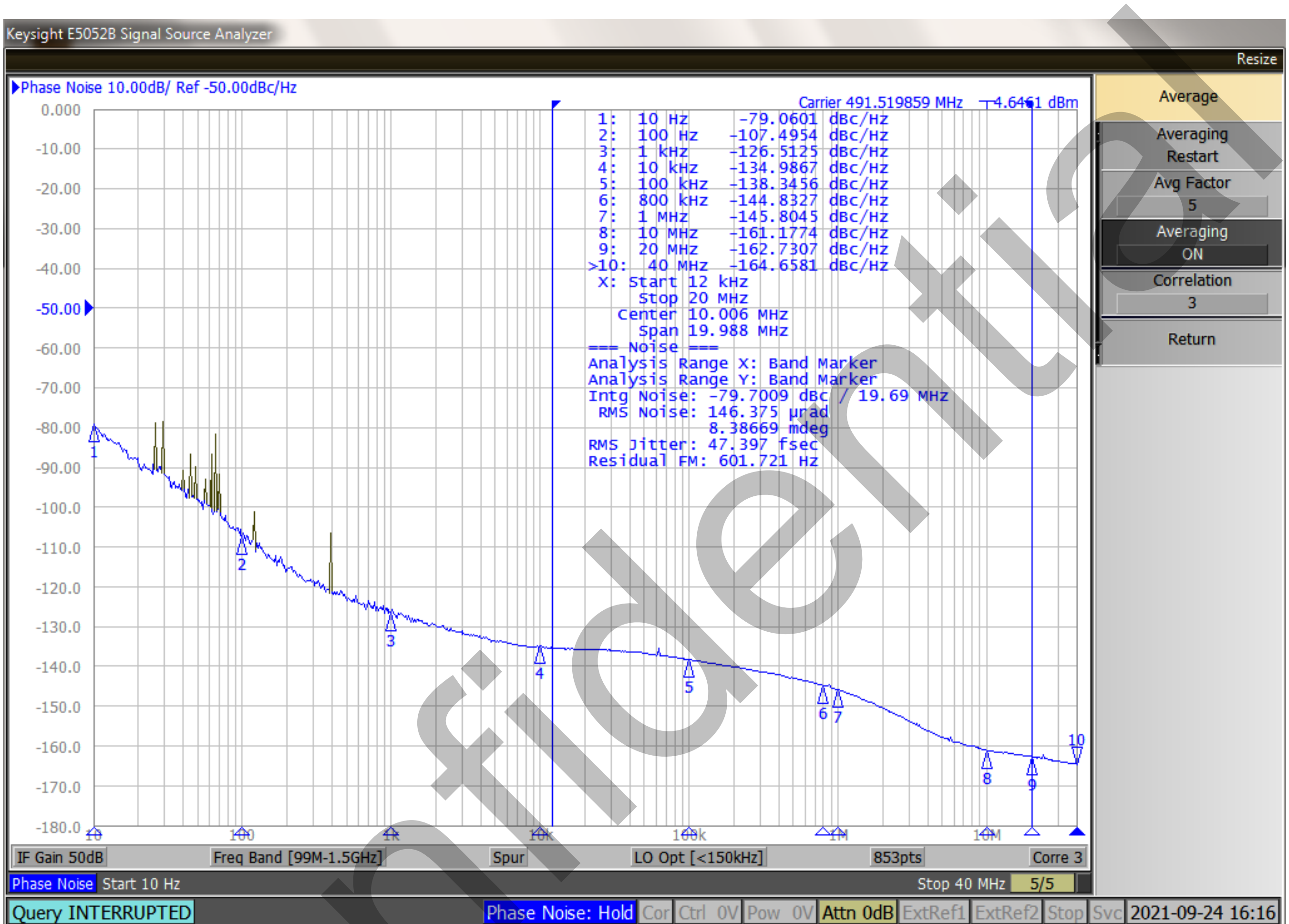

Figure 19. XO Configuration, f_{IN} = 156.25 MHz, f_{OUT} = 491.52 MHz

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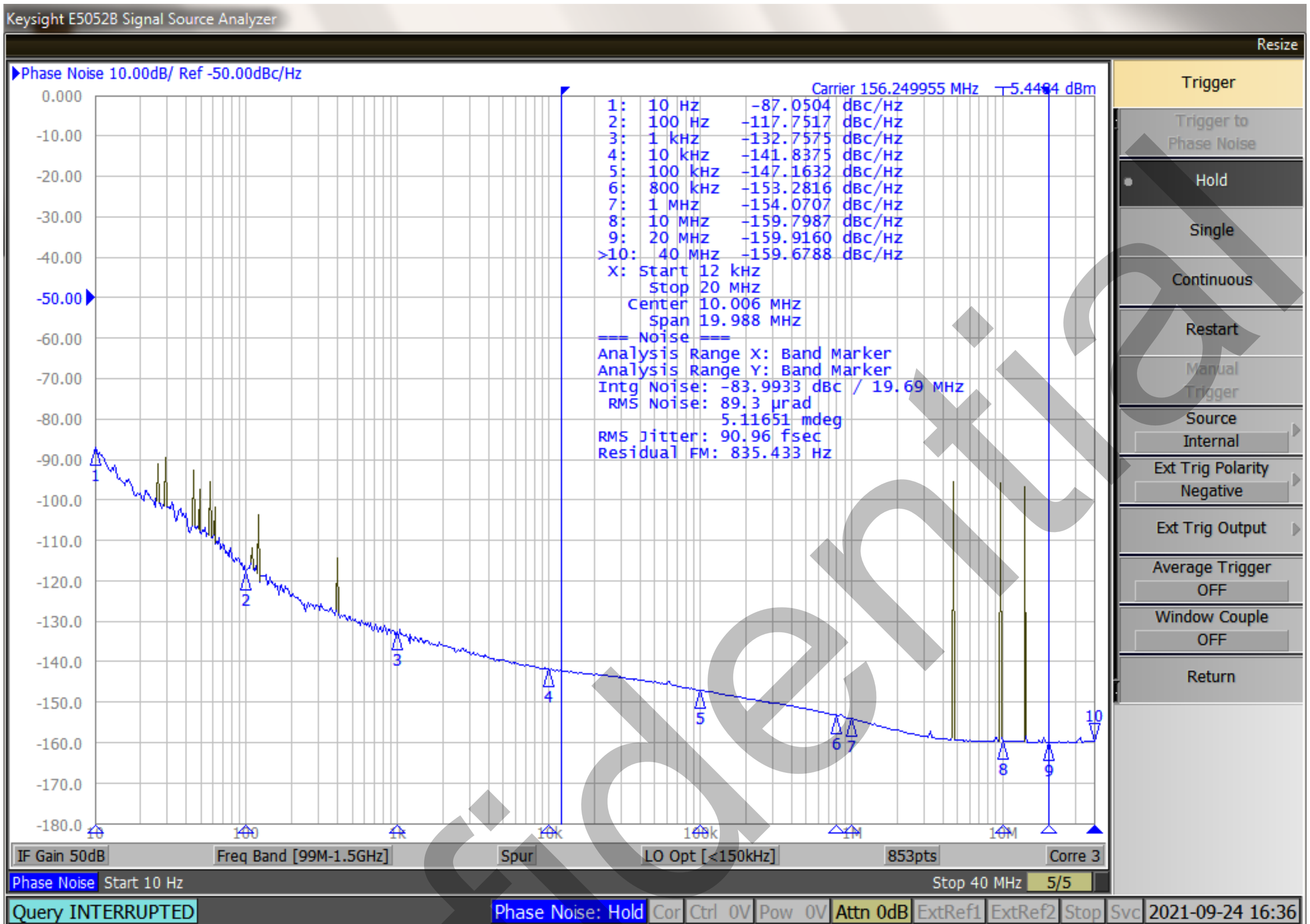

Figure 20. XO Configuration, f_{IN} = 156.25 MHz, f_{OUT} = 156.25 MHz

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7. Pin Descriptions

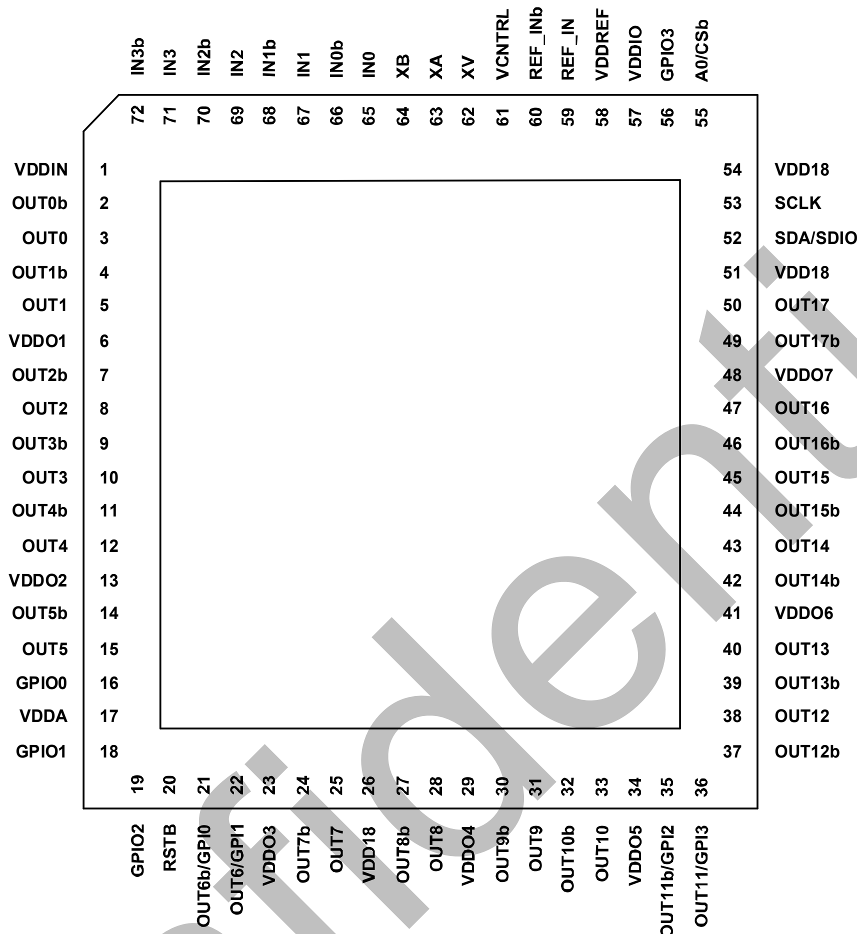

Figure 21. Pin Descriptions

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Table 20. Pin Descriptions

Pin Name	Pin Number	Pin Type [1]	Function
Inputs			
REF_IN	59	I	Input for low phase noise (XO or VCXO).
REF_INb	60		
XV	62	I	**XTAL and VCNTRL Shield** Connect this pin directly to the XTAL and VCNTRL capacitor ground pins. Do not ground the XV pin. XV should be isolated from the PCB ground plane. See the AN1293: Si55xx Schematic Design and Board Layout Guide for layout guidelines.
XA	63	I	**Crystal Input** Input pins for external crystal (XTAL). XA and XB pins can be left unconnected when not in use.
XB	64		
IN0	65	I	**Clock Inputs** IN0–IN3 accepts an input clock for synchronizing the device. They support both differential and single-ended clock signals. When operating in single-ended mode, inputs IN2 and IN3 can provide two SE inputs each for a total of six inputs. See the AN1293: Si55xx Schematic Design and Board Layout Guide and Si5518/12/10/08 Reference Manual for input termination options. These pins are high-impedance and must be terminated externally. IN0–IN3 can be disabled in ClockBuilder Pro and the pins left unconnected if unused.
IN0b	66		
IN1	67		
IN1b	68		
IN2	69		
IN2b	70		
IN3	71		
IN3b	72		
Outputs			
VCNTRL	61	O	**VCXO Control Voltage** Connect this pin directly to the VCXO control voltage input. Place a 0.01 µF capacitor as close to VCNTRL as possible, between the VCNTRL pin and XV to reduce noise. VCNTRL may be left unconnected when not using a VCXO reference.
OUT0b	2	O	**Output Clocks** The output clocks can be programmed as single-ended CMOS or differential LVDS, S-LVDS, CML, HCSL or ac-coupled LVPECL and support a programmable signal amplitude and common-mode voltage. Desired output signal format is configurable in ClockBuilder Pro. Termination recommendations are provided in the Si5518/12/10/08 Reference Manual. Unused outputs should be left unconnected.
OUT0	3		
OUT1b	4		
OUT1	5		
OUT2b	7		
OUT2	8		
OUT3b	9		
OUT3	10		
OUT4b	11		
OUT4	12		
OUT5b	14		
OUT5	15		
OUT6b/GPI0	21	I or O	**Output Clocks with Input Option** Output 6 can alternatively be assigned as two General Purpose Inputs (GPI0/GPI1) that can be programmed to have any of the input control functions listed in "3.11. GPIO Pins (General Purpose Input or Output)" on page 19. Regardless of whether Output 6 is functioning as a clock output or GPI, the power supply will be VDDO3.
OUT6b/GPI1	22		
OUT7b	24	O	**Output Clocks** The output clocks can be programmed as single-ended CMOS or differential LVDS, S-LVDS, CML, HCSL or ac-coupled LVPECL and support a programmable signal amplitude and common-mode voltage. Desired output signal format is configurable in ClockBuilder Pro. Termination recommendations are provided in the Si5518/12/10/08 Reference Manual. Unused outputs should be left unconnected.
OUT7	25		
OUT8b	27		
OUT8	28		
OUT9b	30		
OUT9	31		
OUT10b	32		
OUT10	33		

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Table 20. Pin Descriptions (Continued)

Pin Name	Pin Number	Pin Type [1]	Function
OUT11b/GPI2	35	I or O	**Output Clocks with Input Option** Output 11 can alternatively be assigned as two General Purpose Inputs (GPI2/GPI3) that can be programmed to have any of the input control functions listed in Table 2, “GPIO Pin Descriptions,” on page 19. Regardless of whether Output 11 is functioning as a clock output or GPI, the power supply will be VDDO5.
OUT11/GPI3	36		
OUT12b	37	O	**Output Clocks** The output clocks can be programmed as single-ended CMOS or differential LVDS, S-LVDS, CML, HCSL or ac-coupled LVPECL and support a programmable signal amplitude and common-mode voltage. Desired output signal format is configurable in ClockBuilder Pro. Termination recommendations are provided in the Si5518/12/10/08 Reference Manual. Unused outputs should be left unconnected.
OUT12	38		
OUT13b	39		
OUT13	40		
OUT14b	42		
OUT14	43		
OUT15b	44		
OUT15	45		
OUT16b	46	O	**Output Clocks with Programmable CMOS Slew Rate** When outputs 16 and 17 are configured as CMOS outputs, they can also have the slew rate adjusted. Because of this they do not support a glitchless pulsed SYSREF mode. Continuous SYSREF mode is supported.
OUT16	47		
OUT17b	49		
OUT17	50		
Serial Interface			
SDA/SDIO	52	I/O	**Serial Data Interface** This is the bidirectional data pin (SDA) for the I^{2}C mode, or the bidirectional data pin (SDIO) in the 3-wire SPI mode, or the input data pin (SDI) in the 4-wire SPI mode. When in I^{2}C mode, this pin must be pulled-up using an external resistor of at least 1 kΩ. No pull-up resistor is needed when in SPI mode.
SCLK	53	I	**Serial Clock Input** This pin functions as the serial clock input for both I^{2}C and SPI modes. When in I^{2}C mode, this pin must be pulled-up using an external resistor of at least 1 kΩ. No pull-up resistor is needed when in SPI mode.
A0/CSb	55	I	**Address Select 0/Chip Select** This pin functions as the hardware controlled lsb of the device address (A0) in I^{2}C mode. In SPI mode, this pin functions as the chip select input (active low). This pin is internally pulled-up and can be left floating if unused.
GPIO3 (A1/SDO)	56	O	**Address Select 1/ Serial Data Output/GPIO3** This input pin operates as the hardware controlled next to lsb portion of the device address (A1) in I^{2}C mode. In 4-wire SPI mode this pin operates as the serial data output (SDO). In 3-wire SPI mode this pin can function as an additional GPIO pin (GPIO3).
Control/Status			
GPIO0	16	I or O	**Programmable General Purpose Input or Outputs** These pins can be programmed to the functions defined in Table 2, “GPIO Pin Descriptions,” on page 19.
GPIO1	18		
GPIO2	19		
RSTb	20	I	**Reset Pin** This pin functions as an active-low reset input and is used to generate a device reset when held low for at least the specified Minimum Pulse Width. This resets the device back to a known state and reloads the NVM frequency plan and application. All clocks will stop while the RSTb pin is asserted. If there is no frequency plan in NVM, the reset pin will return the device to the bootloader state in which it is waiting for the frequency plan and application to be downloaded by the host controller. This pin accepts a CMOS input and is internally pulled up with a ~20 kΩ resistor to VDDIO. VDDA and VDD18 must be powered up and stable before releasing RSTb. RSTb must not be toggled faster than the maximum update rate (fUR) specification. Please refer to AN1293: Si55xx Schematic Design and Board Layout Guidelines for more details on RSTb pin circuitry.
Power			
VDDIN	1	P	**Input Clock Supply Voltage** Supply voltage 3.3 V, 2.5 V or 1.8 V for the input clock buffers.

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Table 20. Pin Descriptions (Continued)

Pin Name	Pin Number	Pin Type [1]	Function
VDDO1	6	P	**Output Clock Supply Voltage 1–7** Supply voltage 3.3 V, 2.5 V, or 1.8 V for outputs. Leave VDDO pins of unused output drivers unconnected. An alternate option is to connect the VDDO pin to a power supply and disable the output driver to minimize current consumption. A 0402 1 µF capacitor should be placed very near each of these pins. VDDO may not exceed VDDA. The banks of outputs are powered as follows: VDDO1 – OUT[0:3] VDDO2 – OUT[4:5] VDDO3 – OUT[6:7] VDDO4 – OUT[8:9] VDDO5 – OUT[10:11] VDDO6 – OUT[12:15] VDDO7 – OUT[16:17] Datasheet jitter performance requires all outputs in a given bank to operate at a single frequency.
VDDO2	13		
VDDO3	23		
VDDO4	29		
VDDO5	34		
VDDO6	41		
VDDO7	48		
VDDA	17	P	**Core Analog Supply Voltage** This core supply can operate from a 3.3 V or 1.8 V power supply for Low-Power Mode. Note that all other supply voltages must be equal or lower voltage than the VDDA pin; so, in Low-Power Mode, no other supply can exceed 1.8 V. A 0402 1 µF capacitor should be placed very near each of these pins.
VDD18	26	P	**Core Supply Voltage 1.8 V** The device core operates from a 1.8 V supply. A 0402 1 µF capacitor should be placed very near each of these pins.
VDD18	51	P	
VDD18	54	P	
VDDIO	57	P	**Control, Status IO Clock Supply Voltage** Supply voltage 3.3 V, 2.5 V, or 1.8 V for the serial interface, Control, and Status inputs and outputs.
VDDREF	58	P	**Reference Supply Voltage** Supply voltage of 3.3 V or 1.8 V supported for the reference. For best performance, VDDREF should be the same voltage as the VDD_XO or VDD_VCXO.
GND PAD	Package Bottom	P	**Exposed Die Attach Pad** The exposed die attach pad (ePAD) on the bottom of the package must be connected to electrical ground.

1. I = Input, O = Output, P = Power

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8. Package Outline

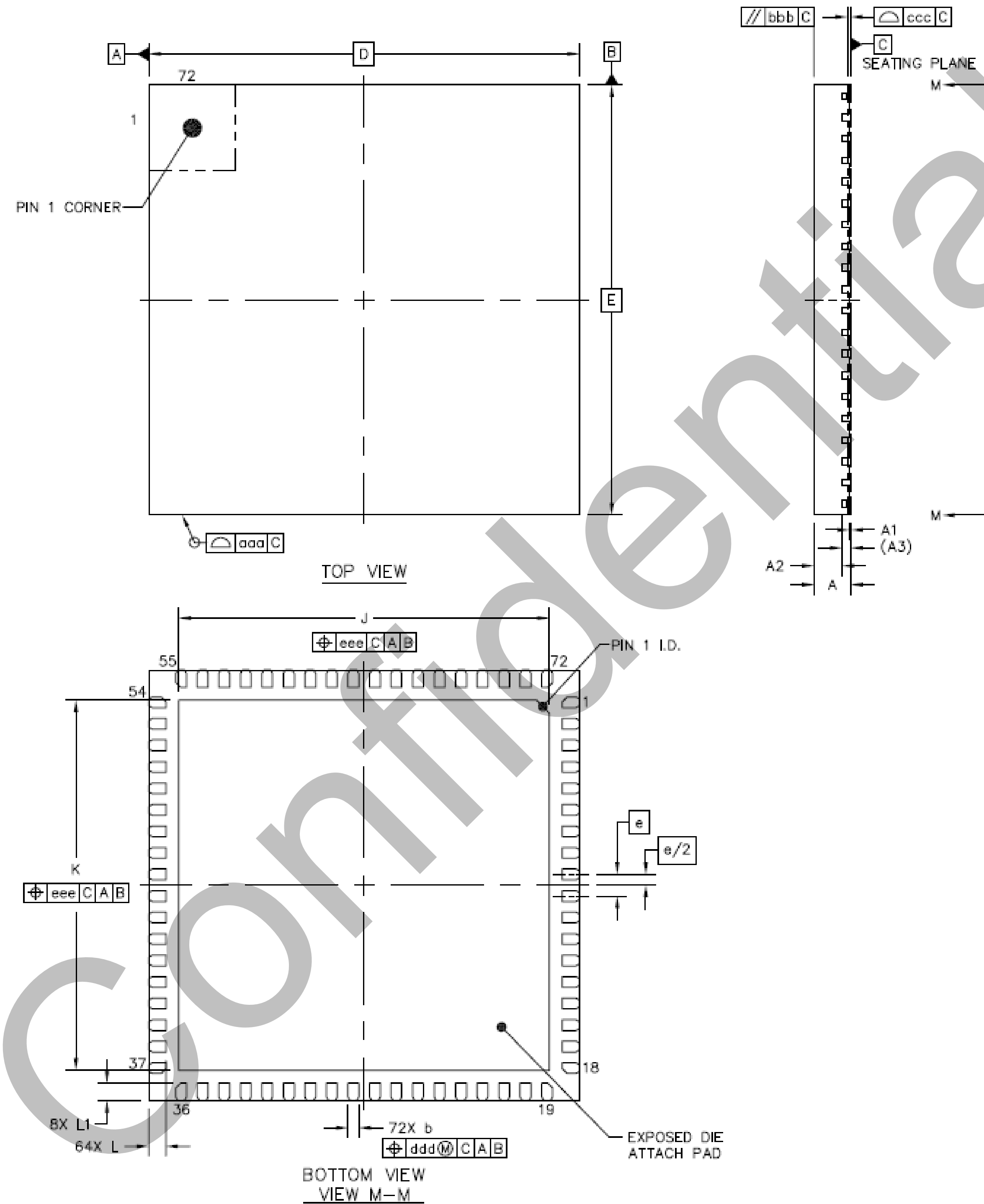

Figure 22. 72-QFN Package Diagram

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Table 21. Package Dimensions [1, 2, 3]

		Symbol	Min	Typ	Max
Total Thickness		A	0.8	0.85	0.9
Stand Off		A1	0	0.035	0.05
Mold Thickness		A2	–	0.65	–
L/F Thickness		A3		0.203 REF	
Lead Width		b	0.2	0.25	0.3
Body Size	X	D		10 BSC	
	Y	E		10 BSC	
Lead Pitch		e		0.5 BSC	
EP Size	X	J	8.5	8.6	8.7
	Y	K	8.5	8.6	8.7
Lead Length		L	0.35	0.4	0.45
		L1	0.3	0.4	0.45
Package Edge Tolerance		aaa		0.1	
Mold Flatness		bbb		0.1	
Coplanarity		ccc		0.08	
Lead Offset		ddd		0.1	
Exposed Pad Offset		eee		0.1	
Weight		N/A	—	0.35g	—

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Solid State Outline MO-220.

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9. PCB Land Pattern

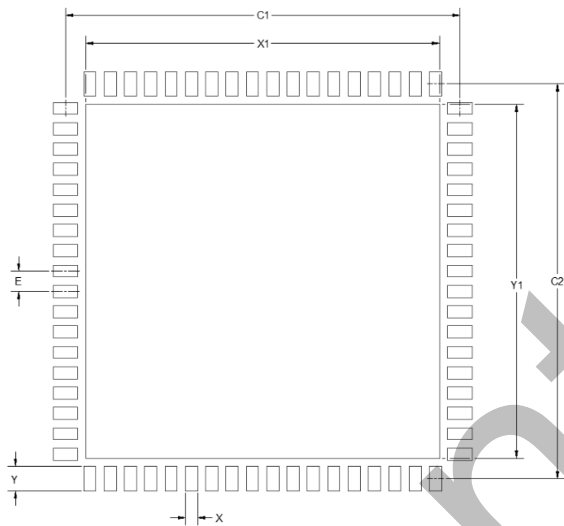

Figure 23. PCB Land Pattern

Table 22. PCB Land Pattern Dimensions

Dimension	mm	Notes
C1	9.70	**General** 1. These notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine tune their SMT process as required for their application and tooling. 2. All dimensions shown are in millimeters (mm). 3. This Land Pattern Design is based on the IPC-7351 guidelines. 4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm. **Solder Mask Design** 1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad. **Stencil Design** 1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release. 2. The stencil thickness should be 0.125 mm (5 mils). 3. The ratio of stencil aperture to land pad size should be 1:1 for all pads. 4. A 4x4 array of 1.45 mm square openings on a 2.00 mm pitch should be used for the center ground pad. **Card Assembly** 1. A No-Clean, Type-3 solder paste is recommended. 2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.
C2	9.70	
E	0.50	
X	0.30	
Y	0.60	
X1	8.70	
Y1	8.70	

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10. Top Marking

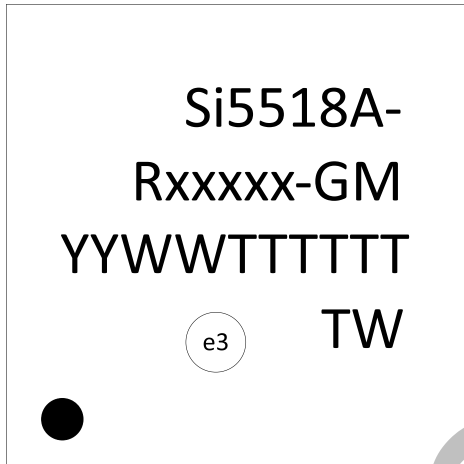

Figure 24. Si5518 Top Marking

Table 23. Top Marking Explanation

Line	Characters	Description
1	Si5518A-	Base part number and Device Grade: A = Device Grade. (Refer to "2. Ordering Guide" on page 4 for latest device grade information).
2	Rxxxxx-GM	R = Product revision. (Refer to Ordering Guide for latest revision). xxxxx = Customer specific NVM sequence number. Optional NVM code assigned for custom, factory pre-programmed devices. Characters are not included for standard, factory default configured devices. See Ordering Guide for more information. -GM = Package (QFN) and temperature range (–40 to +95°C)
3	YYWWTTTTTT	YYWW = Characters correspond to the year (YY) and work week (WW) of package assembly. TTTTTT = Manufacturing trace code.
4	Circle w/ 0.6 mm (72-QFN) diameter	Pin 1 indicator; left-justified
	e3 TW	Pb-free symbol; Center-Justified TW = Taiwan; Country of Origin (ISO Abbreviation)

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11. Revision History

Revision	Date	Description
B	November 8, 2023	Create version with CONFIDENTIAL watermark
A	November 1, 2023	Minor updates to datasheet including figures and tables each being separately sequential numbering: Datasheet Page 1 - Key Points • Replaced G.8273.1 (T-GM) with PRTC (T-GM) to more accurate reflect ITU standards. Section 1. Feature List • Changed last bullet of RFPLL (RF DSPLL) text to correct typos: - Selectable jitter attenuation bandwidth: 10 Hz to 400Hz, 10 Hz to 400Hz Dual Reference JA. Section 2. Ordering Guide • Note 7 - Changed Xilinx to AMD. Section 3.3. Inputs • Figure 6. Input structure block diagram - Added PHMON to Input Monitors Section 3.5.3. Slew Rate Limited (SRL) LVCMOS Output • Added last paragraph to incorporate information found in other application notes, Reference Manuals and support documents. Section 3.12 Device Initialization and Reset • Clarified section by added new sentence "All clocks will stop during a hard reset" after sentence "A hard reset is initiated using RSTb pin or through the Device API RESTART command." And referenced "A hard reset is initiated using RSTb pin or through the Device API RESTART command." Referenced the Si5518/12/10/08 Reference Manual as well as AN1360 for more information. Section 3.18 NVM Programming: • Fixed typos Section 3.19. Application Programming Interface: • Clarified that the secondary serial port only supports SPI 3-wire. Section 3.21 Power Supplies: • Referenced AN1293 Si55xx Schematic Design and Board Layout Guide instead of Si55xx Reference Manual Section 3.21.2 Power Supply Ramp Rate: • Referenced Table 8 for supply voltage ramp rate. Section 3.21.3 Low Power Mode: • Added statement in text as a reminder to customers that NVM programming is not possible in low-power-mode as VDDA must be at 3.3V. Table 8 DC Characteristics: • Core Supply Current (VDD18 + VDDA) Parameter - I_{DD18} Symbol Test Condition - Added note 2 to Si5518[1,2] - Deleted Si5518 Low Power Mode[2] row - I_{DDA} Symbol Test Condition - Added note 2 to Si5518[1,2] - Deleted Si5518 Low Power Mode[2] row • Periphery Supply Current Parameter - IDDIN + IDDIO Symbol Test Condition - Added note 2 to Si5518[1,2] - Deleted Si5518 Low Power Mode[2] row - IDDREF Symbol Test Condition - Added note 2 to Si55181,2 - Deleted Si5518 Low Power Mode[2] row. Table 13. Differential Clock Output Specifications: • Parameter OUT-OUTb Skew, Symbol TSK_OUT - Clarified this parameter is skew between positive and negative output pins. - Expanded Test Conditions portion of table which allowed some specs to be tightened without changing the overall spec Min/Max.

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Revision	Date	Description
A	November 1, 2023	• Removed HCSL line items from the following Table 13 Parameter sections and added new HCSL Output Table 14. - Parameter Output Voltage Swing[5], Symbol VOUT. - Parameter Common Mode Voltage, Symbol VCM. - Parameter Differential Output Impedance, Symbol Z_0. • Expanded table for Parameter Rise and Fall Times (20% to 80%) - Added Parameter Rise and Fall Times (20% to 80%) OUT0 - 15, Symbol t_r/t_f - Removed HCSL line items from the following Table 13 Parameter sections and added new HCSL Output Table 14. - Added Parameter Rise and Fall Times (20% to 80%) OUT16 - 17[6], Symbol t_r/t_f - Outputs 16 and 17 have programmable CMOS Slew Rate so spec tables reflect the Typ and Max for those output types. • Power Supply Noise Rejection[7] - Changed note from note 8 to note 7. • Output-to-Output Crosstalk[8] - Changed note from note 9 to note 8. • Input-to-Output Crosstalk[9] - Changed note from note 10 to note 9. • Note 6 - Removed Note 6 - Removed HCSL line items from Table 13 and added new HCSL Output Table 14. - Renumbered remaining notes. Table 14. HCSL Clock Output Specifications: • Added new Table 14 for HCSL Clock Output Specifications and removed HCSL line items from Table 13. - Separating HCSL outputs into its own table allows the output specifications to be more accurately defined. - Output Voltage Swing5 - Maximum specification changed to 960*SF for: - HCSL Standard, 800mVpp_se for both internal termination and external termination - HCSL Fast, 800mVpp_se external termination Table 15. LVCMOS Clock Output Specifications: • Added Note 6 to Parameter Rise and Fall Time (20% to 80%) [4,5,6] • Added new Note 6 to the Notes section, to cover SRL outputs. Table 17. Performance Characteristics: • Added statement to Note 6 to clarify - "after the output phase has achieved a steady state value." • Updated Note 10 to clarify based on new ClockBuilder Pro Spur Analysis tool which helps customers analyze added jitter and spurs due to cross talk. Table 19. Pin Descriptions: • Pin Name: RSTb, Pin: 20, Pin Type: I - Added addition text on RSTb operation incorporating information found in other application notes, Reference Manuals and other Si5518 support documents. • Pin Name: XV pin 62 and Input clock pins 65 through 72. - Reference AN1293 Si55xx Schematic Design and Board Layout Guide instead of Si5518/12/10/08 Reference Manual. Table 22. Top Marketing Explanation: • Line: 2, Characters: Rxxxxx-GM - Fixed typo on temperature range from -40 to +85C to 40 to +95C.
V1.0	July 2022	Initial release.

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DATA SHEET

Si5403, Si5402, and Si5401: NetSync™ Network Synchronizer Clock for 5G, SyncE, and IEEE 1588 Applications

The Si540x family of NetSync™ Network Synchronizer clocks utilizes Skyworks market-leading, fifth-generation DSPLL® and MultiSyth™ technologies. The Si540x device family consists of the Si5403, which has four PLLs, two MultiSyth any-frequency dividers, and 18 outputs, the Si5402 has four PLLs and two MultiSyths with 14 outputs, and the Si5401 completes the device family with three PLLs, one MultiSyth, and 10 outputs.

This feature-rich family of devices does not require external loop filters and has internal voltage supply regulation that reduce susceptibility to supply noise. Additional features include low transient hitless switching, low-power mode, and a full suite of status monitors.

NetSync clocks offer Synchronous Ethernet (SyncE)-compliant wander filtering and software adjustment of output frequency and phase for IEEE 1588 applications while offering ultra-low jitter output clocks, which eliminates the need for a follow-on jitter attenuator device.

For IEEE 1588 Precision Time Protocol (PTP) applications, the Si540x devices are available with Skyworks' AccuTime™ software to provide a full IEEE 1588-2008 compliant solution including operation in full timing support (FTS), partial timing support (PTS), and assisted partial timing support (APTS). Alternatively, the IEEE 1588-ready hardware features of the Si540x can be coupled with existing or third-party software to provide a complete solution.

This unique combination of features offers savings in system costs, PCB real estate, and power consumption, which makes them an ideal choice for today's complex equipment.

Applications

- Core, metro and edge switches and routers
- 5G BBUs
- 5G O-RAN
  - Central unit (O-CU)
  - Distributed unit (O-DU)
  - Front-haul gateway switches (FHGWS)
- IEEE 1588 grandmasters, boundary clocks and slaves
- SmartNICs

Key Points

- Ultra high-performance network synchronizer for wireline applications
- SyncE, SONET, and SDH
- Utilizes fifth-generation DSPLL® and MultiSynth™ technologies
- Optional AccuTime™ IEEE 1588 software
- Integer output frequencies up to 1.2288 GHz
- Fractional output frequencies up to 650 MHz
- Programmable delay at each output
- Ultra-low jitter 51 fs RMS typ
- Low-Power Mode
- Supports IEEE1588 with DCO adjustable at 1ppt resolution
- Locks to 1PPS and PP2S
- Full suite of status monitors
- Supports ITU-T G.8273.2 (T-TSC, T-BC), ITU-T G.8273.4 (T-BC-P, T-BC-A, T-TSC-P, T-TSC-A), G.8262 (EEC Options 1 and 2), and G.8262.1 (eEEC), PRTC (T-GM)
- AccuTime™ IEEE 1588 Software
  - Field tested proven with compliance reports available
  - O-RAN compatible
  - IEEE 1588 servo loop and protocol stack software runs on host processor

Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to *Skyworks Definition of Green™*, document number SQ04–0074.

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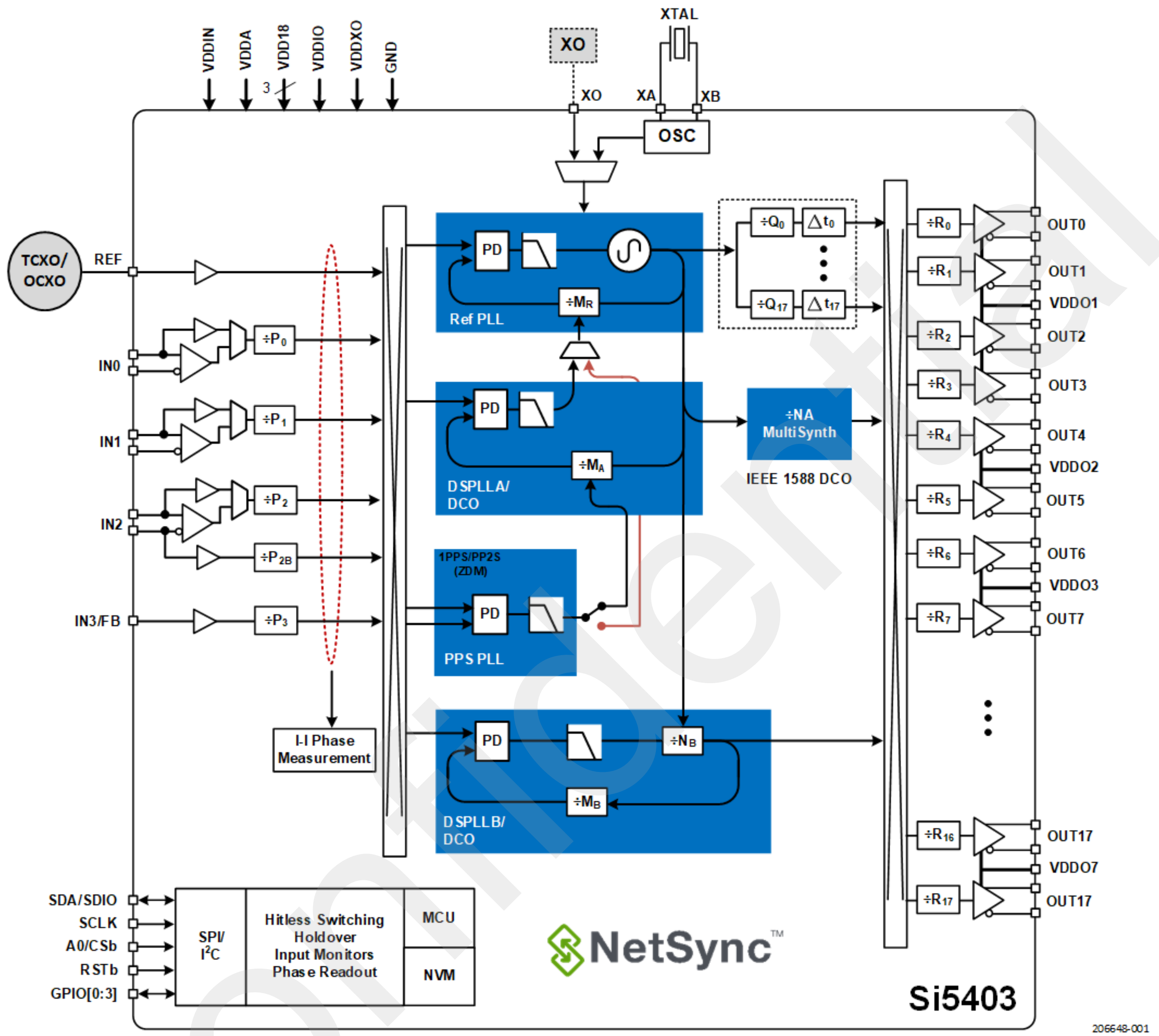

Figure 1. Si5403 Block Diagram

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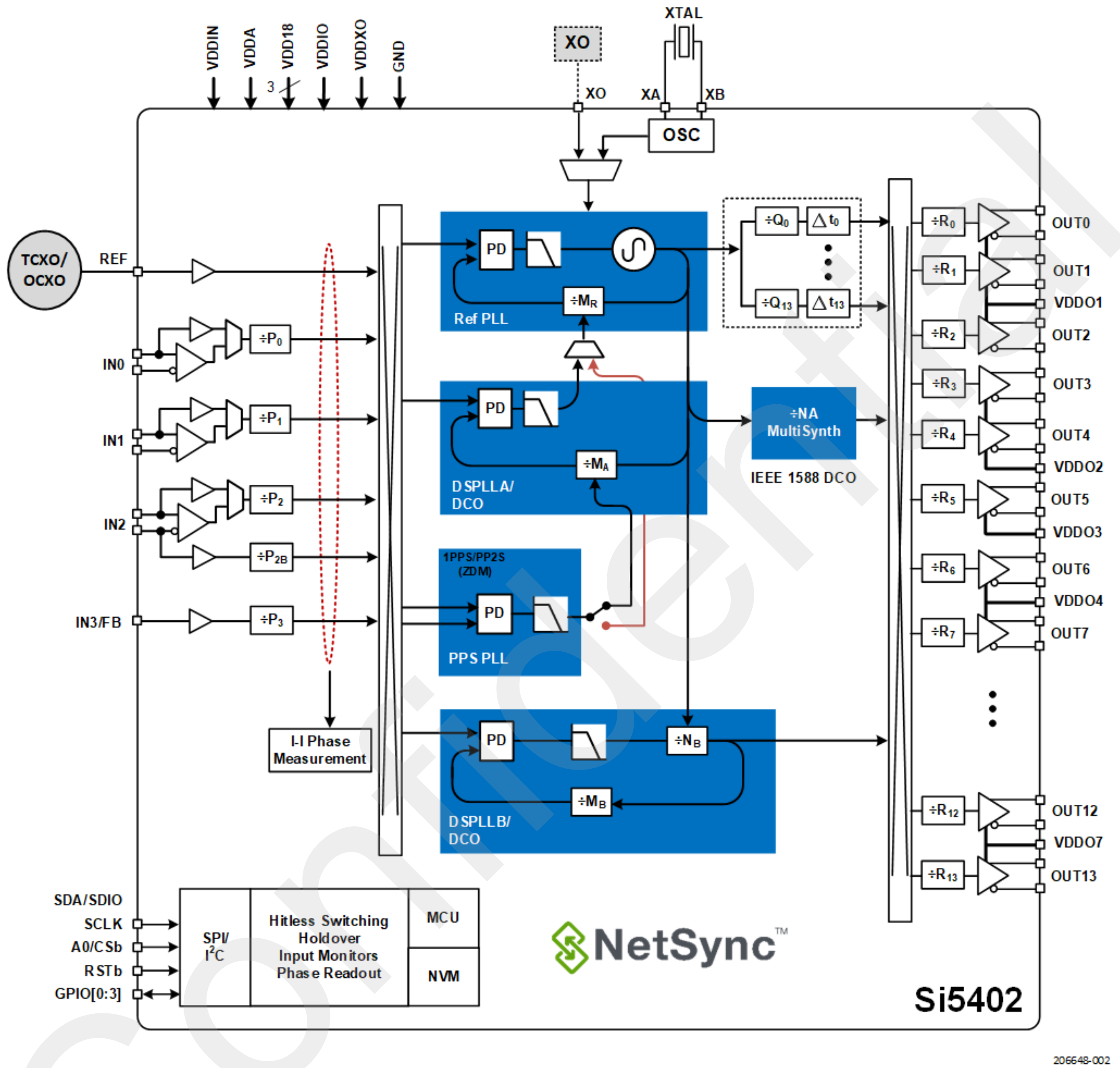

Figure 2. Si5402 Block Diagram

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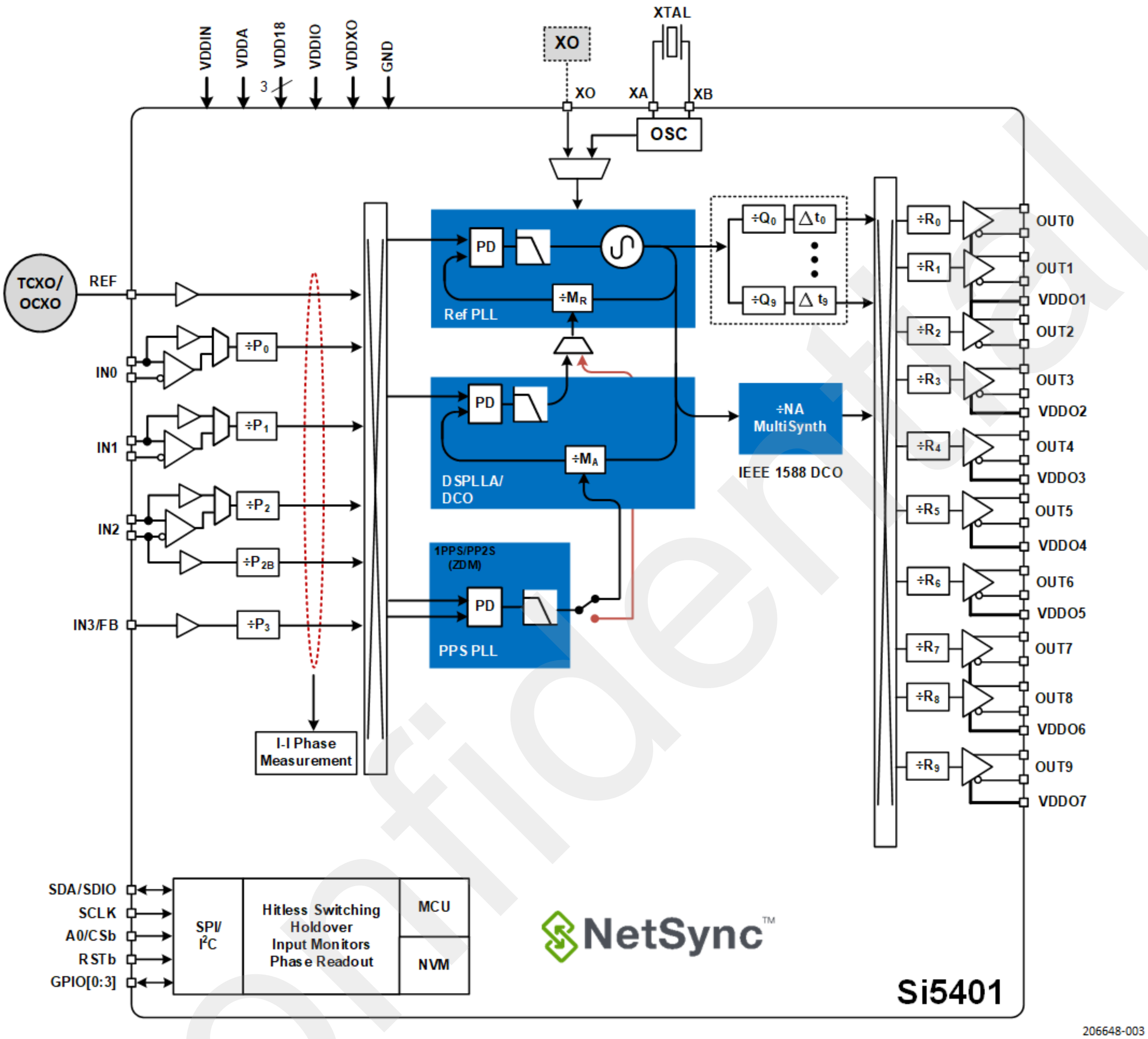

Figure 3. Si5401 Block Diagram

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1. Feature List

- REFPLL
  - Provides low-noise outputs using an external crystal or crystal oscillator
  - Provides output stability and holdover from external TCXO or OCXO
  - Excellent jitter performance:
    - 52 fs typ (12 kHz–20 MHz at 312.5 MHz)
  - Selectable jitter attenuation bandwidth: 10 Hz to 400Hz, 10 Hz to 400Hz dual reference JA
- DSPLL A, DSPLL B
  - Independent network synchronization DSPLLs
  - Supports ITU-T G.8273.2 (T-TSC, T-BC), ITU-T G.8273.4 (T-BC-P, T-BC-A, T-TSC-P, T-TSC-A), and PRTC (T-GM)
  - Programmable loop bandwidth: 1 mHz to 4 kHz
  - Automatic Free-Run, Holdover, and Locked modes
  - Input monitoring
  - Hitless input clock switching: automatic or manual with < 150 ps phase transient
- PPSPLL
  - Dedicated PLL for 1PPS and PP2S inputs
  - Targeted at IEEE 1588 grandmaster and APTS applications
  - Can modulate DSPLL A to support frequency lock to a higher frequency clock and simultaneous phase lock to a 1PPS/PP2S
  - Adaptive architecture allows rapid locking
  - Programmable loop bandwidth 1 mHz to 25 mHz
  - Programmable phase slope limiting (PSL) and phase pull-in rate (PPI)
- 18 Programmable Clock Outputs:
  - Integer Q dividers: PP2S/1PPS to 1.2288 GHz
  - Multisynth Fractional Dividers: PP2S/1PPS to 650 MHz
  - Output Delay Adjustment: ±10 ns
  - Output-output skew: ±50 ps
  - LVDS, S-LVDS, AC coupled LVPECL, LVCMOS, slew rate limited (SRL) LVCMOS, HCSL, CML
- Zero Delay Mode for all PLLs
- Three differential or five single-ended clock inputs:
  - Differential: 8 kHz to 1 GHz
  - CMOS: 1PPS, PP2S, 8 kHz to 250 MHz
- Status monitoring (LOS, OOF, PHMON, FLOL and PLOL)
- Automatically generates free-running clocks at power up
- Automatically locks to a valid clock input
- Automatic holdover mode
- Low-Power Mode
- Core voltage: 3.3 V, 1.8 V
- Output supply pins: 3.3 V, 2.5 V, 1.8 V
- Serial Interface: I2C or SPI (3 or 4-wire)
- In-circuit programmable with non-volatile memory
- ClockBuilder Pro™ software tool simplifies device configuration
- Package: 72-Lead QFN, 10 x 10 mm
- Extended temperature range:
  - –40 to +95 °C ambient
  - –40 to +105 °C board
- Pb-free, RoHS compliant

NOTE: Specifications given on this page are for reference only. Refer to 4. Electrical Specifications for device performance.

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2. Ordering Guide

Table 1. Ordering Guide

Ordering Part Number (OPN)[1,2]	# of PLLs	# of Outputs	Serial Interface	AccuTime™ IEEE 1588 Software Support[3]	Package	Temperature Range
Si5403A-Axxxxx-GM	4 (REFPLL, DSPLL A, DSPLL B and PPSPLL)	18	SPI 4-wire or 3-wire or I^{2}C	No	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient[4] –40 to 105 °C Board
Si5403B-Axxxxx-GM	4 (REFPLL, DSPLL A, DSPLL B and PPSPLL)	18	SPI 4-wire only or I^{2}C	Yes	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient[4] –40 to 105 °C Board
Si5403C-Axxxxx-GM[5]	4 (REFPLL, DSPLL A, DSPLL B and PPSPLL)	18	SPI 4-wire only or I^{2}C	Yes	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient[4] –40 to 105 °C Board
Si5403D-Axxxxx-GM[5]	4 (REFPLL, DSPLL A, DSPLL B and PPSPLL)	18	SPI 4-wire only or I^{2}C	Yes	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient[4] –40 to 105 °C Board
Si5403E-Axxxxx-GM[5]	4 (REFPLL, DSPLL A, DSPLL B and PPSPLL)	18	SPI 4-wire only or I^{2}C	Yes	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient[4] –40 to 105 °C Board
Si5403P-Axxxxx-GM[5]	4 (REFPLL, DSPLL A, DSPLL B and PPSPLL)	18	SPI 4-wire or 3-wire or I^{2}C	No	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient[4] –40 to 105 °C Board
Si5403Q-Axxxxx-GM[5]	4 (REFPLL, DSPLL A, DSPLL B and PPSPLL)	18	SPI 4-wire only or I^{2}C	Yes	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient[4] –40 to 105 °C Board
Si5402A-Axxxxx-GM[5]	4 (REFPLL, DSPLL A, DSPLL B and PPSPLL)	14	SPI 4-wire only or I^{2}C	No	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient[4] –40 to 105 °C Board
Si5402B-Axxxxx-GM[5]	4 (REFPLL, DSPLL A, DSPLL B and PPSPLL)	14	SPI 4-wire only or I^{2}C	Yes	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient[4] –40 to 105 °C Board
Si5402D-Axxxxx-GM[5]	4 (REFPLL, DSPLL A, DSPLL B and PPSPLL)	14	SPI 4-wire only or I^{2}C	Yes	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient[4] –40 to 105 °C Board
Si5402E-Axxxxx-GM[5]	4 (REFPLL, DSPLL A, DSPLL B and PPSPLL)	14	SPI 4-wire only or I^{2}C	Yes	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient[4] –40 to 105 °C Board
Si5402P-Axxxxx-GM[5]	4 (REFPLL, DSPLL A, DSPLL B and PPSPLL)	14	SPI 4-wire only or I^{2}C	No	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient[4] –40 to 105 °C Board
Si5402Q-Axxxxx-GM[5]	4 (REFPLL, DSPLL A, DSPLL B and PPSPLL)	14	SPI 4-wire only or I^{2}C	Yes	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient[4] –40 to 105 °C Board
Si5401A-Axxxxx-GM[5]	3 (REFPLL, DSPLL A and PPSPLL)	10	SPI 4-wire only or I^{2}C	No	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient[4] –40 to 105 °C Board
Si5401B-Axxxxx-GM[5]	3 (REFPLL, DSPLL A and PPSPLL)	10	SPI 4-wire only or I^{2}C	Yes	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient[4] –40 to 105 °C Board
Si5401D-Axxxxx-GM[5]	3 (REFPLL, DSPLL A and PPSPLL)	10	SPI 4-wire only or I^{2}C	Yes	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient[4] –40 to 105 °C Board
Si5401E-Axxxxx-GM[5]	3 (REFPLL, DSPLL A and PPSPLL)	10	SPI 4-wire only or I^{2}C	Yes	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient[4] –40 to 105 °C Board
Si5401P-Axxxxx-GM[5]	3 (REFPLL, DSPLL A and PPSPLL)	10	SPI 4-wire only or I^{2}C	No	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient[4] –40 to 105 °C Board
Si5401Q-Axxxxx-GM[5]	3 (REFPLL, DSPLL A and PPSPLL)	10	SPI 4-wire only or I^{2}C	Yes	72-Lead QFN 10 x 10 mm	–40 to 95 °C Ambient[4] –40 to 105 °C Board
Si540X-A-EVB	4 (REFPLL, DSPLL A, DSPLL B and PPSPLL)	18	—	No	Evaluation Board	
Si5403-A-FMC-EVB[6]	—	—	—	Yes	FPGA Mezzanine Card (FMC)	

1. Add an R at the end of the OPN to denote tape and reel ordering options.
2. Custom, factory preprogrammed devices are available as well as unconfigured base devices. See the figure below for 5-digit numerical sequence nomenclature.
3. AccuTime IEEE 1588 software is only supported on certain part grades. Use this table to determine which grades support AccuTime.
4. Ambient temperature of 95 °C may not be possible with all configurations. This is dependent on device configuration. Tj cannot exceed a maximum of 125 °C.
5. Grades C, D, E, P, and Q are reserved for special applications. See ClockBuilder Pro for details.
6. The Si5403-A-FMC-EVB ships with 10GBASE-SR SFP+ transceivers, optical cable along with the required software on an SD card. FMC requires a customer-provided AMD ZCU102, ZCU111, or ZCU216 FPGA eval board. FMC is only for AccuTime evaluation.

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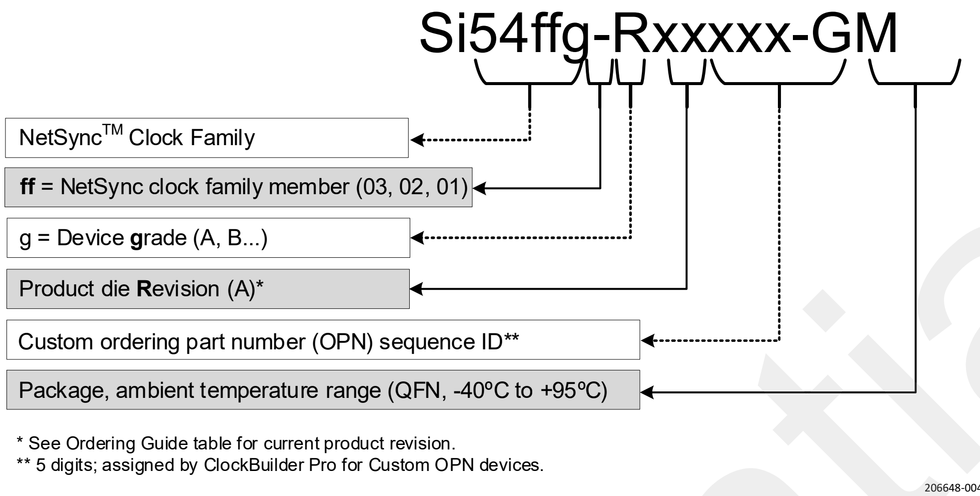

Figure 4. Ordering Guide

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3. Functional Description

The Si540x combines all the features expected of a network synchronizer, such as configurable wander filtering, hitless switching and longterm holdover, with ultra-low jitter clock outputs capable of directly driving high-speed SERDES for line speeds of 10, 25, 56 Gbps and faster. The Si540x achieves this by using a unique nested loop architecture in conjunction with two external reference oscillators. A crystal or crystal oscillator provides the inner loop reference, which controls the output jitter, while a TCXO or OCXO stabilizes the outer loop to support the low bandwidths typically needed in such applications as well as providing a longterm holdover function if no input sources are available. Two flexible PLLs, DSPLL A and B, utilize Skyworks fifth-generation DSPLL technology to provide any-frequency-to-any-frequency functionality.

There is an additional PPSPLL that provides dedicated locking to phase-aligned 1PPS or PP2S inputs for connection to devices such as a GNSS receiver. The PPSPLL and DSPLL A can be cascaded to combine frequency and phase sources.

There are four differential/single-ended inputs available to synchronize any of the phase-locked loops. IN2/IN2b can be configured as dual single-ended inputs in applications where more inputs are required. Input selection can be manual or automatically controlled using an internal state machine. Any of the 18 output clocks (OUT0 to OUT17) can be sourced from any of the PLLs using a flexible crosspoint connection.

Skyworks offers a comprehensive IEEE 1588 solution for applications in a "pizza box" architecture. It consists of three components: An IEEE 1588 protocol stack, a packet synchronizer servo algorithm (or "servo"), and the Si540x network synchronizer clock. The IEEE 1588 stack receives Ethernet packets from the host processor MAC, processes IEEE 1588 packets, and sends time stamp data to the IEEE 1588 servo algorithm implemented on the host. The servo statistically processes the time stamps and adjusts a 1588 system clock that runs the Time of Day (ToD) counter in the host.

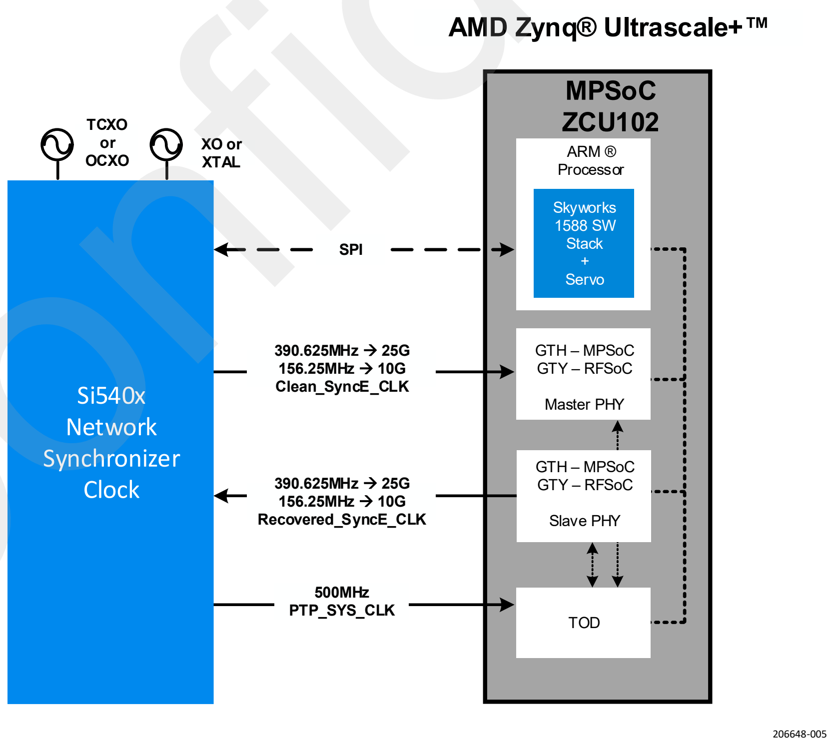

Figure 5. Si540x IEEE 1588 AMD Demo Platform Diagram

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3.1. Frequency Configuration

The frequency configuration of the DSPLL is programmable through the serial interface and can also be stored in non-volatile memory. The combination of input dividers (P), fractional frequency multiplication (M), integer output division (Q), fractional output division (N), and integer output division (R) allows the generation of virtually any output frequency on any of the outputs. All divider values for a specific frequency plan are easily determined using the ClockBuilder Pro utility.

3.2. DSPLL Loop Bandwidth, Initial Lock, and Fast Lock Settings

The DSPLL loop bandwidth determines the amount of input clock jitter and wander attenuation. Each DSPLL has a configurable loop bandwidth. The DSPLL will always remain stable with low peaking regardless of the loop bandwidth selection.

Each of the DSPLL's, and the PPSPLL, have configurable loop bandwidths. There are three configurations, each has a separate setting for the loop bandwidth:

- **Initial Lock Bandwidth**—The PLL uses this bandwidth when it exits the free-run mode and attempts to lock to a new input clock.
- **Loop Bandwidth**—This sets the bandwidth of the PLL once lock to an input is achieved.
- **Fastlock Bandwidth**—This sets the bandwidth of the PLL when exiting from holdover.
  - Selecting a low DSPLL loop bandwidth will generally lengthen the lock acquisition time. The Fastlock feature allows setting a temporary Fastlock Loop Bandwidth that is used during the lock acquisition process. The DSPLL will revert to its normal loop bandwidth once lock acquisition has completed.

See Si540x NetSync™ Reference Manual and ClockBuilder Pro for more information, recommendations, and limits for setting PLL loop bandwidths for different configurations.

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3.3. Inputs

There are three differential inputs, which can also be configured as single-ended CMOS inputs. IN0, IN1, and IN3 can support a single CMOS input, while IN2 can be configured as a dual CMOS input. This allows support for up to five CMOS inputs or any combination of differential and CMOS inputs.

In typical operation, IN3 is configured as a single CMOS input and the external TCXO or OCXO reference is connected to REF. If the PPSPLL is used, then this requires an external delay compensation feedback link that is connected from an output to, typically, IN3.

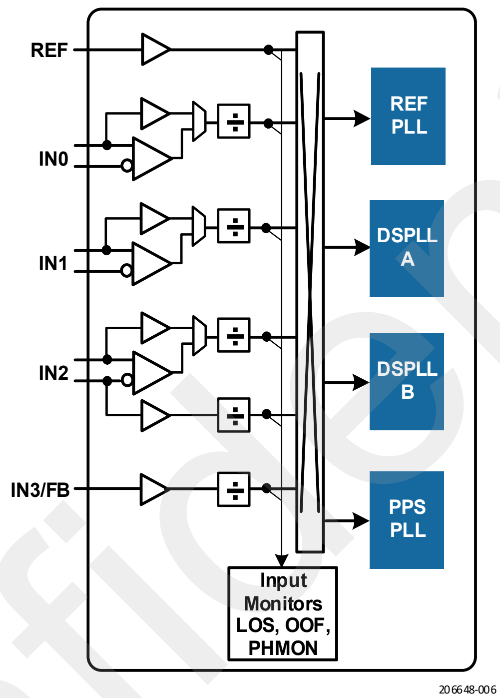

Figure 6. Input Structure

3.3.1. Input Terminations

Refer to AN1347: Si540x Schematic Design and Board Layout Guidelines and Si540x NetSync™ Reference Manual for guidance on input terminations.

3.3.2. Input Selection

Input selection for any of the PLLs can be controlled manually through pin control, Application Programming Interface (API) command, Command Line Interface (CLI) command, or automatically, using an internal state machine.

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3.3.2.1. Input Divider

The device utilizes both fractional and integer input (P) dividers to lock to any frequency input clock. The ClockBuilder Pro software will choose the optimal divide values based on the user-defined frequency plan. Each input divider (P0, P1, P2, P2b, P3, and P3b) can be configured independently of the others.

3.3.2.2. Manual Input Selection

In Manual mode, the input selection is made by defining a GPIO pin as an input select pin and changing the input pin voltage level, or by writing an API or CLI command. Any of the inputs are available to any of the PLLs through a crosspoint input selection switch. If there is no clock signal on the selected input, or if the input is not valid due to LOS/OOF/PHMON input alarms, the PLL will automatically enter Free-Run/Holdover mode. This applies to both the DSPLLs, REFPLL, and the PPSPLL.

3.3.2.3. Automatic Input Selection

When configured in this mode, each of the PLLs automatically selects a valid input that has the highest configured priority. The priority scheme is independently configurable for each PLL and supports revertive or non-revertive selection. All inputs are continuously monitored for loss of signal (LOS), invalid frequency range (OOF), and phase (PHMON). Only valid inputs that have no LOS, OOF or phase monitor (PHMON) alarms can be selected for synchronization by the automatic state machine. The PLL(s) will enter Free-Run or Holdover mode if there are no valid inputs available.

3.3.3. Unused Inputs

Unused inputs should be configured as "Unused (Powered Down)", and the pins may be left unconnected or ac-coupled to ground. See AN1347: Si540x Schematic Design and Board Layout Guidelines and Si540x NetSync™ Reference Manual for recommendations on how to minimize system noise on any CMOS input and/or any differential input configured as "Enabled" but not actively being driven by a clock.

3.3.4. Phase Readout (PHRD)

The Phase Readout Device API command can be used to measure the phase difference between different input clocks to the Si540x. Unused inputs that are not assigned to a DSPLL can also be configured as phase readout (PHRD) or phase readout feedback (PHRD_FB) inputs. These inputs can be used to measure the phase of an output of the Si540x to the input(s) of known phase. PHRD and PHRD_FB inputs use the same alarms, such as LOS/OOF/PHMON, as the other clock inputs, but they are not assigned to a DSPLL.

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3.4. Input Clock Switching

Clock inputs applied to the Si540x can be either from the same source (0 ppm, same nominal frequency) or different sources (non-0 ppm, different nominal frequencies). The Si540x automatically determines the optimal switching mode depending on the nominal frequency difference between the clocks at the time of the switch. When switching between 0 ppm inputs, the Si540x performs either a hitless switch with phase buildout (PBO) or a phase pull-in (PPI) switch depending on the user selection in ClockBuilder Pro. When the input clocks have a non-0 ppm offset, the Si540x performs a frequency-ramped input switch. Automatic input clock switching is not available for PPSPLL. See the Si540x NetSync™ Reference Manual for additional guidance on input clock switching modes. All input clock switches are glitchless, meaning there will be no runt pulses generated at the output during the transition.

3.4.1. Hitless Input Switching for 0 ppm Clocks—Phase Buildout (PBO)

Applications like SyncE require that transients are kept to a minimum when switching between input clocks. Hitless switching with phase buildout (PBO) is a feature that prevents a transient from propagating to the output when switching between two clock inputs that have a fixed phase relationship. A hitless switch can only occur when the two input frequencies are frequency locked, meaning that the nominal frequencies are the same (0 ppm). Due to the nature of hitless switching, the input-to-output delay of the PLL is not preserved. The DSPLL simply absorbs the phase difference between the two input clocks during an input switch. The phase buildout feature supports clock frequencies down to a minimum input frequency of 8 kHz.

The figure below shows the Si540x output transient performance of an input hitless switch between two clock inputs that are at a 0 ppm offset. The Si540x is locked to input IN2 = 156.25 MHz with a second input IN3 = 322.265625 MHz, and both inputs have a 0 ppm offset. Input IN2 is lost, and the Si540x switches to IN3. The plot shows 100 switching events with a typical hitless switching phase transient propagated to the outputs of less than 50 ps and a worst case phase transient of 89 ps when switching between two clock inputs that have a fixed phase relationship.

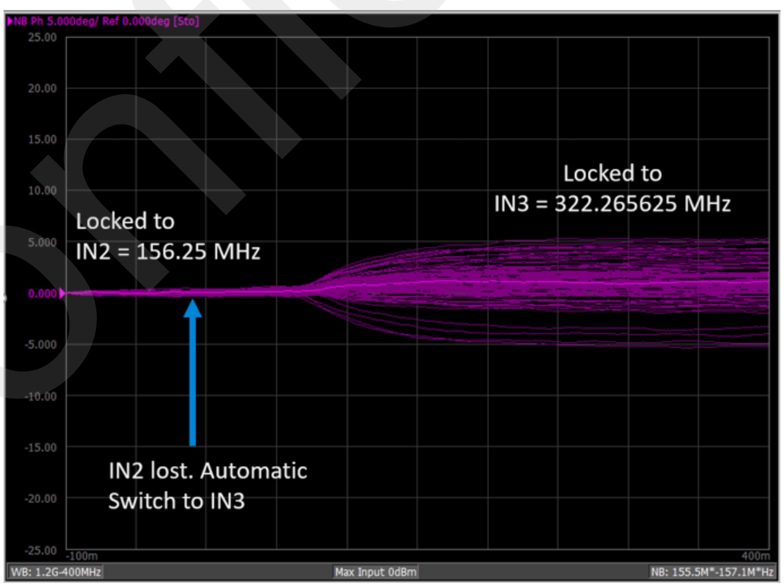

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Figure 7. Si540x Output Transient Performance of an Input Hitless Switch between Two Clock Inputs at 0 ppm Offset

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3.4.2. Phase Pull-In (PPI) Input Switching for 0 ppm Clocks

In some applications, the output phase must track the input phase with minimal delay. This is particularly common in applications which require synchronization to an external 1PPS such as a GNSS receiver or traditional fronthaul clocking. When the application requires the input-to-output delay to be preserved after clock switching, the phase pull-in clock switching mode should be selected. In this mode, the output phase will be pulled in at a user-programmable ramp rate referred to as the PPI slope (ns/s). With phase pull-in switching, the output phase always aligns with the newly selected input. PPI is always enabled for zero-delay mode and PPSPLL applications.

3.4.3. Ramped Input Switching for Non-0 ppm Clocks

The ramped switching feature allows the DSPLLs to switch between two input clock frequencies that have a non-0 ppm offset without an abrupt frequency transient at the output. When the two input clock frequencies are not the same nominal frequency, the DSPLL will pull in the frequency difference between inputs at the ramp rate that is programmable in ClockBuilder Pro from ppb/s to ppm/s. The Loss-of-Lock (LOL) and the LOOP_FILTER_RAMP_IN_PROGRESS indicators (accessible through the Device API) will assert while the DSPLL is ramping to the new clock frequency.

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3.5. Outputs

The Si5403 supports 18 differential output drivers configurable as ac-coupled LVPECL, LVDS, S-LVDS, CML, HCSL, LVCMOS, or Slew Rate Limited (SRL) LVCMOS. When in LVCMOS mode, the differential pair becomes two single-ended (SE) outputs for a maximum of 36 possible outputs. Similarly, Si5402 supports 14 differential or 28 SE outputs, and Si5401 supports 10 differential or 20 SE outputs. Depending on the clock device (Si5403, Si5402, or Si5401), up to two outputs may be configured as SRL LVCMOS outputs. This allows limiting the rise time of the output signal to reduce the possibility of crosstalk to adjacent output drivers. See 3.5.3. Slew Rate Limited (SRL) LVCMOS Outputs for more information. The outputs have power supply pins (VDDOx) with defined output driver groups, which can be individually powered by 3.3, 2.5, or 1.8 V. The LVCMOS output voltage is set by the VDDOx pin. Refer to 7. Pin Descriptions.

3.5.1. Output Crosspoint

A crosspoint allows any of the output drivers to connect with any of the PLLs available for that clock device (Si5403, Si5402, or Si5401). A digital output delay adjustment is possible on each of the outputs connected to the REFPLL. The crosspoint configuration and delay adjustments are programmable and may be stored in NVM so that the desired output configuration is ready at power up.

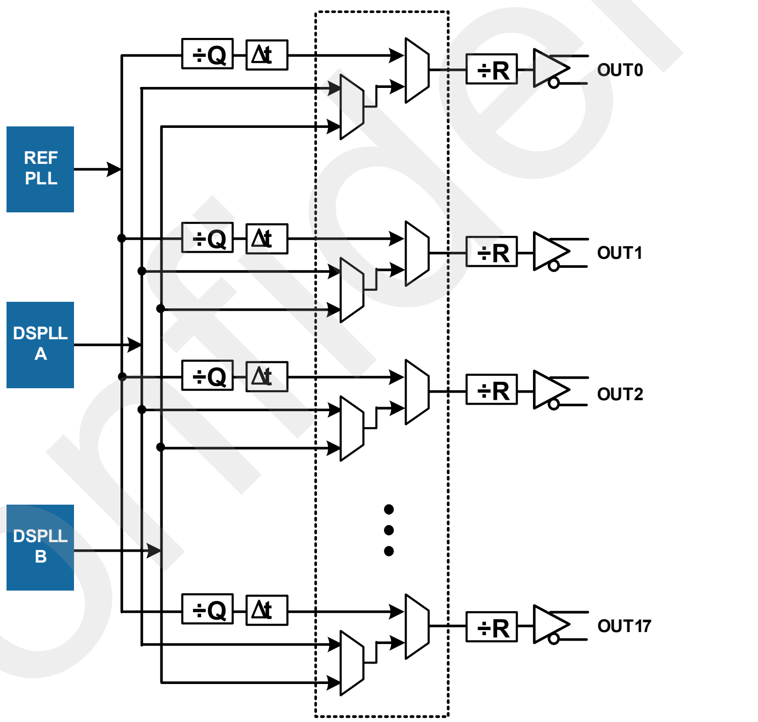

Figure 8. Output Structure

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3.5.2. Differential and LVCMOS Output Terminations

See AN1347: Si540x Schematic Design and Board Layout Guidelines and Si540x NetSync™ Reference Manual for guidance on output terminations.

3.5.3. Slew Rate Limited (SRL) LVCMOS Outputs

The swing of LVCMOS and SRL outputs is rail-to-rail; so, the swing is determined by the voltage of the corresponding VDDO pin of the LVCMOS or SRL LVCMOS output. Each output driver configured as LVCMOS or SRL LVCMOS has two outputs, OUTx/OUTxb. The polarity of each of the two outputs may be independently configured as a noninverted or inverted output as well as enabled or disabled.

Depending on the device (Si5403, Si5402, or Si5401), up to two outputs may be configured as SRL LVCMOS outputs, which have a programmable slew rate and generate significantly less crosstalk than conventional LVCMOS outputs is useful in jitter-critical applications. Refer to 7. Pin Descriptions for each clock device’s (Si5403, Si5402, or Si5401) output pin description and to see which outputs have slew rate control, it’s applicable output driver group, and VDDOx pin.

SRL LVCMOS output clocks on OUT16/16b and OUT17/17b are intended only for low frequency clock applications. Refer to the Si540x NetSync™ Reference Manual for the maximum Fout supported for each slew rate selection.

3.5.4. Output Enable/Disable

Each output driver may be enabled/disabled through programmable GPIO pins. There are two output enable groups, OE0 and OE1, which are logically OR'ed together to determine which outputs are enabled at any point in time. ClockBuilder Pro allows the control and selection of the GPIO pin mapping to the outputs.

Outputs may also be enabled/disabled using the device API. If an output is assigned as GPIO controlled, it cannot be controlled via the API. The API controlled output enable allows for more flexibility than the GPIO control as any of the outputs can be individually enabled/disabled via an API command.

The default output enable/disable behavior is a glitchless enable/disable. For clocks to start or stop as soon as possible, accepting runt pulses or glitches, instant output enable/disable can be used.

3.5.5. State of Disabled Output

The disabled state of an output driver may be configured as stop high, stop low, or Hi-Z. CMOS outputs <2 MHz can also be configured as Hi-Z with weak pullup/down.

Differential outputs, when disabled, will maintain the output common-mode voltage even while the output is not toggling. This minimizes disturbances when disabling and enabling clock outputs.

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3.5.6. Output Dividers

The device utilizes both integer Q dividers and fractional NA, NB MultiSynth output dividers. The ClockBuilder Pro software chooses the optimal divide values based on the user-defined frequency plan.

A summary of each class of divider is listed below:

1. Output Q Divider (Q0–Q17 Si5403, Q0–Q13 Si5402, Q0–Q9 Si5401):
   - Integer Only Divide Value
   - Open loop divider taps directly off VCO
2. DSPLL A/B Feedback M Divider (MA and MB on Si5403 and Si5402, MA only on Si5401):
   - Integer or Fractional Divide Value
3. Output N Divider (NA and NB on Si5403 and Si5402, NA only on Si5401):
   - MultiSynth Divider, Integer or Fractional Divide Value
4. Output Divider (R0-R17 Si5403, R0–R13 Si5402, R0–R9 Si5401):
   - Integer Only Divide Value
5. Synchronized Dual Outputs
   - If one N divider is used in a closed loop fashion and the other N divider (second NB divider is only available on Si5403 and Si5402) is used in an open loop fashion, the dividers may be cascaded so that the output of each N-divider is derived from the same input clock source and is capable of having a fractional frequency relationship.

3.5.7. Output Skew Control

Output skew control allows outputs that are derived from the Q dividers to be phase adjusted in steps of 1/fvco or 1/(4*fvco) when the fine adjust is enabled. The exact skew adjustment and step sizes are reported on the Output Skew Control Tab of the ClockBuilder Pro Wizard.

3.6. REFPLL

The REFPLL (available on Si5403, Si5402, and Si5401) controls the central VCO, which provides many of the essential functions for the device such as generating low jitter clocks and maintaining free-run accuracy and holdover stability for all PLLs (REFPLL, DSPLLA, DSPLLB, PPSPLL). The VCO generates a high-frequency clock that can be divided through the integer Q-dividers to directly drive the outputs with the lowest possible jitter and also provides the timing reference to the DSPLL A and B any-frequency DSPLLs. The REFPLL uses two external references: an inner loop crystal (XTAL) or crystal oscillator (XO), which determines overall output jitter, and an outer loop TCXO or OCXO that is responsible for providing the clock stability needed for low bandwidth applications, such as IEEE 1588 and 1PPS/PP2S locking, as well as holdover stability in the event that no input sources are available.

3.7. DSPLL (DSPLL A, DSPLL B)

DSPLL A and DSPLL B are available on the Si5403 and Si5402; only DSPLL B is available on the Si5401. In general, both DSPLLs have identical performance and flexibility and can be independently configured and controlled through the serial interface. Each of the DSPLLs support locked, free-run, and holdover modes of operation with an optional DCO mode for IEEE 1588 applications. The DSPLLs require the external crystal (shared from the REFPLL) and an external TCXO or OCXO for added frequency stability in free-run and holdover modes.

Rather than driving the output dividers directly, DSPLL A modulates the output frequency of the REFPLL, allowing ultra-low jitter outputs to be generated locked to the DSPLL A inputs.

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3.7.1. DCO Mode

The DCOs in each of the DSPLLs can be frequency controlled in pre-defined steps ranging from <1 ppt to several ppm. This is a useful feature for IEEE 1588 applications. The DCOs can be controlled when its DSPLL is locked to an external SyncE input (hybrid SyncE + PTP mode) or when it's in Free-Run/Holdover mode. Frequency adjustments are controlled through the serial interface by triggering a Device API command or by pin control using frequency increments (FINC) or decrements (FDEC). Both the FINC and FDEC pins are available through the configurable GPIO pins. Each DSPLL can be assigned to the FINC and FDEC pins. A FINC will add the frequency step word to the DSPLL output frequency, while a FDEC will decrement it. Step sizes are configured in ClockBuilder Pro.

3.8. Zero Delay Mode (ZDM)

Zero Delay Mode (ZDM) is a mode of PLL operation in which more accurate input to output phase delay can be achieved by providing an external feedback from one of the clock outputs to one of the clock inputs. ZDM is available on each of the four PLLs (RFPLL, DSPLLA, DSPLLB, PPSPLL) and is required when the PPSPLL is enabled. For more details on implementing ZDM, see AN1347: Si540x Schematic Design and Board Layout Guidelines and Si540x NetSync™ Reference Manual.

3.9. PPSPLL

The PPSPLL is available on the Si5403, Si5402, and Si5401, allows synchronization of the Si540x to an external 1PPS (1 Hz) or PP2S (0.5 Hz) input clock, and is configurable in ClockBuilder Pro. When a valid input clock to DSPLLA is present the PPSPLL modulates DSPLLA. When DSPLLA is unused or in holdover/free-run, the PPSPLL will automatically modulate the REFPLL. The PPSPLL uses an external feedback loop to guarantee minimal input-to-output delay between the PPS input and the generated PPS output. IN3 is used as the feedback input. To minimize input to output latency in PPSPLL zero delay mode, OUT0 or other low-numbered outputs should be used as the feedback output to reduce the PCB routing distance.

See Si540x NetSync™ Reference Manual and ClockBuilder Pro for more information and recommendations regarding the PPSPLL and the features it supports.

The PPSPLL supports the features described in the following subsections.

3.9.1. Instant Lock

When an input clock is first applied to the PPSPLL, the PLL will make a measurement of input frequency to lock the PLL frequency. The PPSPLL will then measure the phase difference between the input clock and the ZDM feedback input and apply an open loop phase adjustment (referred to as a phase jam) to zero out the phase difference at a much faster rate than the low bandwidth of the PPSPLL. See Si540x NetSync™ Reference Manual for an in-depth discussion on PPSPLL instant lock and phase transients that may result.

3.9.2. Bandwidth Settings

Three separate loop bandwidths are configurable in ClockBuilder Pro:

- **Initial Lock Bandwidth**—The PPSPLL uses this bandwidth when it exits the free-run mode and attempts to lock to a new input clock.
- **Loop Bandwidth**—This sets the bandwidth of the PPSPLL once lock to an input is achieved.
- **Fastlock Bandwidth**—This sets the bandwidth of the PPSPLL when exiting from holdover.

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3.9.3. Auto and Manual Relock

When enabled, this feature allows the PPSPLL to quickly reestablish lock during an input phase step or frequency step by issuing a phase jam to the PPS output. The threshold where auto relock is triggered is definable in ClockBuilder Pro.

An alternative option to auto re-lock is to use the PHASE_READOUT API to monitor the phase offset seen by the PPSPLL. When the offset exceeds a desired threshold, manually trigger a relock/phase jam via the PPS_RELOCK API command. A manual relock may often be preferred over auto relock in order to power down or reset RF equipment relying on PPS synchronization before issuing the relock, which will cause large disturbances to the outputs synchronized to PPS.

3.9.4. Phase Slope Limit

When enabled, this feature limits the rate of phase change of the output clock(s) when a phase transient occurs at the input. The phase slope limit (PSL) is definable in ClockBuilder Pro in units of ns/s.

3.9.5. Phase Pull-in Rate

When enabled, this feature limits the phase pull-in of the PPSPLL output clock(s) during an input clock switch or exit from holdover. The phase pull-in rate (PPI) is definable in ClockBuilder Pro in units of ns/s.

3.9.6. Holdover History

The PPSPLL automatically enters holdover when its input fails. It uses the average frequency that was collected while locked to an input to prevent any disturbances at the outputs when entering holdover. The length of data collected is configurable in ClockBuilder Pro.

3.9.7. Status Monitoring

The PPSPLL has several status monitors accessible through API commands. These include (but are not limited to):

- Input Status (IN0, IN1, IN2, IN2b, IN3, REF)
  - Input Valid
  - Loss of Signal (LOS)
  - Out of Frequency (OOF)
  - Phase Monitor (Phase error, Signal late, Signal early)
- PLL Status
  - Loss of Lock (LOL status accessible through API and GPIO)
  - Out of Phase
  - Out of Frequency
  - In Holdover
  - Phase Slope Limit in Progress
  - Fastlock Bandwidth in Use

Refer to the API documentation and the Si540x Reference Manual for more detailed information.

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3.10. External Reference Clocks (XA/XB, XO Inputs)

The Si540x operates from either an external crystal oscillator (XO) connected to the XO input pins or with an optional fixed-frequency crystal (XTAL) connected to the XA, XB pins. The internal oscillator (OSC), combined with a low-cost external XTAL, produces an ultra-low-jitter reference clock for the PLLs available for that clock device (REFPLL, DSPLL A/B, and PPSPLL). When using an external XO, it's important to select one that meets the jitter performance requirements of the end application.

The Si540x also requires an external TCXO or OCXO connected to the REF pin which provides improved output frequency accuracy and stability during Free-Run mode and greater frequency stability in holdover mode. In this case, the REFPLL locks to a TCXO or OCXO that is applied.

Use ClockBuilder Pro to properly configure the device for use with the external references and see Si55xx, Si540x, and Si536x Recommended XTAL, XO, VCXO, TCXO, and OCXO Reference Manual for more information for recommendations on choose external references.

3.10.1. XA, XB Inputs

The XA/XB inputs are used to provide a fixed frequency reference for the PLLs available for that clock device (REFPLL, DSPLL A/B, and PPSPLL). The device includes internal XTAL loading capacitors which eliminate the need for external capacitors and also has the benefit of reduced noise coupling from external sources. A crystal in the range of 48 to 61.44 MHz is recommended for best jitter performance.

3.10.2. XO Inputs

An alternative to using an external XTAL is to connect a crystal oscillator (XO) directly to the XO inputs. The XO inputs accommodate both single-ended CMOS as well as differential XOs. See Si55xx, Si540x, and Si536x Recommended XTAL, XO, VCXO, TCXO, and OCXO Reference Manual for more information.

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3.11. GPIO Pins

There are four GPIO (general purpose input or output) pins with programmable functions. They can be assigned as either an input or an output from one of the functions shown in the table below. OUT6/11 can be repurposed as GPIs when they are not being used as clock outputs.

The GPIs are programmable as either active-high or active-low via ClockBuilder Pro. Active low GPIs are indicated by adding a "b" at the end of the function name, e.g., "OEb", as displayed in ClockBuilder Pro. All GPI pins have a weak pull-up (PU) or pull-down (PD) resistor to set a default state when not externally driven. The default state of the GPI is always deasserted except for OEx, which is, by default, asserted to enable the outputs. The internal resistance of the PU/PD resistor is 20 kΩ typical.

GPIO selectable status outputs (GPOs) are push-pull and do not require any external pull-up or pull-down resistors.

Table 2. GPIO Pin Descriptions

Function	Description
GPIO Selectable Control Inputs (GPI)	
FINC	DCO Frequency Increment.
FDEC	DCO Frequency Decrement.
PLLx_FORCE_HO	Force holdover for REFPLL, or DSPLL A, or DSPLL B.
PLLx_INSEL[0-2]	Input select pins for REFPLL, or DSPLL A, or DSPLL B. There are 3 bits to select from 1 of 6 inputs.
IN[0:5]_FAIL	Force input invalid. A low on this pin indicates to the automatic switching state machine that the associated input is not valid for selection. This is useful in applications that use their own input monitoring.
OE0–OE1	Output enable for specific outputs or group of outputs as defined by the grouping assigned in ClockBuilder Pro.
GPIO Selectable Status Outputs (GPO)	
PLLx_LOL	Loss of lock for REFPLL, DSPLLA, DSPLLB, PPSPLL.
INx_LOS	Loss of Signal status indicator for INx.
REF_OOF	Out of Frequency status indicator of the reference.
INx_OOF	Out of Frequency status indicator for INx.
REF_LOS	Loss of signal at XA/XB or REF pins.
PLLx_HO	This pin indicates when REFPLL, DSPLL A, DSPLL B has entered the holdover state.
INTR	Interrupt pin for the device. Programmable Boolean combination of PLLx_LOL, INx_LOS, INx_OOF, PLLx_HO, REF_LOS, REF_OOF.
Primary Serial Interface (I2C/SPI)	
A1/SDO	A1/SDO of Primary SPI Port. **Assignable to GPIO3 only.
A0/CSb	A0/CSb of Primary SPI Port.
SDA/SDIO	SDA/SDIO of Primary SPI Port.
SCLK	SCLK of Primary SPI Port.
Secondary Serial Interface (3-wire SPI Only)	
CSb2	CSb of secondary SPI Port. **Assignable to GPIO0 only.
SDIO2	SDIO of a secondary SPI Port. **Assignable to GPIO1 only.
SCLK2	SCLK of a secondary SPI port. **Assignable to GPIO2 only.

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3.12. Device Initialization and Reset

Once power is applied and RSTb is de-asserted, the device begins loading preconfigured register values and configuration data from NVM, and performs other initialization tasks. Communicating with the device through the serial interface is possible once this initialization period is complete (see tRDY). No output clocks will be generated until the initialization is complete, and the device locks to the external (VC)XO/XTAL (see tSTART_XO and tSTART_XTAL). A reset, initiated using the RSTb pin or through the Device API RESTART command, restores all registers to the values stored in NVM, and all circuits, including the serial interface, will be restored to their initial state. All clocks will stop during a hard reset. Other feature-specific resets are also available. See the Si540x Reference Manual and AN1360: Serial Communications and API Programming Guide for Si536x, Si540x, and Si55xx Devices for more information on different methods of resetting the device.

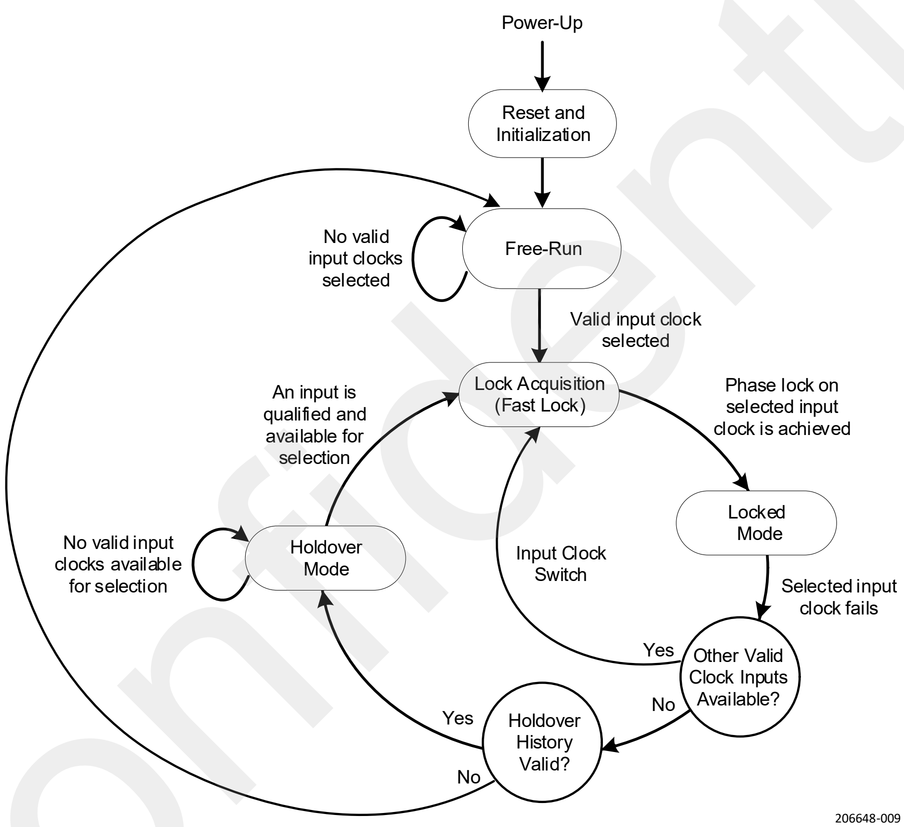

Figure 9. Modes of Operation

3.13. Modes of Operation (REFPLL, DSPLL A, DSPLL B)

Once initialization is complete, each PLL independently operates in one of four modes: Free-Run, Lock Acquisition, Locked, or Holdover. A state diagram showing the modes of operation is shown in the figure above. The following sections describe each of the modes in greater detail.

3.13.1. Free-Run Mode

The PLLs will automatically enter Free-Run Mode once power is applied to the device and initialization is complete. In this mode the frequency accuracy of the generated output clocks is entirely dependent on the frequency accuracy of the reference clock source. If a XTAL is connected to the XA/XB pins then the clock outputs will generate a frequency at the XTAL's accuracy. For example, if a XTAL is operating at –28 ppm then clock outputs will also be –28 ppm. The same is true if a XO is connected at the XO_IN inputs instead of using XTAL at XA/XB. The frequency stability of the outputs will also be determined by the XTAL or XO.

When a TCXO or OCXO is connected to the REF inputs, then the frequency accuracy and stability of the outputs will be dominated by the TCXO or OCXO. This is recommended for applications that need better accuracy and stability than what the XTAL or XO can provide.

3.13.2. Lock Acquisition Mode

Each of the PLLs independently monitors its configured inputs for a valid clock. If at least one valid clock is available for synchronization, a PLL will automatically start the lock acquisition process. If the fast lock feature is enabled, they will acquire lock faster than the PLL Loop Bandwidth would provide and then transition to the normal PLL loop bandwidth. During lock acquisition the outputs will generate a clock that follows the VCO frequency change as it pulls-in to the input clock frequency.

The PLL_STATUS Device API command reports the lock status of a PLL. When the PLL output frequency is within the threshold defined on the Frequency LOL (FLOL) page in ClockBuilder Pro, the PLL_OUT_OF_FREQUENCY bit de-asserts. Some time after that, the PLL will pull in the remaining phase defined on the Phase LOL (PLOL) page in ClockBuilder Pro. Once the PLL is frequency and phase locked, the PLL_LOSS_OF_LOCK (LOL) bit de-asserts, and the PLL enters locked mode.

3.13.3. Locked Mode

Once locked, the PLL will generate clock outputs that are both frequency and phase locked to their selected input clocks. The PLL loop bandwidths can be independently configured. Any frequency changes (e.g., because of temperature variations) of the reference clock (REF) within the PLL loop bandwidth will be corrected by the loop ensuring 0 ppm lock to its input clock (IN). Any frequency changes of the reference clock (REF) beyond the PLL loop bandwidth will pass through to the clock output.

3.13.4. Holdover Mode

Any of the PLLs will automatically enter Holdover Mode when the selected input clock becomes invalid, holdover history is valid, and no other valid input clocks are available for selection. Each PLL uses an averaged input clock frequency as its final holdover frequency to minimize the disturbance of the output clock phase and frequency when an input clock suddenly fails. The holdover circuit for each PLL stores historical frequency data while locked to a valid input clock. The final averaged holdover frequency value is calculated from a programmable window within the stored historical frequency data. Both the window size and delay are programmable as shown in the figure below. The window size determines the amount of holdover frequency averaging. The delay value allows ignoring frequency data that may be corrupt just before the input clock failure.

The maximum window size is a function of input frequency and is reported in ClockBuilder Pro for each PLL. 240 seconds is the maximum window size for 1PPS/PP2S inputs as shown in the figure below. For higher frequency inputs up to 5000 seconds of holdover history can be stored.

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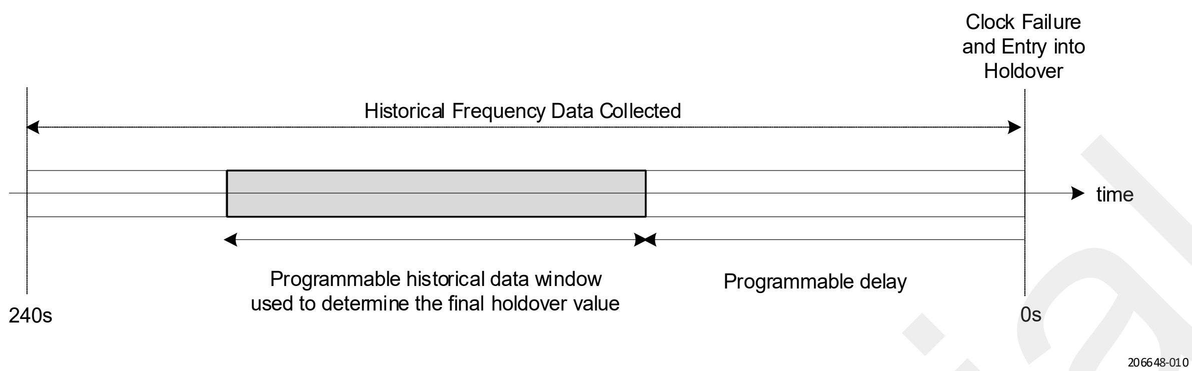

Figure 10. Programmable Holdover Window

When entering Holdover, a PLL will pull its output clock frequency to the calculated averaged holdover frequency. While in Holdover, the output frequency drift is entirely dependent on the external reference clock connected to the REF_IN input. If the input clock becomes valid, a PLL will automatically exit the Holdover mode and reacquire lock to the new input clock. This process involves pulling the output clock frequency to achieve frequency and phase lock with the input clock. This pull-in process is glitchless.

The PLL output frequency when exiting Holdover can be ramped. Just before the exit is initiated, the difference between the current holdover frequency and the new desired frequency is measured. Using the calculated difference and a user-selectable ramp rate, the output is linearly ramped to the new frequency. The PLL loop BW does not limit or affect ramp rate selections (and vice versa). ClockBuilder Pro defaults to ramped exit from Holdover and Free-Run. The ramp rate settings are configurable for initial lock (exit from free-run), exit from holdover, and clock switching. If ramped holdover exit is disabled, the holdover exit is governed either by (1) the PLL loop BW or (2) the PLL Fastlock bandwidth, when enabled.

3.14. IEEE 1588 Mode

3.14.1. Synchronizing to a Master Clock when in IEEE 1588 Mode

When IEEE 1588 mode is used (see Figure 11. Modes of Operation (IEEE 1588 Mode - BMCA) on the next page), the servo loop software will check the Announce Messages it receives from upstream master nodes (in its clock domain), and, using the BMCA, will choose the master with the best clock (which could be itself). It then begins to synchronize its local clock to that of the master's clock using IEEE 1588 timestamp.

The IEEE 1588 Servo Loop Software will acquire lock using the Startup Time Constant and then transition to the Main Time Constant once the node synchronizes its local clock to that of the selected master's clock. These time constants effectively set the servo loop bandwidth and are user-configurable.

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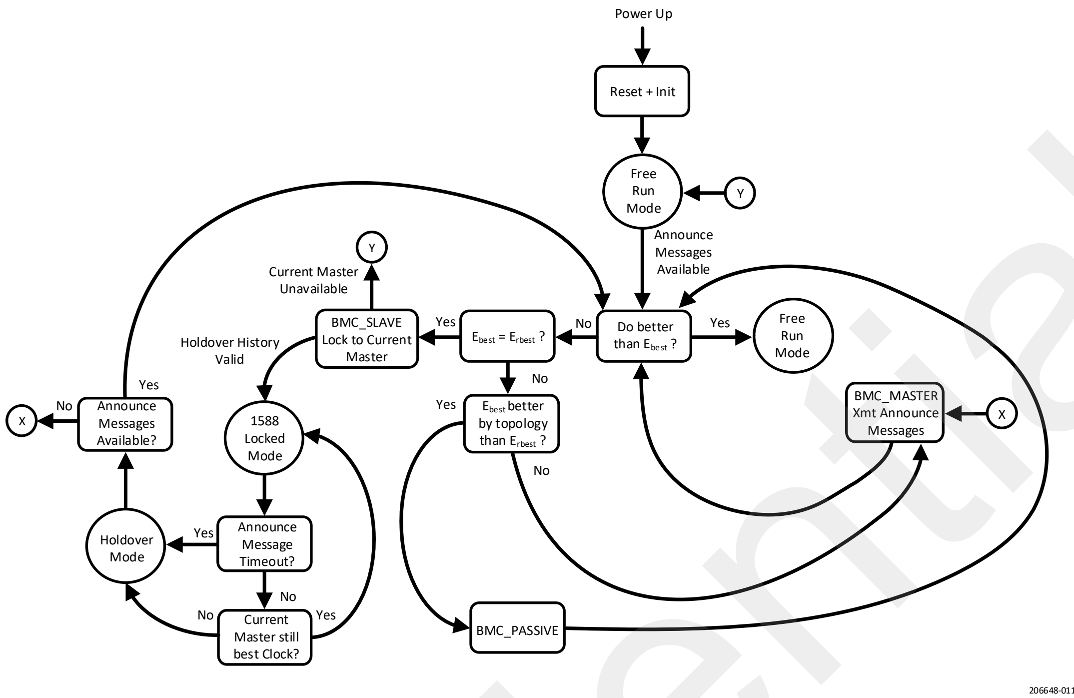

Figure 11. Modes of Operation (IEEE 1588 Mode - BMCA)

3.15. PTP Holdover Mode (IEEE 1588 Holdover Mode)

When timestamps are no longer available (either due to Announce Message timeout from the current master clock or due to selecting a better clock from a remote master via BMCA), the node will enter PTP holdover. In this mode, the accuracy and stability of the output clocks synchronized to PTP will be dependent on the PTP clock average calculation, which is dependent on the "control average" time constant, as well as the stability of the input reference clock. If the reference is from a SyncE input, then this PTP holdover mode will be referred to as "PTP holdover with physical layer assist", and the outputs will assume the stability of the SyncE clock.

If there is no physical layer clock synchronizing the PLL steered by PTP, then it will synchronize to the local reference oscillator, and the outputs will assume the stability of this oscillator. This PTP holdover mode is referred to as "holdover without physical layer assist". Once the connection to an upstream master has been reestablished and the IEEE 1588 timestamps are once again available, the servo loop will exit from PTP holdover and begin synchronizing its local clock to that of the new master.

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3.16. Status and Alarms

The Si540x monitors the input clocks and reference input for status and alarms. The status and alarms provide the internal state machine with real time phase and frequency monitoring used for making decisions, such as switching inputs or entering holdover.

3.16.1. Input Clock Status

All input clocks are continuously monitored for faults using the Loss-of-Signal (LOS), Out-of-Frequency (OOF), and Phase Monitor (PHMON) alarms. When a differential input is configured as a dual CMOS input, then each CMOS input is independently monitored. Any enabled alarms for an input, such as LOS/OOF/PHMON, are logically ORed together to produce the input invalid alarm.

Any input clock with an alarm is not valid until all alarms are cleared. If a PLL is locked to an input clock and that input clock becomes invalid, then the PLL may either switch to a valid input or enter holdover mode, depending on how the device is programmed.

API commands can be used to indicate if an alarm is valid, pending short term fault, under validation or invalid.

3.16.1.1. Loss of Signal (LOS)

The loss of signal alarm measures the period of each input clock cycle to detect phase irregularities or missing clock edges. Each of the input LOS circuits has its own programmable sensitivity, which allows missing edges or intermittent errors to be ignored. Loss of signal sensitivity is configurable using the ClockBuilder Pro utility. The LOS status for each of the monitors is accessible by checking the INPUT_STATUS API.

3.16.1.2. Out of Frequency (OOF) Detection

All inputs are monitored for frequency accuracy with respect to a reference which can be configured as any of the inputs. OOF status is determined by the combination of both a precise OOF monitor and a fast OOF monitor. An option to disable either monitor is available. The live OOF register always displays the current OOF state and its sticky register bit stays asserted until cleared.

The precision OOF monitor circuit measures the frequency of all input clocks to within ±1 ppm accuracy with respect to the selected OOF frequency reference. A valid input clock frequency is one that remains within the OOF frequency range which is register configurable from ±0.1 ppm to ±500 ppm in steps of 0.1 ppm. A configurable amount of hysteresis is also available to prevent the OOF status from toggling at the failure boundary. An example is shown in the figure below. In this case, the OOF monitor is configured with a valid frequency range of ±12 ppm and with 4 ppm of hysteresis.

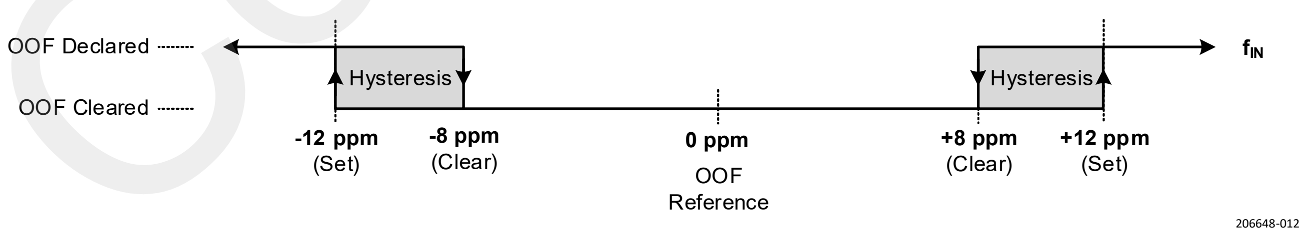

Figure 12. Example of Precise OOF Monitoring Assertion and De-assertion Triggers

3.16.1.3. Phase Monitor (PHMON)

If a clock input undergoes a phase transient, a PLL locked to that input will filter the transient by its loop bandwidth; however, the transient will propagate to the output. Transients that propagate to the output have the potential to negatively impact downstream devices.

Phase Monitor (PHMON) alarm monitors the input clock phase or accumulated phase, and, if the input transient exceeds the programmable threshold, the PHMON alarm will be asserted. PHMON, like the other alarms, is quick to be asserted when the thresholds are violated yet slower to be deasserted to prevent chattering around the threshold.

Each input clock has an independent PHMON alarm. Each alarm can be enabled/disabled individually, and its associated threshold may be independently configured. Note that OOF must be enabled and properly configured for PHMON to operate.

A ZDM input may use the PHMON alarm for monitoring purposes. However, it will have no effect on PLL bandwidth selection and will not cause input switching.

3.16.1.4. Short Term Holdover

The Short-Term Holdover (STHO) feature may be used when the input clock is expected to have a short-term fault and then quickly recover.

If an input clock has STHO enabled, and an LOS/OOF/PHMON alarm is asserted, then a PLL locked to that input will enter holdover and wait for a programmable duration until all alarms on the input clock are deasserted.

If all alarms on the input clock are deasserted before the programmable amount of time has passed, then the PLL will gracefully relock to the same input clock. If all the alarms on the input clock are not deasserted before the programmable amount of time has passed, then the PLL will either switch to the next priority input clock or remain in holdover, depending on the input clock selection settings.

If STHO is disabled, then the PLL will skip the short-term holdover time and immediately switch to the next priority input clock or enter holdover, depending on the input clock selection settings.

STHO may be programmed using Clock Builder Pro to set the duration or to enable or disable the feature for each input clock individually. Note that the STHO setting will affect all PLLs assigned to that input.

3.16.2. PLL Status

REFPLL, DSPLL A, DSPLL B, and PPSPLL are continuously monitored for Loss-of-Lock (LOL). The final LOL status indicator is the logical OR of the Frequency Loss-of-Lock and Phase Loss-of-Lock statuses. See the Si540x Reference Manual for more information.

3.16.2.1. Loss of Lock (LOL)

There is a loss of lock (LOL) monitor for each of the PLLs (REFPLL, DSPLL A, DSPLL B, and PPSPLL). The LOL monitor asserts when a PLL has lost synchronization with its selected input clock. Any of the GPIOs can be programmed as a dedicated loss-of-lock pin that reflects the loss-of-lock condition for each of the PLLs. The LOL monitor measures both the frequency and phase difference between the input and feedback clocks of the phase detector. The frequency monitor gives frequency lock detection (FLOL) while the phase monitor indicates true phase lock PLOL by detecting one or more single slips. Both the phase and frequency LOL monitors have clear and set thresholds and a timer to prevent LOL assertion from toggling or chattering as the DSPLL completes lock acquisition. The cycle slip detector also has configurable sensitivity.

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3.16.2.2. Frequency Loss of Lock (FLOL)

The Frequency Loss-of-Lock (FLOL) monitor measures the frequency difference between the input clock and the feedback clock. The upper and lower LOL thresholds are programmable, which dictates when the alarm will be asserted or deasserted. It is recommended to program the clear threshold to be less than the set threshold to allow for hysteresis in the FLOL set/clear behavior. This prevents the FLOL alarm from chattering or causing multiple interrupts. FLOL, like the other alarms, is quick to be asserted when the threshold is violated yet slower to be deasserted. The alarm validates that the frequency difference between the input and feedback clocks has truly settled to within the LOL clear threshold before the FLOL alarm is deasserted. The time required to validate the frequency difference increases as the loop bandwidth of the PLL decreases.

3.16.2.3. Lock Status Bits

There are four lock status bits that serve as four additional Frequency LOL thresholds. The Status Bit (STB) is asserted if the frequency difference between the input clock and feedback clock exceeds the programmable STB threshold. The assertion or deassertion of an STB does not contribute to the FLOL or LOL status. Rather, they serve as a way to track the lock acquisition process for DSPLL’s with a loop bandwidth of <10 Hz. The lock status bits may be read via the API. In the lock acquisition process, the deassertion of a STB does not indicate that the PLL is frequency locked. This is because the frequency may chatter around the STB threshold. On the other hand, the deassertion of FLOL requires the frequency difference to truly settle below the LOL clear threshold.

3.16.2.4. Phase Loss of Lock (PLOL)

The Phase Loss-of-Lock (PLOL) alarm measures the phase difference between the input clock and feedback clock. The PLOL set threshold is programmable so the alarm will assert or deassert depending on phase difference between the input and feedback clocks relative to the threshold setting. It is recommended to set the clear threshold below the set threshold to allow for hysteresis. This prevents the alarm from chattering or causing multiple interrupts. During the lock acquisition process, the input clock and feedback clock will likely have a significant frequency mismatch; so, the PLOL is not asserted until FLOL is deasserted. Once FLOL has been deasserted, the two frequencies are stable with respect to each other. Then the feedback clock phase can be pulled in to within the PLOL clear threshold.

3.16.2.5. Cycle Slip Detection

REFPLL, DSPLLA, and DSPLLB may be monitored for cycle slips. Like the PLOL alarm, cycle slip detection is not enabled until FLOL is deasserted. Additionally, PLOL must be enabled for cycle slip detection to be enabled. Cycle slips both in the positive and negative direction are monitored. The API can be used to read the total count of positive cycle slips, negative cycle slips and the total count or both positive and negative slips.

3.16.3. External Reference Status

An external reference must always be provided to the device. The Si540x will monitor the external reference input for LOS, OOF, and LOL. If a fault is detected on the external reference, then the outputs will be disabled. Any external reference faults may be read via the API.

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3.16.4. Interrupt Status

The interrupt flag is asserted when any of the status indicators of the device changes state. The interrupt status may be assigned a GPIO pin, or it may be checked using an API command to show which status indicator caused the interrupt to be asserted.

The Interrupt Configuration page in ClockBuilder Pro lists all the status indicators that can be programmed to activate the interrupt pin.

The status indicators that are enabled are logically OR'd together so that the assertion of any of these status indicators will cause the interrupt pin to assert. The interrupt pin status depends on the sticky versions of the individual status indicators, so the interrupt pin will stay asserted until the sticky status indicators are cleared.

3.17. Serial Interface

Configuration and operation of the Si540x is controlled by reading and writing API commands using the I2C or SPI interface. The primary SPI mode operates in either 4-wire or 3- wire modes. A second SPI port, which operates in 3-wire mode, can also be configured allowing dual port access to the device. An internal arbiter prevents contentions during bus operations so that both ports can be used simultaneously. The following tables define the GPIO pins assigned to the primary and secondary SPI ports, respectively.

Table 3. Primary Serial Interface Pins

Pin Number	3-Wire SPI	4-Wire SPI	I^2C
55	CSb	CSb	A0
52	SDIO	SDI	SDA
53	SCLK	SCLK	SCK
56	Unused	SDO	A1

Table 4. Secondary Serial Interface Pins

Pin Number	SPI Pin	Assignable GPIO Pins
16	CS2b	GPIO0
18	SDIO2	GPIO1
19	SCLK2	GPIO2

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3.18. NVM Programming

At power-up, the device loads its default configuration and settings from internal non-volatile memory (NVM). The NVM can be preprogrammed at the factory with a custom frequency plan such that the device starts generating clocks on its first power-up, or the NVM can be programmed in the field using the API command set. NVM programming in the field must be done with VDDA set to 3.3V. NVM programming in the field is not supported in Low-Power mode. For more details on NVM programming, please refer to AN1360: Serial Communications and API Programming Guide for Si536x, Si540x, and Si55xx Devices and Si540x NetSync™ Reference Manual.

3.19. Application Programming Interface (API)

Communication between the customer's host processor and the Si540x internal microcontroller (MCU) is accomplished through the serial interface. The Si540x MCU contains firmware that allows users to have command-level access to the device API. Internal registers are not accessible through the API because all features of the Si540x can be accessed through the Device API. The primary serial port (SPI or I2C) allows programming of the Si540x, and the secondary serial port (SPI 3-wire only) is intended for Phase Readback and status monitoring operations. The host processor can also communicate with the Si540x using Skyworks' optional AccuTime IEEE 1588 software and API. The AccuTime software runs on the Host processor. See the Si540x NetSync™ Reference Manual for more information and examples of the API. Details of the API commands are available through ClockBuilder Pro. For instructions to use the Device API, and for instructions on programming the clock device, see AN1360: Serial Communications and API Programming Guide for Si536x, Si540x, and Si55xx Devices.

3.20. AccuTime™ IEEE 1588 Software

The Si540x may be combined with optional AccuTime IEEE 1588 software to create a complete IEEE 1588 solution for time, phase, and frequency synchronization. AccuTime 1588 software consists of a unique servo algorithm paired with a protocol stack that all runs on the customer's host processor.

The architecture of AccuTime is shown in the simplified figure below. AccuTime is a layered architecture consisting of the customer's hardware platform and the OSAL and OEM at the bottom (system-dependent) layer, including system-dependent configuration files to customize the AccuTime software for the OS and HW platform. Next is the System-Independent Layer consisting of the AccuTime software. The example applications are provided with AccuTime and include the Sync Timing Util application and ESMC handler.

The System-Independent layer interfaces with the user's OS and hardware via API calls through the OSAL and OEM layers. This includes the C API library for controlling and monitoring the Si540x device.

The OEM Abstraction layer allows low level communications with the Si540x via SPI or I2C, GPIO, etc. The OEM layer communicates with the Linux kernel via kernel system calls and IOCTL. Device drivers in the Linux kernel communicate with the hardware devices in the user's hardware platform which includes the Ethernet PHY + MAC, Time of Day (ToD) counter block, serial input/output for transmitting/receiving ToD information, as well as the Si540x.

The OEM and OSAL layers use system calls and rely on the Linux kernel. In the OEM layer case, system calls are used to interact with the hardware, whereas in the OSAL layer case, system calls are used to leverage the software specific functions provided by the kernel (mutexes, semaphores, queues, etc.).

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The AccuTime 1588 Protocol Stack provides an application in the user space running on the host processor on top of the Linux OS. The protocol stack processes the PTP messages and passes the necessary data to the PTP servo. The servo loop controls the 1588 DCO operation to the Si540x device to adjust the system clock it sends to synchronize the ToD counter in the host to align it with the ToD in the master.

Software setup, configuration, API / CLI command libraries, and porting details are fully documented in the AccuTime Software Release.

AccuTime software is available under a license. Contact your Skyworks Representative for more information.

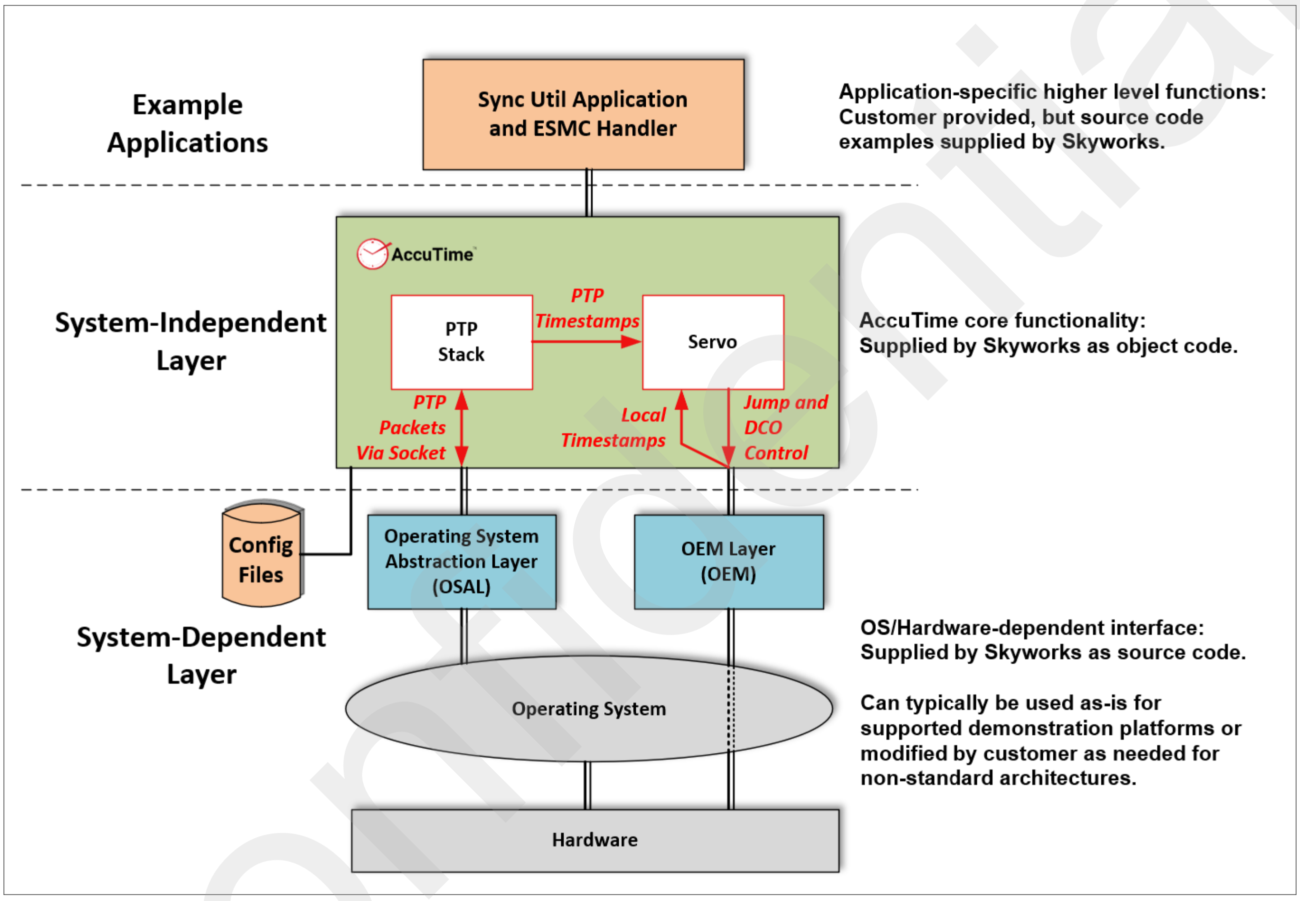

Figure 13. AccuTime Simplified Architecture

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3.21. Power Supplies

The Si540x has 14 power supply pins. The separate power supplies are used for different functions, providing power locally where it is needed on the die to improve isolation. When no outputs are enabled for a particular VDDOx, that supply pin may be left unconnected. Please refer to the Si540x NetSync™ Reference Manual for more details on power management. See AN1347: Si540x Schematic Design and Board Layout Guidelines for filtering recommendations.

3.21.1. Power Supply Sequencing

There are no power sequencing requirements between supplies. VDDA and VDD18 should be powered up before releasing RSTb. VDDA must be equal to the highest voltage supply.

3.21.2. Power Supply Ramp Rate

Power supply ramp times must stay within the maximum supply voltage ramp rate as defined in Table 8, DC Characteristics.

3.21.3. Low-Power Mode

In Low-Power Mode, the analog core supply voltage (VDDA) of the Si540x is set to 1.8 V in order to reduce power consumption. Since VDDA must be equal to the highest voltage applied to the Si540x, in Low-Power Mode, all voltage supplies including VDDO must be 1.8 V. A 1.8 V VDDO restricts the output format to S-LVDS, LVCMOS, or HCSL. If LVPECL or LVDS output format is required, Low-Power Mode cannot be used. NVM programming in the field is not supported in Low-Power Mode since NVM programming requires VDDA to be 3.3V. Please refer to the Si540x NetSync™ Reference Manual for VDDREF and XO/XTAL connections and terminations for low power mode.

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4. Electrical Specifications

All minimum and maximum specifications in the following tables are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise noted.

Table 5. Absolute Maximum Ratings[1,2]

Parameter	Symbol	Test Condition	Value	Unit
DC Supply Voltage	V_{DDIN}		–0.5 to 3.8	V
	V_{DDXO}		–0.5 to 3.8	
	V_{DD18}		–0.5 to 2.4	
	V_{DDA}		–0.5 to 3.8	
	V_{DDO}		–0.5 to 3.8	
	V_{DDIO}		–0.5 to 3.8	
Input Voltage Range	V_{I1}	XO_IN/XO_INb, INx/INxb	–0.85 to 3.8	V
	V_{I2}	GPIO0-3, RSTb, SCLK, SDA/ SDIO, A0/CSb	–0.5 to 3.8	
	V_{I3}	XA/XB	–0.5 to 2.7	
Latch-up Tolerance	LU		JESD78 Compliant	
ESD Tolerance	HBM	100 pF, 1.5 kΩ	2.0	kV
Storage Range	T_{STG}		–55 to 150	°C
Maximum Junction Temperature in Operation	T_{JCT}		125	°C
Soldering Temperature (Pb-free profile)[3]	T_{PEAK}		260	°C
Soldering Time at TPEAK (Pb-free profile)[3]	T_P		20 to 40	sec

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. RoHS-6 compliant. For more packaging information, go to https://www.skyworksinc.com/Product_Certificate.aspx
3. The device is compliant with JEDEC J-STD-020.

Table 6. Thermal Conditions

Parameter	Symbol	Test Condition	Typical Value		Unit
			JEDEC[1]	CEVB[2]	
Thermal Resistance Junction to Ambient	Θ_{JA}	Still Air	16.15	11.17	°C/W
		1 m/s	10.77	8.10	
		2 m/s	9.63	7.53	
Thermal Resistance Junction to Board	Ψ_{JB}[3]	Still Air	3.33	3.08	°C/W
Thermal Resistance Junction to Top Center	Ψ_{JC}	Still Air	0.03	0.05	°C/W

1. Based on PCB dimension: 4" x 4.5", PCB thickness: 1.6 mm, number of Cu layers: 2.
2. Customer EVB: 8-layer board, board dimensions: ~9x9", all 8-layers are copper poured.
3. ΨJB can be used to calculate the junction temperature based on the board temperature and power dissipation for a given frequency plan, Tj = TPCB + (ΨJB*PD). TPCB should be measured as close to the Si540x DUT as possible since temperature may vary across the PCB.

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Table 7. Recommended Operating Conditions

V_{DD18} = 1.8 V ±5%, V_{DDA} = V_{DDXO} = 3.3 V ±5%. All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C
Low-Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDXO} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Temperature	T_A		–40	25	95	°C
Board Temperature	T_B		–40	65	105	°C
Junction Temperature	T_{JMAX}[1]		—	—	125	°C
Core Supply Voltage	V_{DD18}		1.71	1.80	1.89	V
	V_{DDA}		3.14	3.30	3.47	
		Low-Power Mode	1.71	1.80	1.89	
	V_{DDXO}		3.14	3.30	V_{DDA}[2]	
		Low-Power Mode	1.71	1.80	1.89	
Input Supply Voltage	V_{DDIN}		3.14	3.30	V_{DDA}	V
			2.38	2.50	2.62	
			1.71	1.80	1.89	
GPIO Supply Voltage	V_{DDIO}		3.14	3.30	V_{DDA}[2]	V
			2.38	2.50	2.62	
			1.71	1.80	1.89	
Clock Output Driver Supply Voltage	V_{DDO}		3.14	3.30	V_{DDA}2	V
			2.38	2.50	2.62	
			1.71	1.80	1.89	

1. Ambient temperature of 95 °C may not be possible with all configurations. This is dependent on device configuration. Tj cannot exceed a max of 125 °C.
2. V_{DDA} must be greater than or equal to the highest voltage applied to the device. In Low-Power Mode, all voltage supplies must be set to 1.8 V.

Table 8. DC Characteristics

V_{DD18} = 1.8 V ±5%, V_{DDA} = V_{DDXO} = 3.3 V ±5%. All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C
Low-Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDXO} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Core Supply Current (V_{DD18} + V_{DDA})	I_{DD18}	Si540x[1,2]	—	420	670	mA
	I_{DDA}	Si540x[1,2]	—	200	240	
	I_{DD18_PD}	RSTb = 0	—	120	300	
	I_{DD_PD}	RSTb = 0	—	15	16	
Periphery Supply Current (V_{DDIN} + V_{DDIO} + V_{DDXO})	I_{DDIN} + I_{DDIO}	Si540x[1,2]	—	55	72	mA
	I_{DDREF}	Si540x[1,2]	—	12	15	
	I_{DDIN_PD} + I_{DDIO_PD} + I_{DDREF_PD}	RSTb = 0	—	2	3	

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Table 8. DC Characteristics(Continued)

V_{DD18} = 1.8 V ±5%, V_{DDA} = V_{DDXO} = 3.3 V ±5%. All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C
Low-Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDXO} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Buffer Supply Current (V_{DDOX})	I_{DDOX} (per output)	LVPECL (2.5 V, 3.3 V) @ 156.26 MHz[3]	—	24	26	mA
		LVDS (2.5 V, 3.3 V) @ 156.26 MHz[3]	—	13	15	
		S-LVDS (1.8 V) @ 156.26 MHz[3]	—	12	14	
		3.3 V LVCMOS @ 156.26 MHz[4]	—	19	22	
		2.5 V LVCMOS @ 156.26 MHz[4]	—	15	17	
		1.8 V LVCMOS @ 156.26 MHz[4]	—	11	12	
		HSCL Internal Termination (1.8 V, 2.5 V, 3.3 V) @ 156.26 MHz[5]	—	20	23	
		CML (1.8 V, 2.5 V, 3.3 V) @ 156.26 MHz[3]	—	14	17	
	I_{DDOX_PD}	RSTb=0	—	0.23	0.3	
Total Power Dissipation	P_D	Si540x[1]	—	2.1	2.8	W
		Si540x Low-Power Mode[2]	—	1.4	2	
Supply Voltage Ramp Rate	T_{VDD}	Fastest VDD ramp rate allowed on startup	—	—	100	V/ms

1. Typical test condition: The following frequencies on 12 LVDS outputs: 4 to 156.25 MHz (Q), 2 to 312.5 MHz (Q), 1 to 125 MHz (Q), 1 to 100 MHz (NB), 1 to 50 MHz (NB), 2 to 644. 53125MHz (NA), 1 to 322.265625 MHz (NA). Si5401 does not use (NB).
2. Typical test configuration: Same as Note 1, except all supplies set to 1.8 V for Low-Power Mode. Output formats changed to S-LVDS format.
3. Differential outputs terminated into an ac-coupled differential 100 Ω load.
4. LVCMOS outputs measured into a 5-inch, 50 Ω PCB trace with 5 pF load.
5. No external termination; amplitude 800 mVpp_se.

Table 9. Input Specifications

V_{DD18} = 1.8 V ±5%, V_{DDA} = V_{DDXO} = 3.3 V ±5%. All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C
Low-Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDXO} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
LVCMOS (XO Applied to XO_IN)						
Input frequency range	f_{IN_CMOS}	Frequencies > 48 MHz are recommended for best performance	30.72	—	250	MHz
Slew rate[1, 2, 3]	SR		0.75	—	—	V/ns
Input voltage	V_{IL}		—	—	V_{DDXO} x 0.3	V
	V_{IH}		V_{DDXO} x 0.7	—	—	
Input resistance	R_{IN}		—	63	—	kΩ
Duty cycle	DC		40	—	60	%
Capacitance	CI_{N_SE}		—	1.25	—	pF
Differential (XO Applied to XO Input Pins)						
Input frequency range	f_{IN_DIFF}	Frequencies > 48 MHz are recommended for best performance	30.72	—	250	MHz
Voltage swing[2]	V_{IN_DIFF}	Differential, AC coupled	200	350 (LVDS) 800 (LVPECL)	1800	mVpp_se
	V_{IN_SE}	Single-ended, AC coupled	400	1600	1800	
Slew rate[1, 2, 3]	SR		0.75	—	—	V/ns
Duty cycle	DC		40	—	60	%

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Table 9. Input Specifications (Continued)

V_{DD18} = 1.8 V ±5%, V_{DDA} = V_{DDXO} = 3.3 V ±5%. All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C
Low-Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDXO} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Capacitance	C_{IN_DIFF}		—	2.5	—	pF
Crystal (Connected to XA/XB Pins)[4]						
Frequency range	f_{IN_XTAL}		48	54	61.44	MHz
Load capacitance	C_L		—	8	—	pF
Crystal drive level	D_L		—	—	200	µW
Equivalent series resistance	R_{ESR}		Refer to Si55xx/Si540x/Si536x Recommended XTALs Reference Manual to determine ESR and shunt capacitance values.			
Shunt capacitance	C0					
Differential (INx/INxb)						
Input frequency range	f_{IN_DIFF}	Differential, AC coupled	0.008	—	1000	MHz
	f_{IN_SE}	Single-ended, AC coupled	0.008	—	250	
Voltage swing	V_{IN_DIFF}	Differential, AC coupled	200	350 (LVDS) 800 (LVPECL)	1800	mVpp_se
	V_{IN_SE}	Single-ended, AC coupled	400	1600	1800	
Slew rate[3, 5]	SR		0.4	—	—	V/ns
Duty cycle	DC		40	—	60	%
Capacitance	C_{IN_DIFF}		—	2.5	—	pF
LVCMOS (INx/INxb)						
Input frequency range	f_{IN_LVCMOS}		PP2S PPS 0.008	—	250	MHz
Slew rate[3, 5]	SR		0.2	0.4	—	V/ns
Input voltage	V_{IL}		—	—	V_{DDIN} x 0.3	V
	V_{IH}		V_{DDIN} x 0.7	—	—	
Input resistance	R_{IN}		—	63	—	kΩ
Duty cycle	DC		40	—	60	%
Capacitance	C_{IN_SE}		—	1.25	—	pF
Other Control Input Pins (RSTb, FINC, FDEC, OE, PLLx_FORCE_HO, PLLx_INSEL[#], IN_FAIL[#])						
Update rate	f_{UR}	RSTb[6]	—	—	1	Hz
		FINC, FDEC	—	—	800	kHz
Input voltage	V_{IL}		—	—	V_{DDIN} x 0.3	V
	V_{IH}		V_{DDIN} x 0.7	—	—	
Minimum Pulse Width	PW		150	—	—	ns
Programmable Internal Pullup, Pulldown	R_{IN}		—	20	—	kΩ

1. The minimum slew rate on the XO applied to XO inputs is recommended to meet the specified jitter performance.
2. To achieve this slew rate and voltage swing, use one of the XOs from Si55xx/Si540x/Si536x Recommended XTALs Reference Manual, placed as close as possible to the XO input pins.
3. Slew rate can be estimated using the following simplified equation: SR = ((0.8 – 0.2) x VIN_VPP_se)/tr.
4. To meet specified jitter performance use one of the XTALs from Si55xx/Si540x/Si536x Recommended XTALs Reference Manual.
5. The minimum slew rate on the input clock applied to INx/INxb is recommended to meet the specified input-to-output delay and close-in phase noise (<1 kHz) performance.
6. Glitches and toggles on RSTb more frequent than fUR may cause the device to lock up in reset. Power cycle the device to restore operation.

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Table 10. I²C Timing Specifications (SCL, SDA)

V_{DD18} = 1.8 V ±5%, V_{DDA} = V_{DDXO} = 3.3 V ±5%. All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C
Low-Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDXO} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C

Parameter	Symbol	Test Condition	Standard Mode 100 kbps		Fast Mode 400kbps		Unit
			Min	Max	Min	Max	
SCL clock frequency	f_{SCL}		—	100	—	400	kHz
SMBus timeout	—		25	35	25	35	ms
Hold time (Repeated) start condition	$t_{HD:STA}$		4.0	—	0.6	—	µs
Low period of the SCL clock	t_{LOW}		4.7	—	1.3	—	µs
HIGH Period of the SCL clock	t_{HIGH}		4.0	—	0.6	—	µs
Setup time for a repeated start condition	$t_{SU:STA}$		4.7	—	0.6	—	µs
Data hold time	$t_{HD:DAT}$		100	—	100	—	ns
Data setup time	$t_{SU:DAT}$		250	—	100	—	ns
Setup time for stop condition	$t_{SU:STO}$		4.0	—	0.6	—	µs
Bus free time between a stop and start condition	t_{BUF}		4.7	—	1.3	—	µs
Data Valid Time	$t_{VD:DAT}$		—	3.45	—	0.9	µs
Data Valid Acknowledge Time	$t_{VD:ACK}$		—	3.45	—	0.9	µs

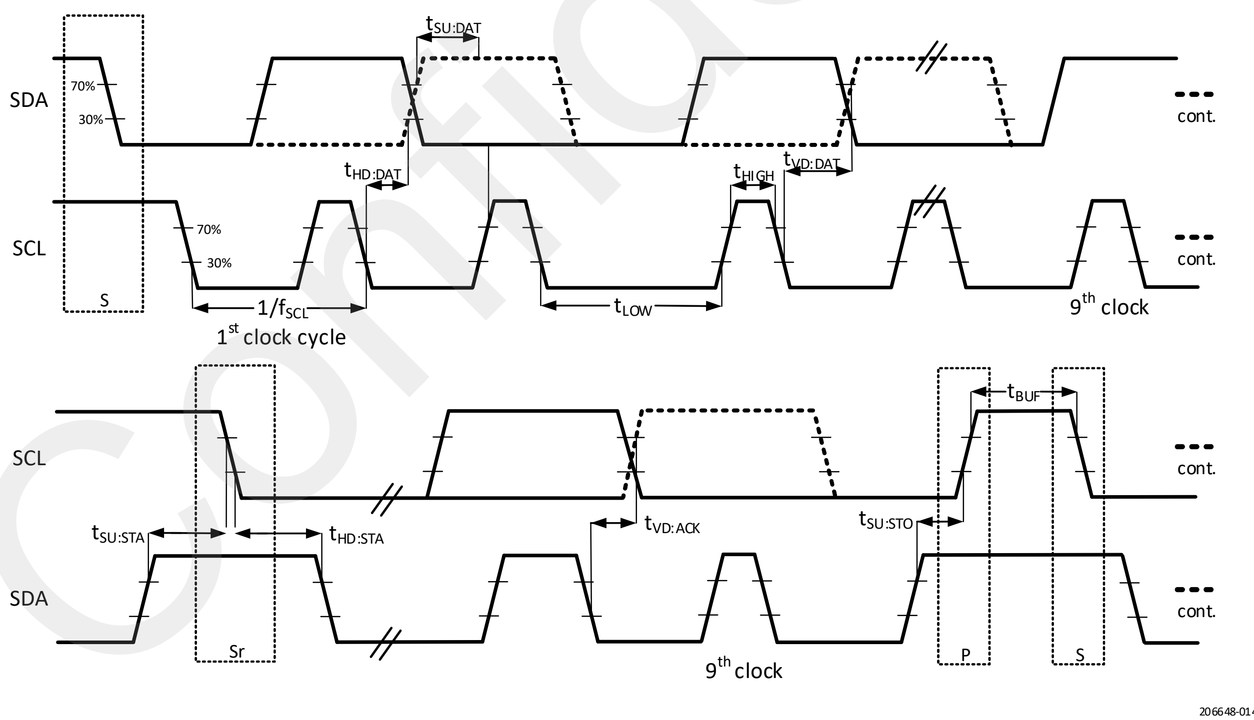

Figure 14. I²C Serial Port Timing Standard and Fast Modes

Table 11. SPI Timing Specifications (4-Wire)

V_{DD18} = 1.8 V ±5%, V_{DDA} = V_{DDXO} = 3.3 V ±5%. All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C
Low-Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDXO} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C

Parameter	Symbol	Min	Typ	Max	Unit
SCLK frequency	f_{SPI}	—	—	30	MHz
SCLK duty cycle	T_{DC}	40	—	60	%
SCLK period	T_C	33.333	—	—	ns
Delay time, SCLK fall to SDO active	T_{D1}	—	12.5	20	ns
Delay time, SCLK fall to SDO	T_{D2}	—	10	15	ns
Delay time, CSb rise to SDO tri-state	T_{D3}	—	10	20	ns
Setup time, CSb to SCLK	T_{SU1}	5	—	—	ns
Hold time, SCLK fall to CSb	T_{H1}	5	—	—	ns
Setup time, SDI to SCLK rise	T_{SU2}	5	—	—	ns
Hold time, SDI to SCLK rise	T_{H2}	5	—	—	ns
Delay time between chip selects (CSb)	T_{CS}	5	—	—	µs

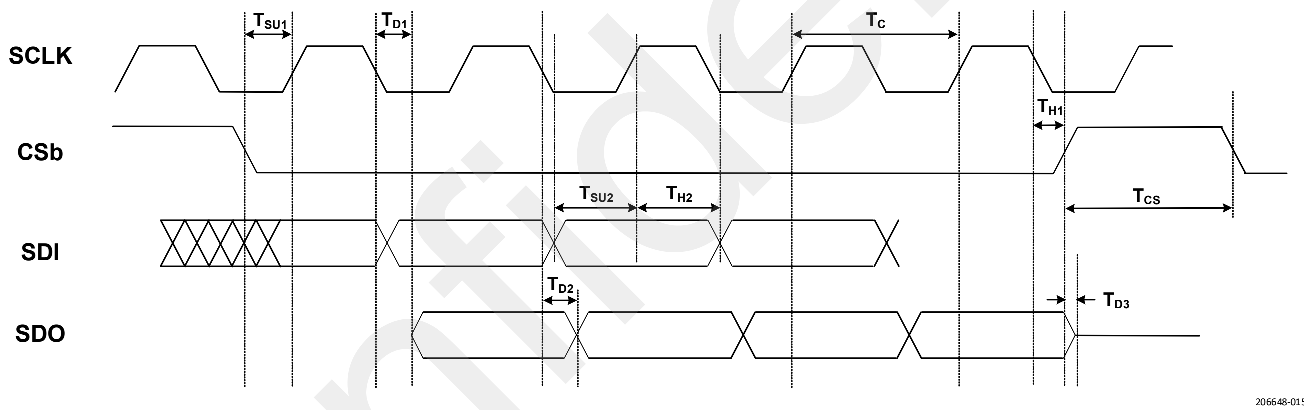

Figure 15. 4-Wire SPI Serial Interface Timing

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Table 12. SPI Timing Specifications (3-Wire)

V_{DD18} = 1.8 V ±5%, V_{DDA} = V_{DDXO} = 3.3 V ±5%. All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C

Low-Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDXO} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C

Parameter	Symbol	Min	Typ	Max	Unit
SCLK frequency	f_{SPI}	—	—	30	MHz
SCLK duty cycle	T_{DC}	40	—	60	%
SCLK period	T_C	33.333	—	—	ns
Delay time, SCLK fall to SDIO turn-on	T_{D1}	—	12.5	20	ns
Delay time, SCLK fall to SDIO next-bit	T_{D2}	—	10	15	ns
Delay time, CSb rise to SDIO tri-state	T_{D3}	—	10	20	ns
Setup time, CSb to SCLK	T_{SU1}	5	—	—	ns
Hold time, CSb to SCLK fall	T_{H1}	5	—	—	ns
Setup time, SDI to SCLK rise	T_{SU2}	5	—	—	ns
Hold time, SDI to SCLK rise	T_{H2}	5	—	—	ns
Delay time between chip selects (CSb)	T_{CS}	5	—	—	µs

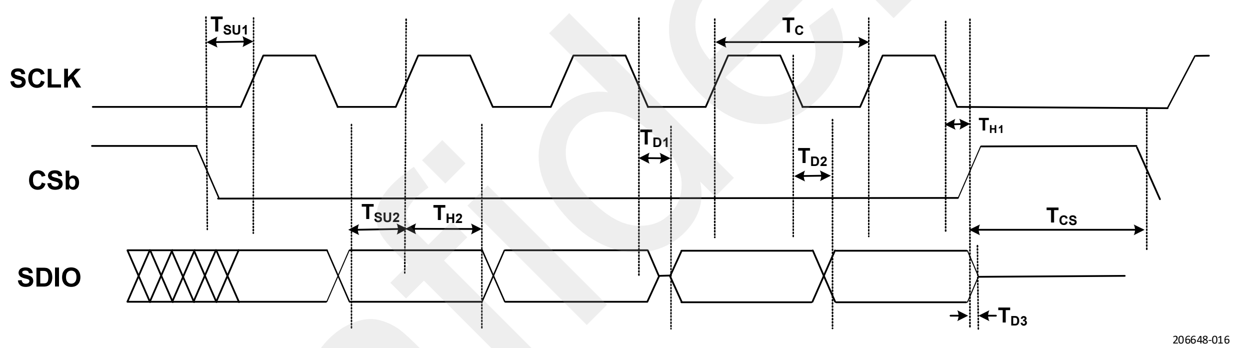

Figure 16. 3-Wire SPI Serial Interface Timing

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Table 13. Differential Clock Output Specifications

V_{DD18} = 1.8 V ±5%, V_{DDA} = V_{DDXO} = 3.3 V ±5%. All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C

Low-Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDXO} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output frequency	f_{OUT}	Q divider, non PPS[1]	0.008	—	1228.8	MHz
		Q divider, PPS	0.5	—	1	Hz
		NA divider, non PPS[2]	0.008	—	650	MHz
		NA divider, PPS	0.5	—	1	Hz
		NB divider[2]	0.008	—	650	MHz
Duty cycle	DC	f < 400 MHz	49.5	50	50.5	%
		400 MHz < f < 1228.8 MHz	48	50	52	
Output-to-output skew	T_{SK}	Q divider outputs, same differential format[3]	–50	—	50	ps
		MultiSynth (NA or NB) outputs, same differential format, same MultiSynth				
		Q divider outputs, differential SYSCLK to LVCMOS SYNC	0	—	300	
OUT-OUTb skew	T_{SK_OUT}	Skew between positive and negative output pins, VDDO = 3.3 V, LVPECL, LVDS, CML, and custom diff, f < 500 MHz	—	—	10	ps
		VDDO = 2.5 V, LVPECL, LVDS, CML, and custom diff, f < 500 MHz	—	—	25	
		VDDO = 3.3 V/2.5 V, LVPECL, LVDS, CML, and custom diff, f > 500 MHz	—	—	25	
		VDDO = 1.8 V, CML, S-LVDS, and custom diff, all frequencies	—	—	35	
Output voltage swing[4]	V_{OUT}	VDDO = 3.3 V/2.5 V, LVDS	330*SF	360*SF	380*SF	mVpp_se
		VDDO = 1.8 V, S-LVDS	350*SF	370*SF	410*SF	
		VDDO = 3.3 V/2.5 V, AC coupled LVPECL	780*SF	840*SF	910*SF	
		VDDO = 3.3 V/2.5 V/1.8 V, CML	390*SF	420*SF	460*SF	
		VDDO = 3.3 V/2.5 V, Custom diff 600 mVpp_se	560*SF	610*SF	650*SF	
Output voltage swing scaling factor (SF) OUT0-15	SF	f < 500 MHz	1	1	1	SF
		500 MHz < f < 1 GHz	0.9	0.95	1	
		1 GHz < f < 1.2288 GHz	0.8	0.9	1	
Output voltage swing scaling factor (SF) OUT0-17[5]	SF	f < 500 MHz	1	1	1	SF
		500 MHz < f < 1 GHz	0.9	0.95	1	
		1 GHz < f < 1.2288 GHz	0.8	0.9	1	
Common mode voltage	V_{CM}	VDDO = 3.3 V/2.5 V, LVDS, Custom Differential, CML	1.15	1.2	1.25	V
		VDDO = 1.8 V, S-LVDS, CML	0.85	0.9	0.95	
Rise and fall times (20% to 80%) OUT0-15	t_r/t_f	VDDO = 3.3 V/2.5 V, LVDS, AC coupled LVPECL, custom diff	—	125	260	ps
		VDDO = 1.8 V, S-LVDS	—	150	270	
		VDDO = 3.3 V/2.5 V/1.8 V, CML	—	150	280	
Rise and fall times (20% to 80%) OUT0-17[5]	t_r/t_f	VDDO = 3.3 V/2s.5 V, LVDS, AC coupled LVPECL, custom diff	—	140	300	ps
		VDDO = 1.8 V, S-LVDS	—	165	310	
		VDDO = 3.3 V/2.5 V/1.8 V, CML		165	320	

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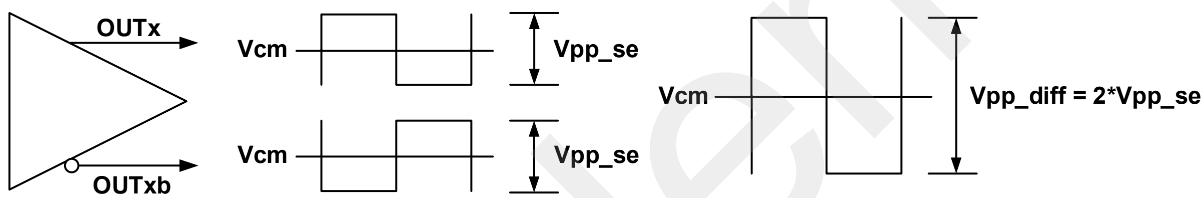
Table 13. Differential Clock Output Specifications (Continued)

V_{DD18} = 1.8 V ±5%, V_{DDA} = V_{DDXO} = 3.3 V ±5%. All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C
Low-Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDXO} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Differential output impedance	Z_O	All differential formats	—	100	—	Ω
Power supply noise rejection[6]	PSR	25 kHz sinusoidal noise	—	–94	—	dBc
		100 kHz sinusoidal noise	—	–95	—	
		500 kHz sinusoidal noise	—	–91	—	
		1 MHz sinusoidal noise	—	–91	—	
Output-to-output crosstalk[7]	$XTALK_{OUT}$	Differential outputs, same format	—	–95	—	dBc
input-to-output crosstalk[8]	$XTALK_{IN}$	Differential input and output, same format	—	–90	—	dBc

1. Q dividers support output frequencies within the specified range equal to fVCO/Q, where Q is an integer.
2. NA, NB MultiSynths support any output frequency within the specified range.
3. SYNC outputs are not included in this output-to-output skew specification.
4. Output voltage swing is dependent on frequency range. Scale all values by the scaling factor (SF). Voltage swing is specified in mVpp_SE as shown below.



5. OUT16/17 have programmable slew rate limit capability when configured as LVCMOS. This causes additional attenuation for higher frequency outputs. The output voltage swing scaling factor (SF) for OUT16/OUT17 is shown below. It is recommended to use OUT0-15 for fOUT > 500 MHz.
6. Measured for a 156.25 MHz output frequency. 100 mVpp sinewave noise added to VDDO = 3.3 V and noise spur amplitude measured.
7. Crosstalk spur measured with the victim running at 153.6 MHz and the aggressor at 156.25 MHz. Victim and aggressor are separated by two unused channels.
8. Crosstalk spur measured with the victim running at 153.6 MHz on OUT0 and the aggressor at 156.25 MHz on IN3.

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Table 14. HCSL Clock Output Specifications

VDD18 = 1.8 V ±5%, VDDIN = VDDIO = 3.3 V ±5%, 1.8 V ±5%, VDDREF = VDDA = 3.3 V ±5%,
VDDO = 3.3V ±5%, 2.5V ±5%, 1.8 V ±5% TA = –40 to 95 °C
Low-Power Mode: VDD18 = VDDIN = VDDIO = VDDREF = VDDA = VDDO = 1.8 V ±5%, TA = –40 to 95 °C

Parameter	Symbol	Test Condition			Min	Typ	Max	Unit
Output frequency	f_{OUT}	Q divider, non PPS[1]			0.008	—	500	MHz
		Q divider, PPS			0.5	—	1	Hz
		NA divider, non PPS[2]			0.008	—	500	MHz
		NA divider, PPS			0.5	—	1	Hz
		NB divider[2]			0.008	—	500	MHz
Duty cycle	DC	f < 400 MHz			49.5	50	50.5	%
		400 MHz < f < 500 MHz			48	50	52	
Output-to-output skew	T_{SK}	Q divider outputs, same differential format[3]			–50	—	50	ps
		MultiSynth (NA or NB) outputs, same differential format, same MultiSynth						
		Q divider outputs, differential SYSCLK to LVCMOS SYNC output			0	—	300	
OUT-OUTb skew	T_{SK_OUT}	Skew between positive and negative output pins	VDDO = 3.3 V	HCSL Standard, 800 mVpp_se, int term	—	—	15	ps
				HCSL Standard, 800 mVpp_se, ext term	—	—	25	
				HCSL Fast, 800mV or 1200mV, ext term	—	—	10	
			VDDO = 2.5 V	HCSL Standard, 800 mVpp_se, int term	—	—	15	
				HCSL Standard, 800 mVpp_se, ext term	—	—	30	
				HCSL Fast, 800mV or 1200mV, ext term	—	—	20	
			VDDO = 1.8 V	HCSL Standard, 800 mVpp_se, int term	—	—	22	
				HCSL Standard, 800 mVpp_se, ext term	—	—	70	
				HCSL Fast, 800mV, ext term	—	—	36	
Output voltage swing[4]	V_{OUT}	VDDO = 3.3 V/2.5 V/1.8 V	HCSL Standard, 800 mVpp_se, int term		740*SF	810*SF	960*SF	mVpp_se
		VDDO = 3.3 V/2.5 V/1.8 V	HCSL Standard, 800 mVpp_se, ext term		730*SF	810*SF	960*SF	
		VDDO = 3.3 V/2.5 V	HCSL Fast, 800 mVpp_se, ext term		730*SF	810*SF	960*SF	
		VDDO = 3.3 V/2.5 V	HCSL Fast, 1200 mVpp_se, ext term		1100*SF	1175*SF	1260*SF	
Output voltage swing scaling factor (SF) Standard, 800mVpp_se, int term, OUT0-17	SF	f < 10 MHz			1	1	1	SF
		10 MHz < f < 100 MHz			0.91	0.94	0.95	
		10 0MHz < f < 200 MHz			0.89	0.91	0.93	
		20 0MHz < f < 400 MHz			0.83	0.85	0.92	
		f > 400 MHz			0.74	0.78	0.89	

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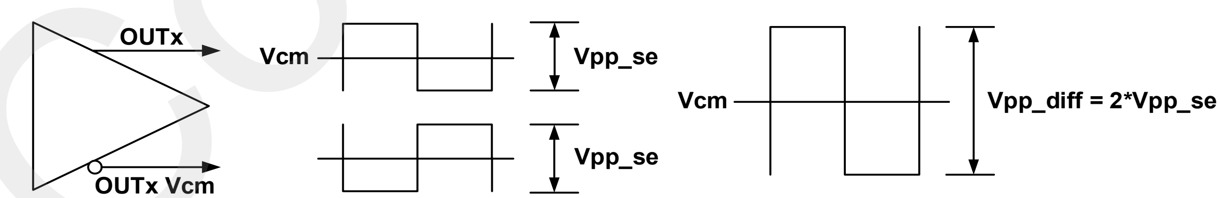
Table 14. HCSL Clock Output Specifications (Continued)

VDD18 = 1.8 V ±5%, VDDIN = VDDIO = 3.3 V ±5%, 1.8 V ±5%, VDDREF = VDDA = 3.3 V ±5%,
VDDO = 3.3V ±5%, 2.5V ±5%, 1.8 V ±5% TA = –40 to 95 °C
Low-Power Mode: VDD18 = VDDIN = VDDIO = VDDREF = VDDA = VDDO = 1.8 V ±5%, TA = –40 to 95 °C

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Output voltage swing scaling factor (SF) Standard, 800mVpp_se, ext term, OUT0-17	SF	f < 10 MHz		1	1	1	SF
		10 MHz < f < 100 MHz		0.97	0.96	0.97	
		10 0MHz < f < 200 MHz		0.94	0.93	0.95	
		20 0MHz < f < 400 MHz		0.91	0.90	0.88	
		f > 400 MHz		0.68	0.71	0.75	
Output voltage swing scaling factor (SF), Fast, 800mVpp_se, ext term, OUT0-17	SF	f < 10 MHz		1	1	1	SF
		10 MHz < f < 100 MHz		0.98	0.99	0.99	
		10 0MHz < f < 200 MHz		0.94	0.94	0.96	
		20 0MHz < f < 400 MHz		0.94	0.95	0.97	
		f > 400 MHz		0.89	0.92	0.95	
Common mode voltage	V_{CM}	VDDO = 3.3 V/2.5 V/1.8 V	HCSL 800 mVpp_se	0.35	0.425	0.52	V
		VDDO = 3.3 V/2.5 V	HCSL 1200 mVpp_se	0.55	0.6	0.68	
Rise and fall times (20% to 80%) OUT0-15	t_r/t_f	VDDO = 3.3 V/2.5 V/1.8 V	HCSL Fast, 800 or 1200 mVpp_se, ext term	—	270	360	ps
		VDDO = 3.3 V/2.5 V/1.8 V	HCSL Standard, 800mVpp_se, ext term	—	450	700	
		VDDO = 3.3 V/2.5 V/1.8 V	HCSL Standard, 800mVpp_se, int term	—	270	420	
Rise and fall times (20% to 80%) OUT0-16-17[5]	t_r/t_f	VDDO = 3.3 V/2.5 V/1.8 V	HCSL Fast, 800 or 1200 mVpp_se, ext term	—	285	400	ps
		VDDO = 3.3 V/2.5 V/1.8 V	HCSL Standard, 800mVpp_se, ext term	—	465	740	
		VDDO = 3.3 V/2.5 V/1.8 V	HCSL Standard, 800mVpp_se, int term		285	460	
Differential output impedance	Z_O	HCSL Standard Slew Rate, int term		—	100	—	Ω
		HCSL Standard Slew Rate, ext term		—	Hi-Z	—	
		HCSL Fast Slew Rate, ext term		—	200	—	
Output-to-output crosstalk[6]	$XTALK_{OUT}$	HCSL outputs, same format		—	–95	—	dBc
input-to-output crosstalk[7]	$XTALK_{IN}$	HCSL input and output, same format		—	–90	—	dBc

1. Q dividers support output frequencies within the specified range equal to fVCO/Q, where Q is an integer.
2. NA, NB MultiSynths support any output frequency within the specified range.
3. SYNC outputs are not included in this output-to-output skew specification.
4. Output voltage swing is dependent on frequency range, HCSL slew rate, and HCSL termination settings. Scale all values by the scaling factor (SF). Voltage swing is specified in mVpp_SE as shown below.



5. OUT16/17 have programmable slew rate limit capability when configured as LVCMOS. This causes additional attenuation for higher frequency outputs. The output voltage swing scaling factor (SF) for OUT16/OUT17 is shown below. It is recommended to use OUT0-15 for fOUT > 491.52 MHz.
6. Crosstalk spur measured with the victim running at 153.6 MHz and the aggressor at 156.25 MHz. Victim and aggressor are separated by two unused channels.
7. Crosstalk spur measured with the victim running at 153.6 MHz on OUT0 and the aggressor at 156.25 MHz on IN3.

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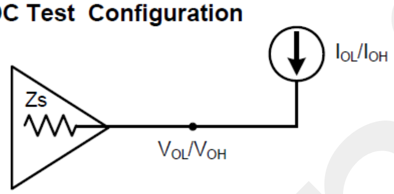
Table 15. LVCMOS Clock Output Specifications

V_{DD18} = 1.8 V ±5%, V_{DDA} = V_{DDXO} = 3.3 V ±5%. All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C
Low-Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDXO} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C

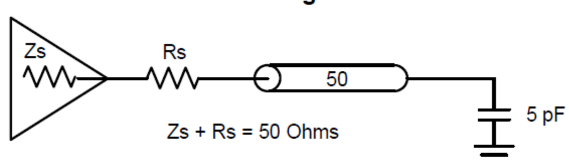
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output frequency	f_{OUT}	Q divider, non PPS[1]	0.008	—	250	MHz
		Q divider, PPS[1]	0.5	—	1	Hz
		NA divider, non PPS[2]	0.008	—	250	MHz
		NA divider, PPS	0.5	—	1	Hz
		NB divider[2]	0.008	—	250	MHz
Duty cycle	DC	f < 100 MHz	49.5	—	50.5	%
		100 MHz < f < 250 MHz	45	—	55	
Output voltage high[3]	V_{OH}	V_{DDO} = 3.3 V/2.5 V/1.8 V I_{OH}= –8/–6/–4 mA I_{OL} = 8/6/4 mA	V_{DDO} x 0.85	—	—	V
Output voltage low[3]	V_{OL}		—	—	V_{DDO} x 0.15	V
Rise and fall times (20% to 80%)[4,5,6]	t_r/t_f	LVCMOS	0.35	0.8	1.35	ns
		SRL LVCMOS "4 ns rise/fall"	3	4	6	
		SRL LVCMOS "6.5 ns rise/fall"	4	6.5	10	
		SRL LVCMOS "13 ns rise/fall"	7	13	24	
		SRL LVCMOS "25 ns rise/fall"	13	25	42	

1. Q dividers support output frequencies within the specified range equal to fVCO/Q where Q is an integer.
2. NA, NB MultiSynths support any output frequency within the specified range.
3. V_{OL} /V_{OH} is measured at IOL /IOH as shown in the DC Test Configuration.
4. A 15 to 25 Ω series termination resistor (RS) is recommended to help match the source impedance to a 50 Ω PCB trace. A 5 pF capacitive load is assumed as shown in the AC test configuration.

DC Test Configuration



AC Test Configuration



5. Slew rate limited (SRL) LVCMOS format is only available on specific outputs. For information on which outputs support SRL, see Table 19, Si5403 Pin Descriptions, Table 20, Si5402 Pin Descriptions, or Table 21, Si5401 Pin Descriptions.
6. SRL LVCMOS format clocks are intended only for low frequency clock applications. Refer to the Si540x NetSync™ Reference Manual for the maximum Fout supported for each slew rate selection.

Table 16. Output Status Pin Specifications

V_{DDIO} = 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C
Low-Power Mode: V_{DDIO} = 1.8 V ±5%

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Serial and Status Output Pins (GPIO, SDA/SDIO, SDO)						
Output voltage high	V_{OH}[1]	I_{OH} = –2 mA	V_{DDIO} x 0.85	—	—	V
Output voltage low	V_{OL}	I_{OL} = 2 mA	—	—	V_{DDIO} x 0.15	V

1. The V_{OH} specification does not apply to the open-drain SDA output when the serial interface is in I^2C mode. V_{OL} remains valid in all cases.

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Table 17. Performance Characteristics

V_{DD18} = 1.8 V ±5%, V_{DDA} = V_{DDXO} = 3.3 V ±5%. All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C

Low-Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDXO} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Initial start up time	t_{START}	Time from POR to when the device generates free running clocks from NVM frequency plan	—	25	40	ms
	t_{RDY}	POR to API ready	—	25	30	
PLL lock time	t_{ACQ_DSPLL}[1]	REFPLL, IN = 19.44 MHz, BW = 100 Hz, FLOL deassert	—	230	350	ms
		REFPLL, IN = 19.44 MHz, BW = 100 Hz, LOL deassert	—	1.3	1.6	s
		DSPLLA/B, IN = 156.25 MHz, BW = 3 Hz, FLOL deassert	—	190	240	ms
		DSPLLA/B, IN = 156.25 MHz, BW = 3 Hz, LOL deassert	—	1.3	1.6	s
	t_{ACQ_PPS}[2]	PPSPLL, IN = 1PPS, BW = 12.5 mHz, coarse LOL deassert	—	23	25	s
		PPSPLL, IN = 1PPS, BW = 12.5 mHz, fine LOL deassert	—	31	33	
		PPSPLL, IN = PP2S, BW = 12.5 mHz, coarse LOL deassert	—	53	56	
		PPSPLL, IN = PP2S, BW = 12.5 mHz, fine LOL deassert	—	69	72	
Output delay adjustment	t_{QDIV}	Range[3]	–TVCO x 127	—	+TVCO x 127	ps
		Resolution		T_{VCO}	—	
		Resolution - fine delay enabled		$T_{VCO}/4$	—	
Jitter peaking	J_{PK}	All PLLs	—	—	0.1	dB
Max phase transient during hitless switch[4]	t_{SWITCH}		—	35	150	ps
Pull-in range	ω_P		—	±100	—	ppm
Input-to-output delay + variation[5, 6]	$t_{IODELAY}$	DSPLLA[7]	–400	—	400	ps
	t_{ZDELAY}	ZDM: 1PPS, PP2S	–200	—	200	
		ZDM: fIN > 8 kHz	–100	—	100	
Input-to-output delay variation[8]	$t_{VIODELAY}$	DSPLLB (Si5402 and 03 only)	–500	—	500	ps
Si5401/02/03 DSPLLA RMS Jitter Performance 12 kHz to 20 MHz[9,10]	Qdiv	644.53125 MHz	—	51	75	fs
		390.625 MHz	—	52	75	
		322.265625 MHz	—	52	75	
		312.5 MHz	—	53	75	
		156.25 MHz	—	58	80	
		125 MHz	—	60	85	
	NA/NB Div	125 MHz	—	95	145	
		100 MHz	—	95	135	
		25/50 MHz	—	200	255	
		322.265625 MHz	—	80	95	
		390.625 MHz	—	82	95	
		644.53125 MHz	—	67	80	
Si5402/03 DSPLLB RMS Jitter Performance 12 kHz to 20 MHz[9,10]	NA/NB Div	322.265625 MHz	—	135	210	fs

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1. FLOL deasserts once frequency lock is achieved. LOL deasserts once both frequency and phase lock are achieved. Refer to 3.13.2. Lock Acquisition Mode for more details on LOL thresholds.
2. PPSPLL lock time specified for frequency plans with a greatest common divisor of SYSCLK frequencies greater than or equal to 960 kHz. Coarse lock is declared once the PPSPLL has steered the output phase to within 500 ns of the input phase. Fine lock is declared when the output phase is within 30 ns of the input phase. For more details on PPSPLL lock times, see Si540x NetSync™ Reference Manual.
3. Output delay adjustment range will vary depending on frequency plan. Output delay adjust range (ns) is displayed in the **Output Skew Control** step of the ClockBuilder Pro Wizard. FVCO range is 10.4 GHz to 13 GHz.
4. Phase transient specification only applies to clock switches between two synchronous inputs to a DSPLL configured for a phase buildout clock switching mode in ClockBuilder Pro.
5. Input-to-output delay is measured at the output driver with respect to the input after the output phase has achieved a steady state value. This spec excludes wander from the OCXO/TCXO.
6. IO delay requires clock switching to be configured for phase pull-in within ClockBuilder Pro. IO delay is not specified for phase buildout (hitless) clock switching mode.
7. Input-to-output delay in these modes is only specified for outputs derived from Q dividers or the NA divider.
8. Only IO delay variation is specified for these DSPLL configurations. Absolute delay is dependent on frequency plan.
9. Added jitter and spurs due to crosstalk is frequency-plan-dependent and can be determined using the ClockBuilder Pro Spur Analysis tool.
10. Jitter generation conditions: XTAL = 54 MHz TXC 7M54072006, fIN = 156.25 MHz, LVPECL output format, REFPLL BW = 100 Hz, DSPLLA BW = 2 Hz, DSPLLB BW = 2 Hz.

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5. Standards Compliance

DSPLLA, DSPLLB, and PPSPLL can be configured to support the requirements of the ITU-T standards shown in the following table.

Table 18. Supported ITU-T Standards

ITU-T Standard	Option	Comment
G.8262	EEC Option 1	SDH. SyncE. Based on G.813 Option 1
	EEC Option 2	SDH. SyncE. Based on G.812 Type IV
G.8262.1	eEEC	Enhanced SyncE
G.8273.1	N/A	Grandmaster T-GM
G.8273.2	N/A	Supported with and without SyncE. T-TSC and T-BC
G.8273.4	N/A	Assisted Partial Timing Support (APTS). T-TSC-A and T-TBC-A

6. Typical Operating Characteristics

The figures below show the typical phase noise and jitter performance for the Si540x. The phase noise plots were taken under the following conditions: f_{IN} = 156.25 MHz, LVPECL output format, REF PLL BW = 40 Hz, XTAL = 54 MHz TXC 7M54072006, T_A= 25 °C. Phase noise performance is shown for clocks derived from the Q divider as well as the NA/NB MultiSynths.

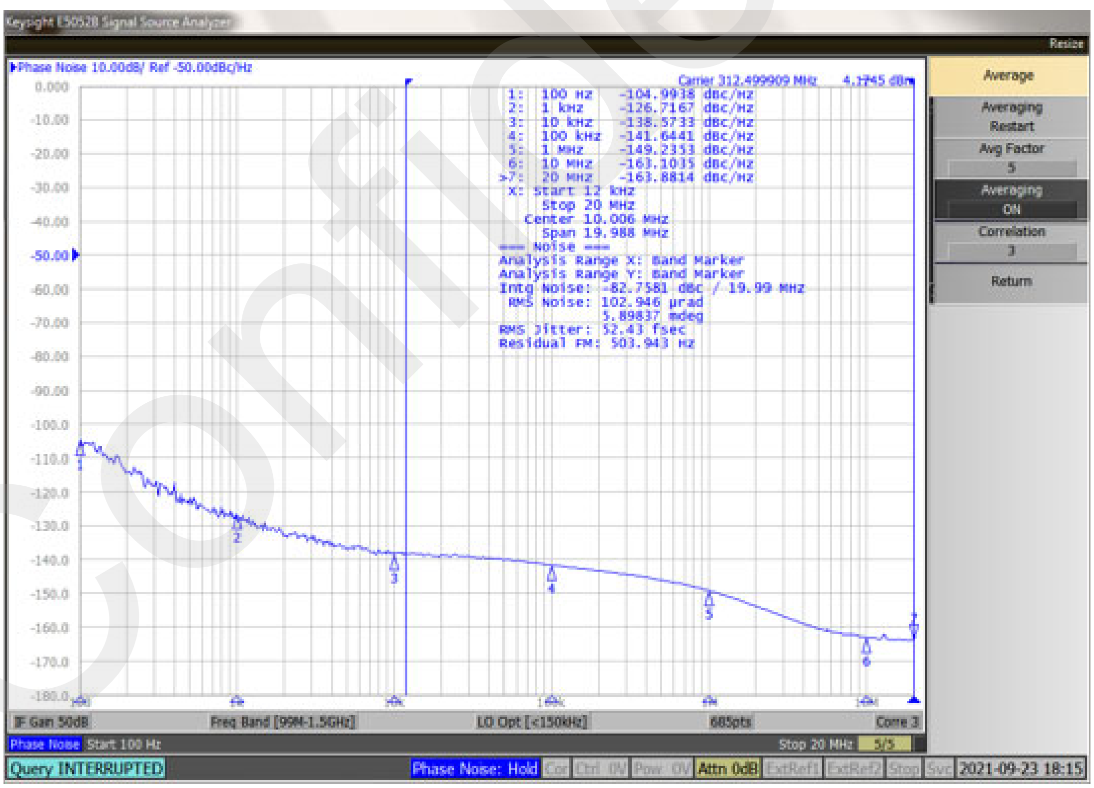

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Figure 17. XTAL Configuration, fIN = 156.25 MHz, fout = 312.5 MHz, Q Divider

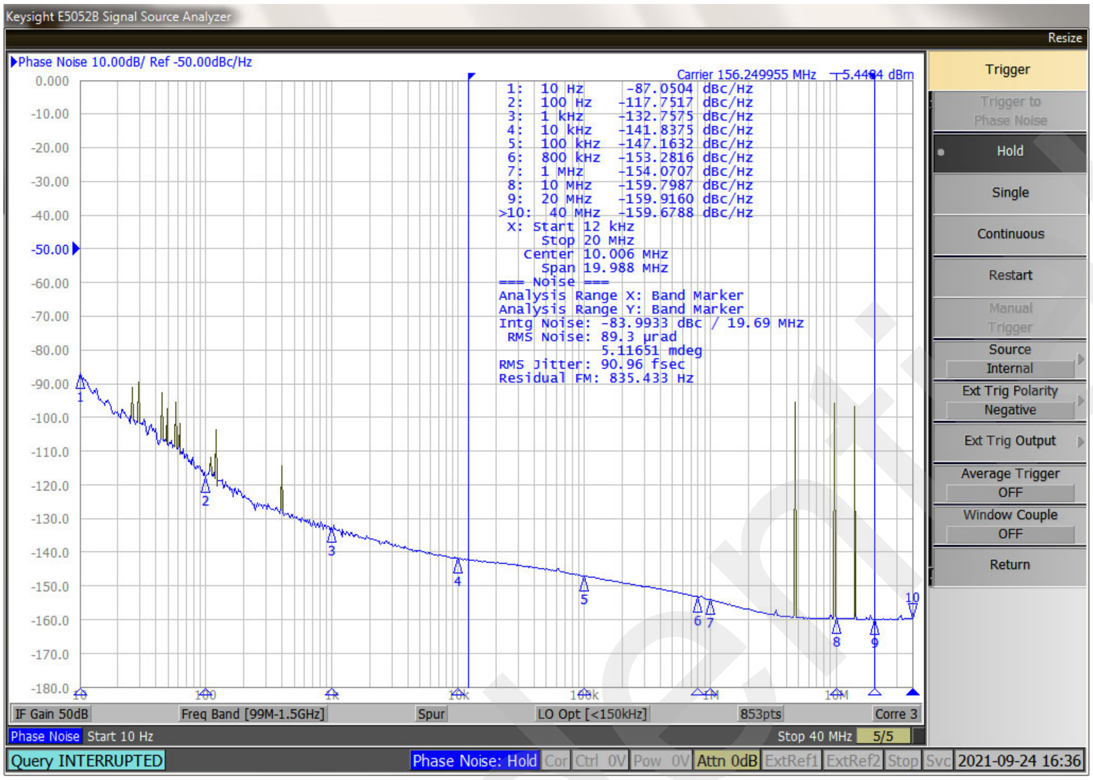

Figure 18. XTAL Configuration, f_{IN} = 156.25 MHz, f_{out} = 156.25 MHz, MultiSynth NA or NB

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7. Pin Descriptions

7.1. Si5403 Pin Descriptions

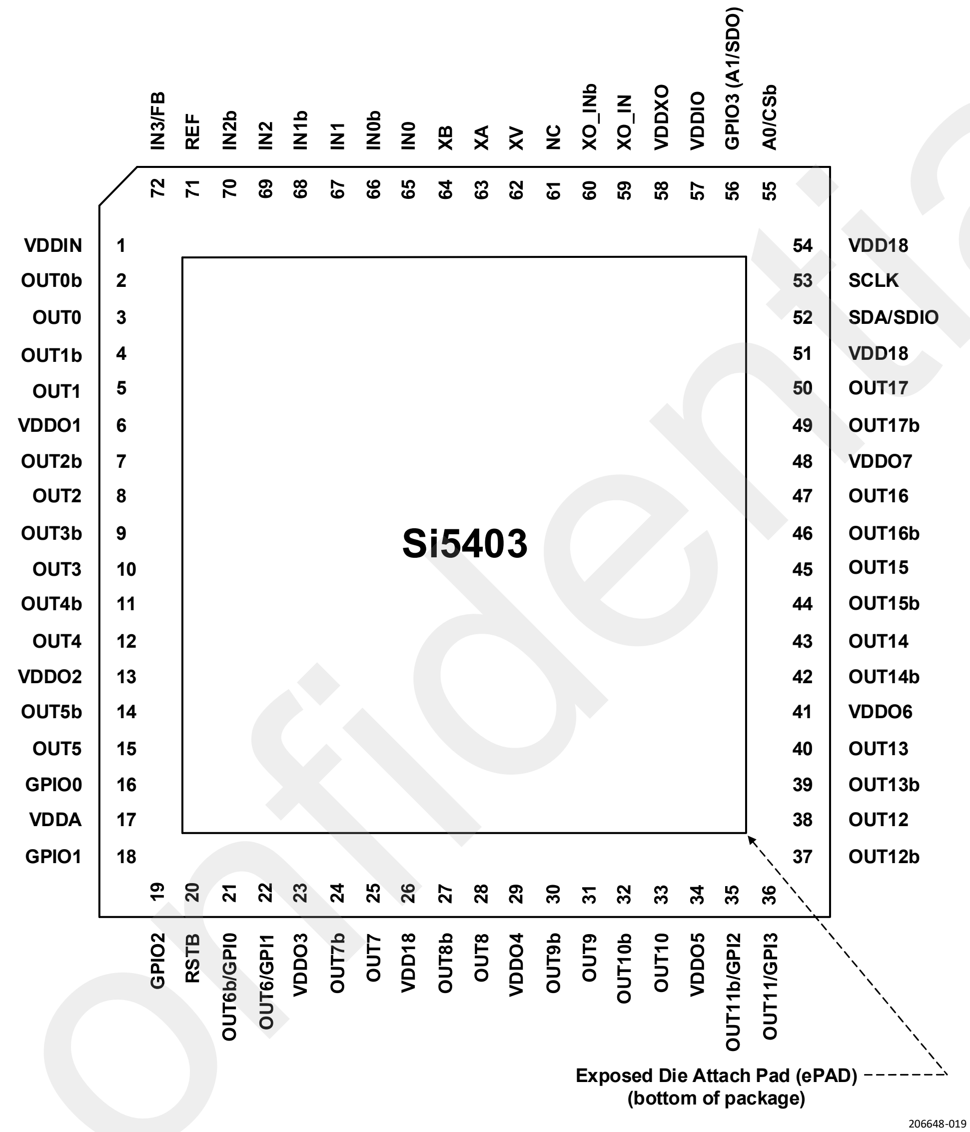

Figure 19. Si5403 Pinout

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Table 19. Si5403 Pin Descriptions

Pin Name	Pin Number	Pin Type[1]	Description
Inputs			
XO_IN	59	I	Input for inner loop crystal oscillator (XO) option.
XO_INb	60		
XV	62	I	**XTAL shield:** Connect this pin directly to the XTAL ground pins. Do not ground the XV pin. XV should be isolated from the PCB ground plane. See AN1347: Si540x Schematic Design and Board Layout Guidelines for layout guidelines.
XA	63	I	**Crystal input:** Input pins for external crystal (XTAL). XA and XB pins can be left unconnected when not in use.
XB	64		
REF	71	I	**Reference input:** Only used for TCXOs or OCXOs with single-ended outputs.
IN0	65	I	**Clock inputs:** IN0–IN3/FB accept an input clock for synchronizing the device. IN0–IN2 support both differential and single-ended clock signals. Input IN3/FB only supports a single-ended (SE) mode and can be used for Zero Delay Mode (ZBM) feedback (FB). When input IN2 is operating in single-ended mode it can provide two SE inputs each for a total of five customer-definable inputs. These pins are high-impedance and must be terminated externally. IN0–IN3/FB can be disabled in ClockBuilder Pro and the pins left unconnected if unused. Refer to the Si540x NetSync™ Reference Manual and AN1347: Si540x Schematic Design and Board Layout Guidelines for input termination options and more information on ZDM.
IN0b	66		
IN1	67		
IN1b	68		
IN2	69		
IN2b	70		
IN3/FB	72		
Outputs			
OUT0b	2	O	**Output clocks:** The output clocks can be programmed as single-ended CMOS or differential LVDS, S-LVDS, CML, HCSL or ac-coupled LVPECL and support a programmable signal amplitude and common-mode voltage. Desired output signal format is configurable in ClockBuilder Pro. Termination recommendations are provided in the Si540x NetSync™ Reference Manual and AN1347: Si540x Schematic Design and Board Layout Guidelines. Unused outputs should be left unconnected.
OUT0	3		
OUT1b	4		
OUT1	5		
OUT2b	7		
OUT2	8		
OUT3b	9		
OUT3	10		
OUT4b	11		
OUT4	12		
OUT5b	14		
OUT5	15		
OUT6b/GPI0	21	I or O	**Output clocks with input option:** Output 6 can alternatively be assigned as two general purpose inputs (GPI0/GPI1) that can be programmed to have any of the input control functions listed in 3.11. GPIO Pins. Regardless of whether Output 6 is functioning as a clock output or GPI, the power supply will be VDDO3.
OUT6/GPI1	22		
OUT7b	24	O	**Output clocks:** The output clocks can be programmed as single-ended CMOS or differential LVDS, S-LVDS, CML, HCSL or ac-coupled LVPECL and support a programmable signal amplitude and common-mode voltage. Desired output signal format is configurable in ClockBuilder Pro. Termination recommendations are provided in the Si540x NetSync™ Reference Manual and AN1347: Si540x Schematic Design and Board Layout Guidelines. Unused outputs should be left unconnected.
OUT7	25		
OUT8b	27		
OUT8	28		
OUT9b	30		
OUT9	31		
OUT10b	32		
OUT10	33		

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Table 19. Si5403 Pin Descriptions (Continued)

Pin Name	Pin Number	Pin Type[1]	Description
OUT11b/GPI2	35	I or O	**Output clocks with input option:** Output 11 can alternatively be assigned as two General Purpose Inputs (GPI2/GPI3) that can be programmed to have any of the input control functions listed in Table 2, GPIO Pin Descriptions. Regardless of whether Output 11 is functioning as a clock output or GPI, the power supply will be VDDO5.
OUT11/GPI3	36		
OUT12b	37	O	**Output clocks:** The output clocks can be programmed as single-ended CMOS or differential LVDS, S-LVDS, CML, HCSL or ac-coupled LVPECL and support a programmable signal amplitude and common-mode voltage. Desired output signal format is configurable in ClockBuilder Pro. Termination recommendations are provided in the Si540x NetSync™ Reference Manual and AN1347: Si540x Schematic Design and Board Layout Guidelines**.** Unused outputs should be left unconnected.
OUT12	38		
OUT13b	39		
OUT13	40		
OUT14b	42		
OUT14	43		
OUT15b	44		
OUT15	45		
OUT16b	46	O	**Output clocks with programmable slew rate limiting (SRL):** When outputs 16 and 17 are configured as CMOS outputs, they can also have the slew rate adjusted.
OUT16	47		
OUT17b	49		
OUT17	50		
Serial Interface			
SDA/SDIO	52	I/O	**Serial data interface:** This is the bidirectional data pin (SDA) for the I^2C mode, or the bidirectional data pin (SDIO) in the 3-wire SPI mode, or the input data pin (SDI) in the 4-wire SPI mode. When in I^2C mode, this pin must be pulled-up using an external resistor of at least 1 kΩ. No pull-up resistor is needed when in SPI mode.
SCLK	53	I	**Serial clock input:** This pin functions as the serial clock input for both I2C and SPI modes. When in I2C mode, this pin must be pulled-up using an external resistor of at least 1 kΩ. No pull-up resistor is needed when in SPI mode.
A0/CSb	55	I	**Address select 0/chip select:** This pin functions as the hardware controlled lsb of the device address (A0) in I^2C mode. In SPI mode, this pin functions as the chip select input (active low). This pin is internally pulled-up and can be left floating if unused.
GPIO3 (A1/ SDO)	56	O	**Address select 1/ serial data output/GPIO3:** This input pin operates as the hardware controlled next to lsb portion of the device address (A1) in I^2C mode. In 4-wire SPI mode this pin operates as the serial data output (SDO). In 3-wire SPI mode this pin can function as an additional GPIO pin (GPIO3).
Control/Status			
GPIO0	16	I or O	**Programmable general purpose input or outputs:** These pins can be programmed to the functions defined in Table 2, GPIO Pin Descriptions.
GPIO1	18		
GPIO2	19		
RSTb	20	I	**Reset pin:** This pin functions as an active-low reset input and is used to generate a device reset when held low for at least the specified Minimum Pulse Width. This resets the device back to a known state and reloads the NVM frequency plan and application. All clocks will stop while the RSTb pin is asserted. If there is no frequency plan in NVM, the reset pin will return the device to the bootloader state in which it is waiting for the frequency plan and application to be downloaded by the host controller. This pin accepts a CMOS input and is internally pulled up with a ~20 kΩ resistor to VDDIO. VDDA and VDD18 must be powered up and stable before releasing RSTb. RSTb must not be toggled faster than the maximum update rate (fUR) specification. Please refer to AN1347: Si540x Schematic Design and Board Layout Guidelines for more details on RSTb pin circuitry.

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Table 19. Si5403 Pin Descriptions (Continued)

Pin Name	Pin Number	Pin Type[1]	Description
Power			
VDDIN	1	P	**Input clock supply voltage:** Supply voltage 3.3 V, 2.5 V or 1.8 V for the input clock buffers.
VDDO1	6	P	**Output clock supply voltage 1 to 7:** Supply voltage 3.3 V, 2.5 V, or 1.8 V for outputs. Leave VDDO pins of unused output drivers unconnected. An alternate option is to connect the VDDO pin to a power supply and disable the output driver to minimize current consumption. An 0402 1 µF "decoupling" capacitor should be placed very close to each of these pins. VDDO may not exceed VDDA. The banks of outputs are powered as follows: VDDO1 - OUT[0:3] VDDO2 - OUT[4:5] VDDO3 - OUT[6:7] VDDO4 - OUT[8:9] VDDO5 - OUT[10:11] VDDO6 - OUT[12:15] VDDO7 - OUT[16:17] Data sheet jitter performance requires all outputs in a given bank to operate at a single frequency.
VDDO2	13		
VDDO3	23		
VDDO4	29		
VDDO5	34		
VDDO6	41		
VDDO7	48		
VDDA	17	P	**Core analog supply voltage:** This core supply can operate from a 3.3 V or 1.8 V power supply for Low-Power Mode. Note that all other supply voltages must be equal or lower voltage than the VDDA pin; so, in Low-Power Mode, no other supply can exceed 1.8 V. A 0402 1 µF capacitor should be placed very close to each of these pins.
VDD18	26	P	**Core supply voltage 1.8 V:** The device core operates from a 1.8 V supply. A 0402 1 µF capacitor should be placed very close to each of these pins.
VDD18	51	P	
VDD18	54	P	
VDDIO	57	P	**Control, status IO clock supply voltage:** Supply voltage 3.3 V, 2.5 V, or 1.8 V for the serial interface, Control, and Status inputs and outputs.
VDDXO	58	P	**XTAL/external oscillator (XO) supply voltage:** Supply voltage of 3.3 V or 1.8 V supported for the reference. For best performance, VDDXO should be the same voltage and power source that is applied to the external oscillator (XO).
GND	Package Bottom	P	**Exposed die attach pad:** The exposed die attach pad (ePAD) on the bottom of the package should be connected to electrical ground.
No Connect			
NC	61	NC	No connection

1. I = Input; O = Output; P = Power; NC = No Connection; GND = Ground.

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7.2. Si5402 Pin Descriptions

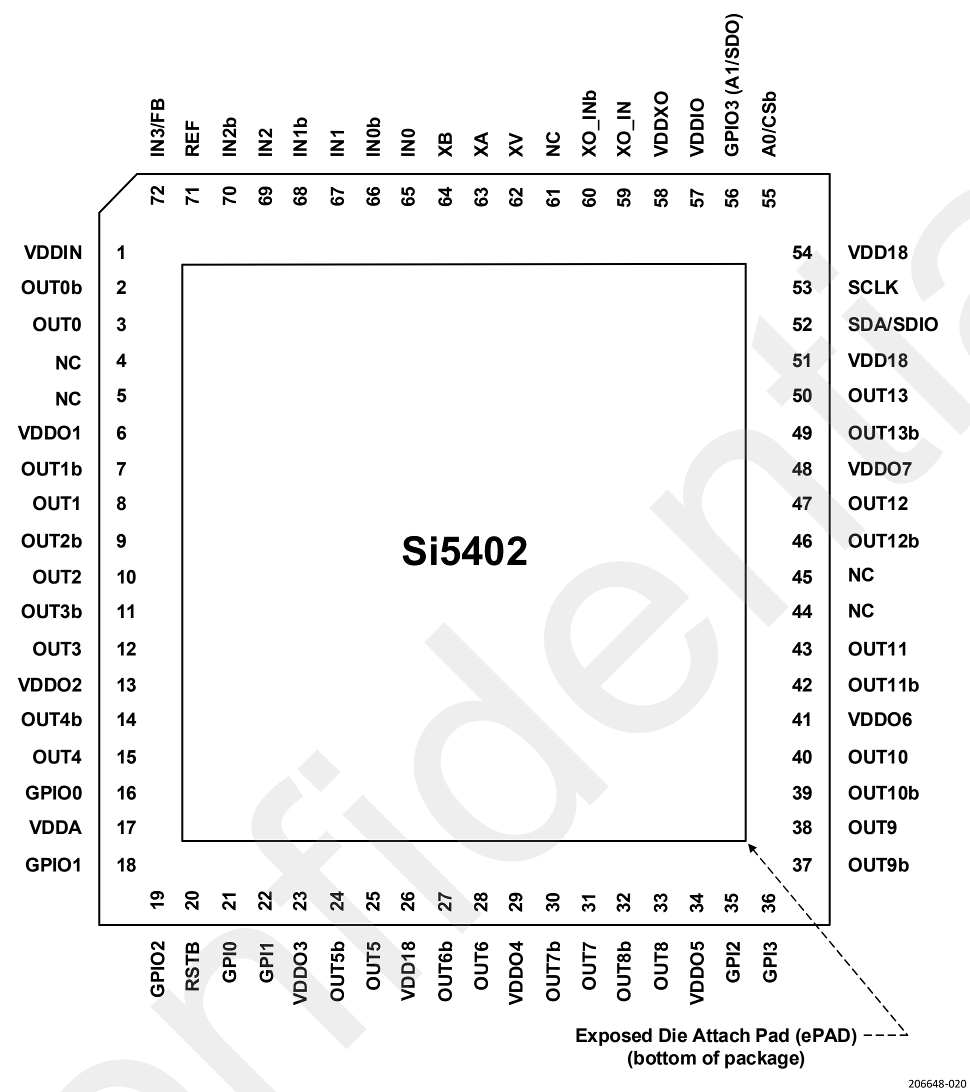

Figure 20. Si5402 Pinout

Table 20. Si5402 Pin Descriptions

Pin Name	Pin Number	Pin Type[1]	Description
Inputs			
XO_IN	59	I	Input for inner loop crystal oscillator (XO) option.
XO_INb	60		
XV	62	I	**XTAL shield:** Connect this pin directly to the XTAL ground pins. Do not ground the XV pin. XV should be isolated from the PCB ground plane. See AN1347: Si540x Schematic Design and Board Layout Guidelines for layout guidelines.
XA	63	I	**Crystal input:** Input pins for external crystal (XTAL). XA and XB pins can be left unconnected when not in use.
XB	64		
REF	71	I	**Reference input:** Only used for TCXOs or OCXOs with single-ended outputs.
IN0	65	I	**Clock inputs:** IN0–IN3/FB accept an input clock for synchronizing the device. IN0–IN2 support both differential and single-ended clock signals. Input IN3/FB only supports a single-ended (SE) mode and can be used for Zero Delay Mode (ZBM) feedback (FB). When input IN2 is operating in single-ended mode it can provide two SE inputs each for a total of five customer-definable inputs. These pins are high-impedance and must be terminated externally. IN0–IN3/FB can be disabled in ClockBuilder Pro and the pins left unconnected if unused. Refer to the Si540x NetSync™ Reference Manual and AN1347: Si540x Schematic Design and Board Layout Guidelines for input termination options and more information on ZDM.
IN0b	66		
IN1	67		
IN1b	68		
IN2	69		
IN2b	70		
IN3/FB	72		
Outputs			
OUT0b	2	O	**Output clocks:** The output clocks can be programmed as single-ended CMOS or differential LVDS, S-LVDS, CML, HCSL or ac-coupled LVPECL and support a programmable signal amplitude and common-mode voltage. Desired output signal format is configurable in ClockBuilder Pro. Termination recommendations are provided in the Si540x NetSync™ Reference Manual and AN1347: Si540x Schematic Design and Board Layout Guidelines. Unused outputs should be left unconnected.
OUT0	3		
OUT1b	7		
OUT1	8		
OUT2b	9		
OUT2	10		
OUT3b	11		
OUT3	12		
OUT4b	14		
OUT4	15		
OUT5b	24		
OUT5	25		
OUT6b	27		
OUT6	28		
OUT7b	30		
OUT7	31		
OUT8b	32		
OUT8	33		
OUT9b	37		
OUT9	38		
OUT10b	39		
OUT10	40		

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Table 20. Si5402 Pin Descriptions (Continued)

Pin Name	Pin Number	Pin Type[1]	Description
OUT11b	42	O	**Output clocks:** The output clocks can be programmed as single-ended CMOS or differential LVDS, S-LVDS, CML, HCSL or ac-coupled LVPECL and support a programmable signal amplitude and common-mode voltage. Desired output signal format is configurable in ClockBuilder Pro. Termination recommendations are provided in the Si540x NetSync™ Reference Manual and AN1347: Si540x Schematic Design and Board Layout Guidelines. Unused outputs should be left unconnected.
OUT11	43		
OUT12b	46	O	**Output clocks with programmable slew rate limiting (SRL):** When outputs 12 and 13 are configured as CMOS outputs, they can also have the slew rate adjusted.
OUT12	47		
OUT13b	49		
OUT13	50		
Serial Interface			
SDA/SDIO	52	I/O	**Serial data interface:** This is the bidirectional data pin (SDA) for the I^{2}C mode, or the bidirectional data pin (SDIO) in the 3-wire SPI mode, or the input data pin (SDI) in the 4-wire SPI mode. When in I2C mode, this pin must be pulled-up using an external resistor of at least 1 kΩ. No pull-up resistor is needed when in SPI mode.
SCLK	53	I	**Serial clock input:** This pin functions as the serial clock input for both I^{2}C and SPI modes. When in I^{2}C mode, this pin must be pulled-up using an external resistor of at least 1 kΩ. No pull-up resistor is needed when in SPI mode.
A0/CSb	55	I	**Address select 0/chip select:** This pin functions as the hardware controlled lsb of the device address (A0) in I^{2}C mode. In SPI mode, this pin functions as the chip select input (active low). This pin is internally pulled-up and can be left floating if unused.
GPIO3 (A1/SDO)	56	O	**Address select 1/ serial data output/GPIO3:** This input pin operates as the hardware controlled next to lsb portion of the device address (A1) in I^{2}C mode. In 4-wire SPI mode this pin operates as the serial data output (SDO). In 3-wire SPI mode this pin can function as an additional GPIO pin (GPIO3).
Control/Status			
GPIO0	16	I or O	**Programmable general purpose input or outputs:** These pins can be programmed to the functions defined in Table 2, GPIO Pin Descriptions.
GPIO1	18		
GPIO2	19		
RSTb	20	I	**Reset pin:** This pin functions as an active-low reset input and is used to generate a device reset when held low for at least the specified Minimum Pulse Width. This resets the device back to a known state and reloads the NVM frequency plan and application. All clocks will stop while the RSTb pin is asserted. If there is no frequency plan in NVM, the reset pin will return the device to the bootloader state in which it is waiting for the frequency plan and application to be downloaded by the host controller. This pin accepts a CMOS input and is internally pulled up with a ~20 kΩ resistor to VDDIO. VDDA and VDD18 must be powered up and stable before releasing RSTb. RSTb must not be toggled faster than the maximum update rate (fUR) specification. Please refer to AN1347: Si540x Schematic Design and Board Layout Guidelines for more details on RSTb pin circuitry.
Power			
VDDIN	1	P	**Input clock supply voltage:** Supply voltage 3.3 V, 2.5 V or 1.8 V for the input clock buffers
VDDO1	6	P	**Output clock supply voltage 1 to 7:** Supply voltage 3.3 V, 2.5 V, or 1.8 V for outputs. Leave VDDO pins of unused output drivers unconnected. An alternate option is to connect the VDDO pin to a power supply and disable the output driver to minimize current consumption. An, 0402 1 µF "decoupling" capacitor, should be placed very close to each of these pins. VDDO may not exceed VDDA. The banks of outputs are powered as follows: VDDO1 – OUT[0:2] VDDO2 – OUT[3:4] VDDO3 – OUT[5] VDDO4 – OUT[6:7] VDDO5 – OUT[8] VDDO6 – OUT[9:11] VDDO7 – OUT[12:13] Data sheet jitter performance requires all outputs in a given bank to operate at a single frequency.
VDDO2	13		
VDDO3	23		
VDDO4	29		
VDDO5	34		
VDDO6	41		
VDDO7	48		
VDDA	17	P	**Core analog supply voltage:** This core supply can operate from a 3.3 V or 1.8 V power supply for low power mode. Note that all other supply voltages must be equal or lower voltage than the VDDA pin; so, in low power mode, no other supply can exceed 1.8 V. A 0402 1 µF capacitor should be placed very close to each of these pins.

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Table 20. Si5402 Pin Descriptions (Continued)

Pin Name	Pin Number	Pin Type[1]	Description
VDD18	26	P	**Core Supply Voltage 1.8 V:** The device core operates from a 1.8 V supply. A 0402 1 µF capacitor should be placed very close to each of these pins.
VDD18	51		
VDD18	54		
VDDIO	57	P	**Control, status IO clock supply voltage:** Supply voltage 3.3 V, 2.5 V, or 1.8 V for the serial interface, control, and status inputs and outputs.
VDDXO	58	P	**XTAL/external oscillator (XO) supply voltage:** Supply voltage of 3.3 V or 1.8 V supported for the reference. For best performance, VDDXO should be the same voltage and power source that is applied to the external oscillator (XO).
GND	Package Bottom	P	**Exposed die attach pad:** The exposed die attach pad (ePAD) on the bottom of the package should be connected to electrical ground.
No Connect			
NC	4	NC	No connection
NC	5	NC	
NC	44	NC	
NC	45	NC	
NC	61	NC	

1. I = Input; O = Output; P = Power; NC = No Connection; GND = Ground.

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7.3. Si5401 Pin Descriptions

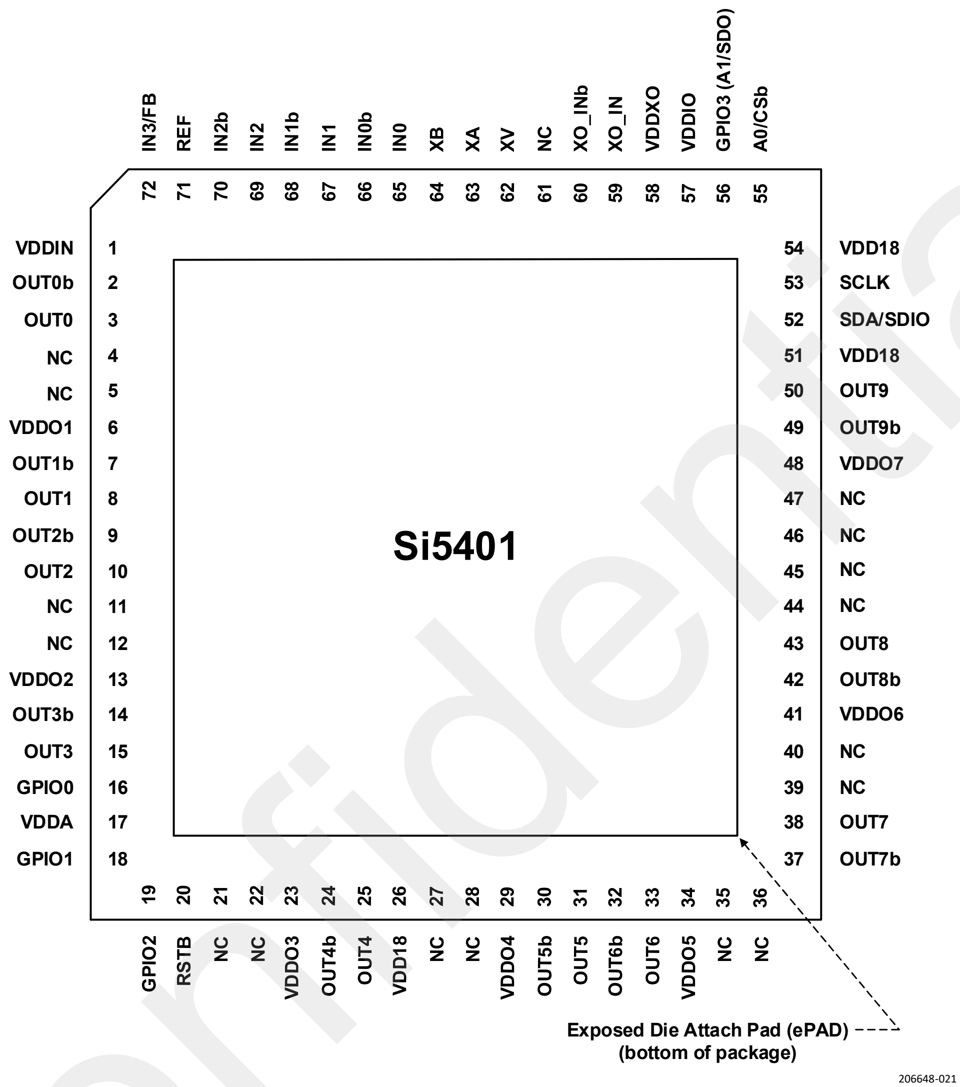

Figure 21. Si5401 Pinout

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Table 21. Si5401 Pin Descriptions

Pin Name	Pin Number	Pin Type[1]	Description
Inputs			
XO_IN	59	I	Input for inner loop crystal oscillator (XO) option.
XO_INb	60		
XV	62	I	**XTAL shield:** Connect this pin directly to the XTAL ground pins. Do not ground the XV pin. XV should be isolated from the PCB ground plane. See AN1347: Si540x Schematic Design and Board Layout Guidelines for layout guidelines.
XA	63	I	**Crystal input:** Input pins for external crystal (XTAL). XA and XB pins can be left unconnected when not in use.
XB	64		
REF	71	I	**Reference input:** Only used for TCXOs or OCXOs with single-ended outputs.
IN0	65	I	**Clock inputs:** IN0–IN3/FB accept an input clock for synchronizing the device. IN0–IN2 support both differential and single-ended clock signals. Input IN3/FB only supports a single-ended (SE) mode and can be used for Zero Delay Mode (ZBM) feedback (FB). When input IN2 is operating in single-ended mode it can provide two SE inputs each for a total of five customer-definable inputs. These pins are high-impedance and must be terminated externally. IN0–IN3/FB can be disabled in ClockBuilder Pro and the pins left unconnected if unused. Refer to the Si540x NetSync™ Reference Manual and AN1347: Si540x Schematic Design and Board Layout Guidelines for input termination options and more information on ZDM.
IN0b	66		
IN1	67		
IN1b	68		
IN2	69		
IN2b	70		
IN3/FB	72		
Outputs			
OUT0b	2	O	**Output clocks:** The output clocks can be programmed as single-ended CMOS or differential LVDS, S-LVDS, CML, HCSL or ac-coupled LVPECL and support a programmable signal amplitude and common-mode voltage. Desired output signal format is configurable in ClockBuilder Pro. Termination recommendations are provided in the Si540x NetSync™ Reference Manual and AN1347: Si540x Schematic Design and Board Layout Guidelines. Unused outputs should be left unconnected.
OUT0	3		
OUT1b	7		
OUT1	8		
OUT2b	9		
OUT2	10		
OUT3b	14		
OUT3	15		
OUT4b	24		
OUT4	25		
OUT5b	30		
OUT5	31		
OUT6b	32		
OUT6	33		
OUT7b	37		
OUT7	38		
OUT8b	42		
OUT8	43		
OUT9b	49	O	**Output clocks with programmable slew rate limiting (SRL):** When Output 9 is configured as CMOS outputs, it can also have the slew rate adjusted.
OUT9	50		

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Table 21. Si5401 Pin Descriptions (Continued)

Pin Name	Pin Number	Pin Type[1]	Description
Serial Interface			
SDA/SDIO	52	I/O	**Serial data interface:** This is the bidirectional data pin (SDA) for the I^{2}C mode, or the bidirectional data pin (SDIO) in the 3-wire SPI mode, or the input data pin (SDI) in the 4-wire SPI mode. When in I2C mode, this pin must be pulled-up using an external resistor of at least 1 kΩ. No pull-up resistor is needed when in SPI mode.
SCLK	53	I	**Serial clock input:** This pin functions as the serial clock input for both I^{2}C and SPI modes. When in I^{2}C mode, this pin must be pulled-up using an external resistor of at least 1 kΩ. No pull-up resistor is needed when in SPI mode.
A0/CSb	55	I	**Address select 0/chip select:** This pin functions as the hardware controlled lsb of the device address (A0) in I^{2}C mode. In SPI mode, this pin functions as the chip select input (active low). This pin is internally pulled-up and can be left floating if unused.
GPIO3 (A1/SDO)	56	O	**Address select 1/ serial data output/GPIO3:** This input pin operates as the hardware controlled next to lsb portion of the device address (A1) in I^{2}C mode. In 4-wire SPI mode this pin operates as the serial data output (SDO). In 3-wire SPI mode this pin can function as an additional GPIO pin (GPIO3).
Control/Status			
GPIO0	16	I or O	**Programmable general purpose input or outputs:** These pins can be programmed to the functions defined in Table 2, GPIO Pin Descriptions.
GPIO1	18		
GPIO2	19		
RSTb	20	I	**Reset pin:** This pin functions as an active-low reset input and is used to generate a device reset when held low for at least the specified Minimum Pulse Width. This resets the device back to a known state and reloads the NVM frequency plan and application. All clocks will stop while the RSTb pin is asserted. If there is no frequency plan in NVM, the reset pin will return the device to the bootloader state in which it is waiting for the frequency plan and application to be downloaded by the host controller. This pin accepts a CMOS input and is internally pulled up with a ~20 kΩ resistor to VDDIO. VDDA and VDD18 must be powered up and stable before releasing RSTb. RSTb must not be toggled faster than the maximum update rate (fUR) specification. Please refer to AN1347: Si540x Schematic Design and Board Layout Guidelines for more details on RSTb pin circuitry.
Power			
VDDIN	1	P	**Input clock supply voltage:** Supply voltage 3.3 V, 2.5 V or 1.8 V for the input clock buffers
VDDO1	6	P	**Output clock supply voltage 1 to 7:** Supply voltage 3.3 V, 2.5 V, or 1.8 V for outputs. Leave VDDO pins of unused output drivers unconnected. An alternate option is to connect the VDDO pin to a power supply and disable the output driver to minimize current consumption. An, 0402 1 µF "decoupling" capacitor, should be placed very close to each of these pins. VDDO may not exceed VDDA. The banks of outputs are powered as follows: VDDO1 – OUT[0:2] VDDO2 – OUT[3] VDDO3 – OUT[4] VDDO4 – OUT[5] VDDO5 – OUT[6] VDDO6 – OUT[7:8] VDDO7 – OUT[9] Data sheet jitter performance requires all outputs in a given bank to operate at a single frequency.
VDDO2	13		
VDDO3	23		
VDDO4	29		
VDDO5	34		
VDDO6	41		
VDDO7	48		
VDDA	17	P	**Core analog supply voltage:** This core supply can operate from a 3.3 V or 1.8 V power supply for low power mode. Note that all other supply voltages must be equal or lower voltage than the VDDA pin; so, in low power mode, no other supply can exceed 1.8 V. A 0402 1 µF capacitor should be placed very close to each of these pins.
VDD18	26	P	**Core Supply Voltage 1.8 V:** The device core operates from a 1.8 V supply. A 0402 1 µF capacitor should be placed very close to each of these pins.
VDD18	51		
VDD18	54		
VDDIO	57	P	**Control, status IO clock supply voltage:** Supply voltage 3.3 V, 2.5 V, or 1.8 V for the serial interface, control, and status inputs and outputs.
VDDXO	58	P	**XTAL/external oscillator (XO) supply voltage:** Supply voltage of 3.3 V or 1.8 V supported for the reference. For best performance, VDDXO should be the same voltage and power source that is applied to the external oscillator (XO).
GND	Package Bottom	P	**Exposed die attach pad:** The exposed die attach pad (ePAD) on the bottom of the package should be connected to electrical ground.
No Connect			

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Table 21. Si5401 Pin Descriptions (Continued)

Pin Name	Pin Number	Pin Type[1]	Description
NC	4	NC	No connection
NC	5	NC	
NC	11	NC	
NC	12	NC	
NC	21	NC	
NC	22	NC	
NC	27	NC	
NC	28	NC	
NC	35	NC	
NC	36	NC	
NC	39	NC	
NC	40	NC	
NC	44	NC	
NC	45	NC	
NC	46	NC	
NC	61	NC	

1. I = Input; O = Output; P = Power; NC = No Connect; GND = Ground.

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8. Packaging

8.1. Package Outline

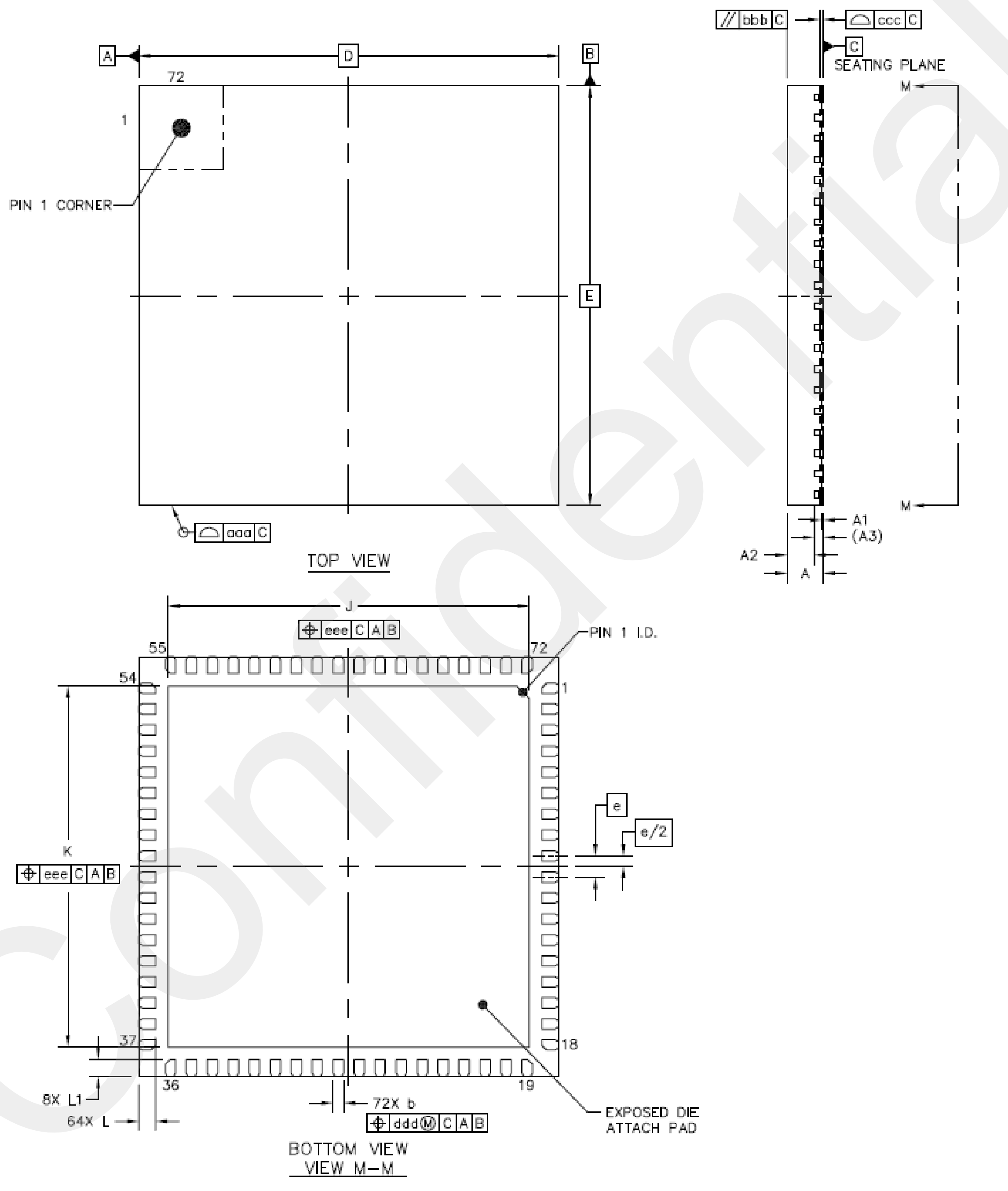

Figure 22. Si540x 72-QFN Package Diagram

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Table 22. Si540x Package Dimensions[1]

		Symbol	Min	Typ	Max
Total Thickness		A	0.8	0.85	0.9
Stand Off		A1	0	0.035	0.05
Mold Thickness		A2	–	0.65	–
L/F Thickness		A3	0.203 REF		
Lead Width		b	0.2	0.25	0.3
Body Size	X	D	10 BSC		
	Y	E	10 BSC		
Lead Pitch		e	0.5 BSC		
EP Size	X	J	8.5	8.6	8.7
	Y	K	8.5	8.6	8.7
Lead Length		L	0.35	0.4	0.45
		L1	0.3	0.4	0.45
Package Edge Tolerance		aaa	0.1		
Mold Flatness		bbb	0.1		
Coplanarity		ccc	0.08		
Lead Offset		ddd	0.1		
Exposed Pad Offset		eee	0.1		
Weight		N/A	—	0.35g	—

1. All dimensions shown are in millimeters (mm) unless otherwise noted. Dimensioning and tolerancing per ANSI Y14.5M-1994. This drawing conforms to JEDEC Solid State Outline MO-220.

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8.2. PCB Land Pattern

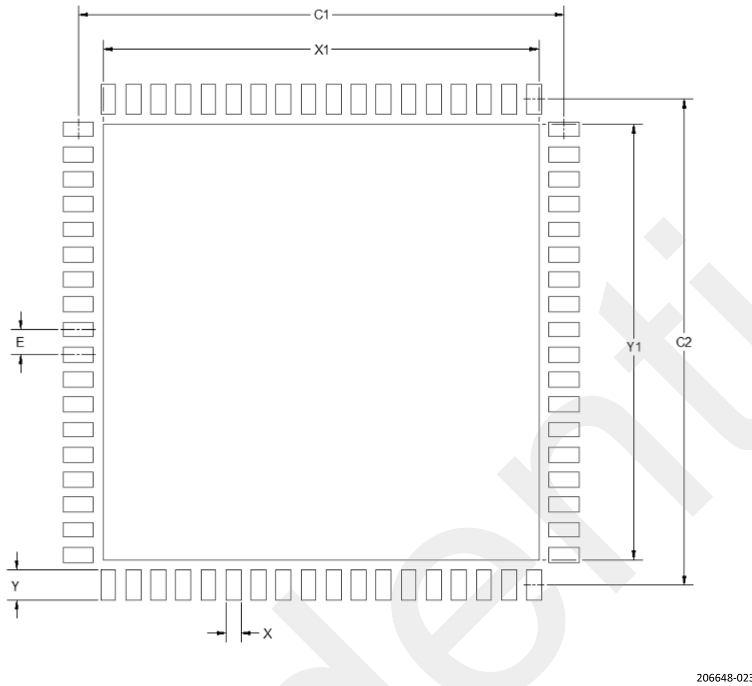

Figure 23. Si540x PCB Land Pattern

Table 23. Si540x PCB Land Pattern Dimensions[1]

Dimensions	mm	Notes
C1	9.70	**General** All dimensions shown are in millimeters (mm). This Land Pattern Design is based on the IPC-7351 guidelines. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a fabrication allowance of 0.05 mm. **Solder Mask Design** All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 mm minimum, all the way around the pad. **Stencil Design** A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release. The stencil thickness should be 0.125 mm (5 mils). The ratio of stencil aperture to land pad size should be 1:1 for all pads. A 4x4 array of 1.25 mm square openings on a 2.00 mm pitch should be used for the center ground pad. **Card Assembly** A No-Clean, Type-3 solder paste is recommended. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.
C2	9.70	
E	0.50	
X	0.30	
Y	0.60	
X1	8.70	
Y1	8.70	

1. The table notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine tune their SMT process as required for their application and tooling

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8.3. Top Marking

Figure 24. Si540x Top Marking

Table 24. Si540x Top Marking

Line	Characters	Description
1	Si540xg-	Base part number and device grade. **x** = Base Part number, 540**1**, 540**2**, 540**3**. g represents device grade. Refer to 2. Ordering Guide for latest device grade information.
2	Rxxxxx-GM	R = Product revision. (Refer to 2. Ordering Guide for latest revision). xxxxx = Customer specific NVM sequence number. Optional NVM code as- signed for custom, factory pre-programmed devices. Characters are not included for standard, factory default configured devices. -GM = Package (QFN) and temperature range.
3	YYWWTTTTTT	YYWW = Characters correspond to the year (YY) and work week (WW) of package assembly. TTTTTT = Manufacturing trace code.
4	Circle w/ 0.6 mm (72-QFN) diameter	Pin 1 indicator; left-justified.
	e3	Pb-free symbol; Center-Justified.
	TW	TW = Taiwan; Country of Origin (ISO Abbreviation).

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9. Revision History

Revision	Date	Description

A	October, 2023	Minor updates to datasheet template including figures and tables each being separately sequential numbering.
		
		Key Points
		• Replaced G.8273.1 (T-GM) with PRTC (T-GM) to more accurate reflect ITU standards.
		
		Block Diagrams
		• Updated Figure 1. Si5403 Block Diagram, Figure 2. Si5402 Block Diagram and Figure 3. Si5401 Block Diagram:
		- Changes have no impact to existing designs, changes add more flexibility in new designs. Configuration done in ClockBuilder Pro.
		- TCXO/OCXO REF input goes into input multiplexer, not directly into REFPLL.
		- REFPLL takes its input from input multiplexer.
		- Input to Input Phase Measurement includes TCXO/OCXO REF input.
		
		Section 1. Feature List
		• Changed last bullet of RFPLL (RF DSPLL) text to correct typos
		• Selectable jitter attenuation bandwidth: 10 Hz to 400Hz, 10 Hz to 400Hz Dual Reference JA.
		
		Section 2. Ordering Guide
		• Table 1. Ordering Guide, changed note 6 from Xilinx to AMD.
		
		Section 3. Functional Description
		• Figure 5. Si540x IEEE 1588 AMD Demo Platform Diagram, changed Xilinx to AMD.
		
		Section 3.3. Inputs
		• Figure 6. Input Structure
		- Changes have no impact to existing designs, changes add more flexibility in new designs.
		- TCXO/OCXO REF input goes into input multiplexer, not directly into REFPLL.
		- REFPLL takes its input from input multiplexer.
		- Added PHMON to Input Monitors
		
		Section 3.12 Device Initialization
		• Clarified the section by adding the new sentence "All clocks will stop during a hard reset" after sentence "A hard reset is initiated using RSTb pin or through the Device API RESTART command," and referenced "A hard reset is initiated using RSTb pin or through the Device API RESTART command." Referenced the Si540x Reference Manual as well as AN1360 for more information.
		
		Section 3.19. Application Programming Interface
		• Clarified that the secondary serial port only supports SPI 3-wire.
		
		Section 3.21 Power Supplies
		• Referenced AN1347 instead of Si540x Reference Manual.
		
		Section 3.21.2 Power Supply Ramp Rate
		• Referenced Table 8 for supply voltage ramp rate.
		
		Section 3.21.3 Low Power Mode
		• Added statement that NVM programming is not possible in low-power-mode, as VDDA must be at 3.3 V.
		
		Section 4. Electrical Specifications
		• Table 8. DC Characteristics
		- Core supply current (V_{DD18} + V_{DDA}) parameter:
		  - I_{DD18} symbol test condition, added footnote 2 to Si540x and deleted Si540x low power mode row.
		  - I_{DDA} symbol test condition, added footnote 2 to Si540x and deleted Si540x low power mode row.
		- Periphery supply current parameter:
		  - I_{DDIN} + I_{DDIO} symbol test condition, added footnote 2 to Si540x and deleted Si540x low power mode row
		  - I_{DDREF} symbol test condition, added footnote 2 to Si540x and deleted Si540x Low Power Mode row.

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Revision	Date	Description

A	October, 2023	• Table 13. Differential Clock Output Specifications
		- Parameter OUT-OUTb Skew, Symbol TSK_OUT
		  - Clarified this parameter is skew between positive and negative output pins.
		  - Expanded test conditions, which allowed some specs to be tightened without changing the overall spec min/max.
		- Removed HCSL line items from the following Table 13 parameter sections and added new HCSL output table (Table 14).
		  - Parameter output voltage swing, symbol V_{OUT}
		  - Parameter common mode voltage, symbol V_{CM}
		  - Parameter differential output impedance, symbol Z_0
		- Expanded table for parameter rise and fall times (20% to 80%)
		  - Added parameter rise and fall times (20% to 80%) OUT0 - 15, symbol t_r/t_f
		  - Removed HCSL line items from Table 13 parameter sections and added new Table 14 HCSL Output.
		  - Added Parameter Rise and Fall Times (20% to 80%) OUT16 - 17, Symbol tr/tf
		  - Outputs 16 and 17 have programmable CMOS slew rate, accordingly specification tables reflect the typical and maximum for those output types.
		- Removed previous footnote 6
		- Power supply noise rejection, footnote changed from note 8 to 7.
		- Output-to-output crosstalk, footnote changed from note 9 to 8.
		- Input-to-output crosstalk, footnote changed note from note 10 to 9.
		
		• Table 14. HCSL Clock Output Specifications
		- Added new Table 14 for HCSL clock output specifications and removed HCSL line items from Table 13.
		  - Separating HCSL outputs into its own table allows the output specifications to be more accurately defined.
		  - Output voltage swing maximum specification changed to 960*SF for HCSL standard, 800mVpp_se for both internal termination and external termination; HCSL fast, 800mVpp_se external termination.
		
		• Table 15. LVCMOS Clock Output Specifications
		- Added new footnote 6 to address SRL outputs.
		- Added footnote 6 to parameter rise and fall time (20% to 80%).
		
		• Table 17. Performance Characteristics
		- Clarified footnote 5 with the following additional statement: “after the output phase has achieved a steady state value.”
		- Updated footnote 9 to clarify based on new ClockBuilder Pro spur analysis tool, which helps customers analyze added jitter and spurs due to cross talk.
		
		• Tables 19, 20, and 21. Si5403, Si5402, and Si5401 Pin Descriptions
		- Updated RSTb pin name to: RSTb, Pin: 20, Pin Type: I.
		  - Added addition text on RSTb operation incorporating information found in other application notes, reference manuals, and Si550x supporting documents.
		- Updated XV pin 62 and input clock pins 65 through 72.
		  - Added reference to AN1347 instead of Si540x Reference Manual.

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