PCN No.: 2082	**Date:** May 17th, 2022

Title: **epc635 design improvements** (Elimination of asymmetrical DCSs, improve PLL speed performance)

Classification: ☐ Major ☒ Minor

Item: ☒ Design ☐ Assembly Process ☐ Testing ☐ Data Sheet ☐ Package/Logistic
☐ Others:

Affected Product(s)
epc635 (P100 181)

Description of Change(s)

a) PLL stability improvement

- Change(s):
  - Power supply rejection (PSR) improved
- Achievement(s):
  - PLL frequency stability over specified temperature range and PLL frequency range guaranteed with improved margin

b) DCS asymmetry elimination

- Change(s):
  - Pixel wiring optimization to reduce parasitic coupling
- Achievement(s):
  - DCS asymmetries reduced as expected
  - Design changes and improvements verified and compared with implementation with epc660-011

Reason of Change(s)
Improve performance of epc635

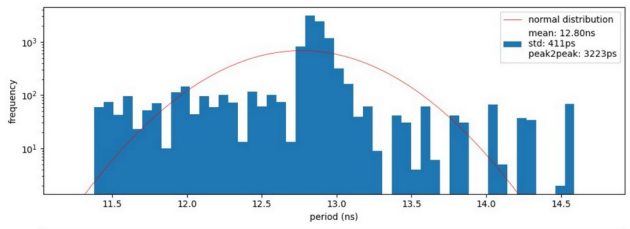
Verification Summary

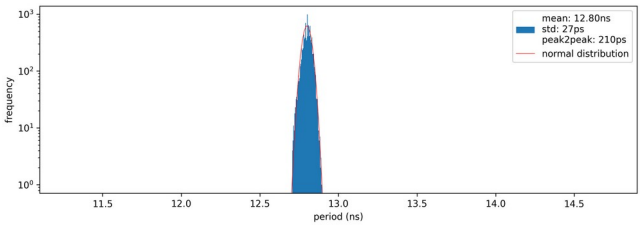
a) PLL stability improvement

Verified on epc635-003. PLL frequency stability at wafer level proven at -40°C with a frequency of 80 MHz. Jitter in video mode is a factor of 2 to 5 better in v003 than in v002 and 10 to 20 times better in idle mode. The following graph shows the jitter measurement in idle mode.

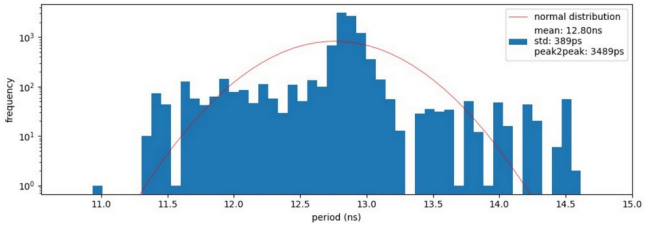
epc635-002 epc635-003

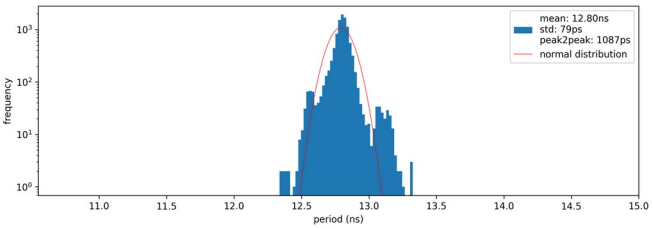
Idle





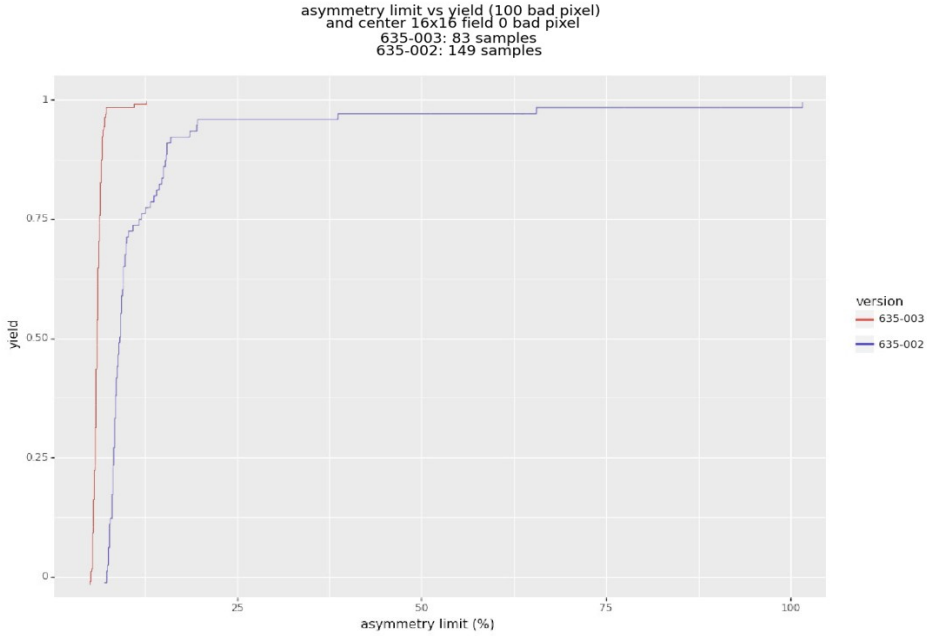
video mode





b) DCS asymmetry elimination

Verified on epc635-003. The DCS asymmetry of epc635-003 improved significantly compared to epc635-002, as shown in the graph below. The blue curve (line) shows the distribution of the asymmetry index of the epc635-002, whereas the red line shows the new epc635-003.



Reliability / Qualification Summary No impact on reliability nor on physical quality expected → no reliability or qualification tests will be performed.		
Implementation Plan • Phase-out epc635-002 from stock by end Q2´2022 adopting ´low temperature operation" (see "epc635_Low-temp_operation-V1.4" and datasheet V2.19) • Phase-in epc635-003 starting May´2022		
Originator: FMO	***Date:***17.03.22	
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