

## Product / Process Change Notice

PCN No.: Q000-PCN-PA202205-01A

Date: 2023-09-21.

<b>Change Title:</b> <u>Add DB HiTek as new fabrication FAB site.</u>			
Change Classification: <input checked="" type="checkbox"/> Major <input type="checkbox"/> Minor Change item: <input type="checkbox"/> Design <input type="checkbox"/> Raw Material <input checked="" type="checkbox"/> Wafer FAB <input type="checkbox"/> Package Assembly <input type="checkbox"/> Testing <input type="checkbox"/> Others: _____.			
<b>Affected Product(s) :</b> The affected part is NPCP215FA0YX.			
<b>Description of Change(s) :</b> Add new fabrication FAB site for affected part at DB HiTek(DB HiTek Co., Ltd., Korea) as the new source as the 2nd source. <b><u>New Supplier</u></b> DB HiTek Co., Ltd., Korea (hereinafter “DB HiTek”), (73, Sanguan-gil, Gangok-myeon, Eumseong-gun, Chungcheongbuk-do, 27605, Rep. of KOREA).			
<b>Reason for Change(s) :</b> Enabling alternate foundry capability for the affected part to secure manufacturing capacity, extend manufacturing flexibility and enhance preparedness for disaster recovery.			
<b>Impact of Change(s) : ( positive &amp; negative )</b> Form: No change. Fit: No change. Function: No change. Reliability: No change. (passed the qualification.) HSF (Hazardous Substances Free): No change			
<b>Qualification Plan/ Results :</b> Passed the reliability qualification includes Pre-Condition, TCT, uHAST and HTSL, please refer to appendix A for details.			
<b>Implementation Plan :</b> 1. Samples for customer evaluation are available, should customer decide such evaluation is needed. 2. Depending on inventory availability, Nuvoton may execute this PCN immediately after customer approval. Therefore, if customer approval is obtained prior to the implementation date, Nuvoton may make this PCN effective right after customer approved. <input checked="" type="checkbox"/> Date Code: _____ onward <input type="checkbox"/> Lot No.: _____ onward <input type="checkbox"/> Implemented date: <u>Dec. 19, 2023</u>			
<b>Originator:</b>	<b>H.Y. Lai / Q100</b>	<b>Approval:(QRA Director )</b>	<b>C.H. Shen/ Q000</b>
<b>Contact for Questions &amp; Concerns</b> Name: <u>HYLai</u> TEL: <u>886-3-5770066 (ext. 31226)</u> FAX: <u>886-3-5792673.</u> Address: <u>No.4, Creation Rd. III Science-Based Industrial Park Hsinchu, Taiwan, R.O.C..</u> E-mail: <u>hylai0@nuvoton.com.</u>			

## Customer Comments:

Note: Please sign this notice, and return to **Nuvoton** contact within **30** days. If no response is received within **30** days, this Change Request will be assumed to meet your approval.

<input type="checkbox"/> Approval	<input type="checkbox"/> Disapproval	<input type="checkbox"/> Conditional Approval: _____
Date: _____	Dept. name: _____	Person in charge: _____

## Follow-up and Tracing:

### A. copies to

**Test / Product:** ☐ UL40 Long Chieu ☐ UL40 Simon Wilson ☐ AS60 CHTsai ☐ AS70 JWCheng.

**Design/ Marketing:** ☐ UL00 Mark Hemming ☐ AM00 CPLin ☐ AM20 YHYu.

**Production control/ Others:** ☐ P100 YLHsu ☐ P100 CHHsu.

### B. Changes:

#### 1. Document / Test program:

Document No/ test program	Document name/ test program name	Version		Responsible	Completed date	Remark
		before	after			
NA	NA	NA	NA	NA	NA	NA

Verifed by: \_\_\_\_\_.

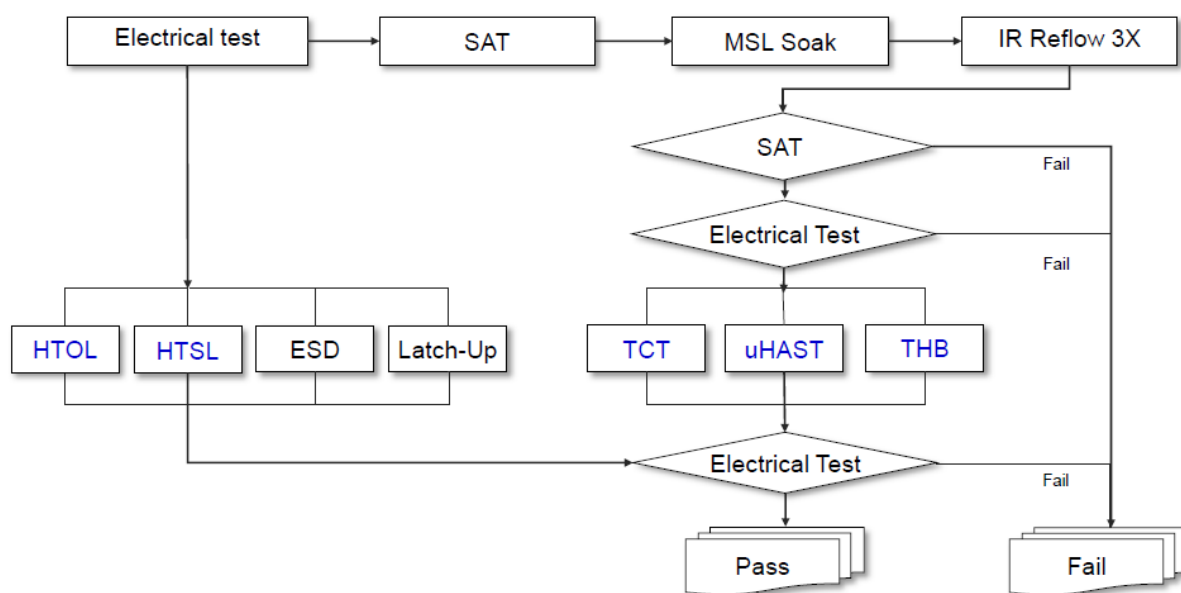
## Appendix A: Qualification report

### Data Summary



TEST MODE	TEST CONDITION	DURATION	LOT #	S/S	FAIL	MEASUREMENT
Precondition	Bake : 125℃	24Hr	3	600	0	Electrical test SAT
	Soak : 30℃ / 60%	192Hr				
	Reflow : 260℃	3cycle				
High Temperature Operating Life (HTOL)	T <sub>a</sub> ≥ 125℃ ± 5℃ VDDIO : 3.6V, PVDD : 28V	1008Hr	3	231	0	Electrical test
High Temperature Storage Life (HTSL)	150℃	1008Hr	3	150	0	Electrical test
Temperature Humidity Bias Test (THB) *	85℃ / 85% RH VDD1 : 3.47V, VDD2 : 26.4V	1008Hr	3	45	0	Electrical test
Temperature Cycling (TCT) *	-65℃ ~ 150℃	500cycle	3	150	0	Electrical test
Highly Accelerated Stress Test with unbiased (uHAST) *	130℃/85%RH/33.3psia No bias	96Hr	3	150	0	Electrical test

## Test Procedure



## Test Description \_ Life Test

### HTOL ( High Temperature Operating Life test)

This test is used to determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way, and is primarily for device qualification and reliability monitoring.



→ A total of 231 devices are completed 1008 hours with no failure.

Test Condition	Reference Document	Duration	SS	Results
125℃ VDDIO 3.6V, PVDD 28V	JESD22-A108	1008 Hrs	231 EA	PASS

## Test Description \_ Life Test

### FIT and MTTF Calculation based on HTOL

Temperature acceleration for semiconductor failure mechanism is usually described by the Arrhenius equation:

$$AFT = \exp \left[ \frac{E_a}{k} \cdot \left( \frac{1}{T_1} - \frac{1}{T_2} \right) \right] = 77.94$$

Where :

AFT = Temperature acceleration factor

exp = Exponential function of the natural logarithm

Ea = Activation energy in electron volts (Model acceleration factor : 0.7 eV for Gate oxide defect)

k = Boltzmann's constant ( $8.617 \times 10^{-5}$  electron volts/Kelvin)

T1 = Temperature at normal use conditions (55 °C) in kelvins (328 K)

T2 = Temperature at accelerated condition (125 °C) in kelvins (398 K)

The Failure rate is described by the following equation:

$$\lambda = \left[ \chi^2 (\alpha, d.f.) \cdot 10^9 / 2 \text{ EDH} \right] \text{ FITs} = 50.4 \text{ FITs}$$

Where :

$\lambda$  = Failure rate in FITs  $\chi^2$  = Chi-square distribution value

$\alpha$  = confidence level 60 % (0.4) d.f = Degree of freedom = 2 (n + 1)

n = Number of observed failure during test

EDH = Equivalent Device Hour (AF \* Sample size \* Stress time t)

Based on HTOL (High Temperature Operating Life) & ELFR (Early Life Failure Rate)

a. FIT (Failures-In-Time) =  $\chi^2 (\alpha, d.f.) \cdot 10^9 / 2 \text{ EDH}$  ] FITs = 50.4 FITs

b. MTTF (Mean Time To Failure) =  $1 / \lambda$  = 756 Year

## Test Description \_ Life Test

### HTSL ( High Temperature Storage Life test )

High Temperature storage test is typically used to determine the effect of time and temperature, under storage conditions, for thermally activated failure mechanisms of solid state electronic devices, including nonvolatile memory devices (data retention failure mechanisms).



→ A total of 150 devices are completed 1008 hours with no failure.

Test Condition	Reference Document	Duration	SS	Results
150℃	JESD22-A103	1008 Hrs	150 EA	PASS

## Test Description \_ Environmental Test

### THB ( Temperature Humidity Bias test )

This test is performed for the purpose of evaluating the reliability of non-hermetic packaged solid-state devices in humid environments. It employs conditions of temperature, humidity, and bias which accelerate the penetration of moisture through the external protective material or along the interface between the external protective material and the metallic conductors which pass through it.

→ A total of 45 devices are completed 1008 hours with no failure.

Test Condition	Reference Document	Duration	SS	Results
85°C / 85% RH VDD1 3.47V, VDD2 26.4V	JESD22-A101	1008 Hrs	45 EA	PASS

### TCT ( Temperature Cycle test )

This test is conducted to determine the ability of components and solder interconnects to withstand mechanical stresses induced by alternating high and low temperature extremes. Permanent changes in electrical and/or physical characteristics can result from these mechanical stresses.



→ A total of 150 devices are completed 500 cycles with no failure.

Test Condition	Reference Document	Duration	SS	Results
-65°C / 150°C	JESD22-A104	500 cycles	150 EA	PASS



## Test Description \_ Environmental Test



### uHAST ( Unbiased Highly Accelerated Temperature and Humidity Stress test)

This test is performed to evaluate the moisture resistance integrity of non-hermetic packaged solid state devices using moisture condensing or moisture saturated steam environments. It is a highly accelerated test which employs conditions of pressure, humidity and temperature under condensing conditions to accelerate moisture penetration through the external protective material or along the interface between the external protective material and the metallic conductors passing through it.



→ A total of 150 devices are completed 96 hours with no failure.

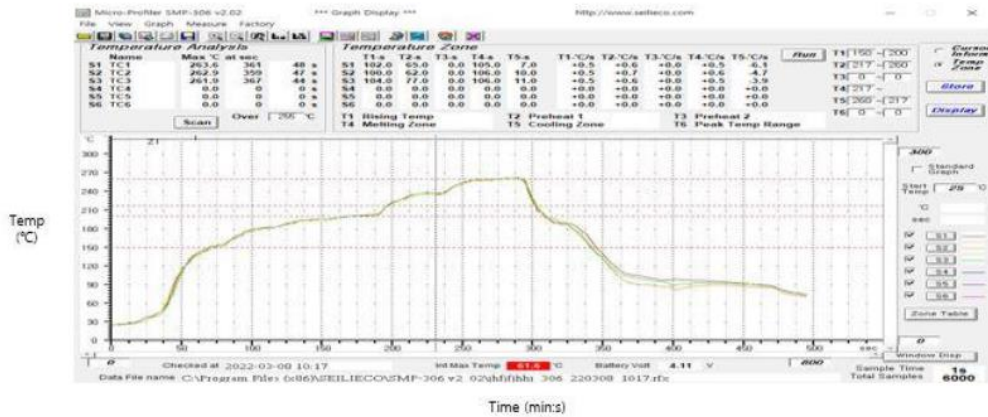
Test Condition	Reference Document	Duration	SS	Results
130 °C / 85% / 33.3psia	JESD22-A102	96 Hr	150 EA	PASS

# Reflow Profile



Reflow Profile was set using 3 representative components. All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow.

고객번호	2203-03399-01	의뢰번호	2203-03399-01	고객사	웰랑	제품명	DNW116F
PKG TYPE	-	사용장비	Reflow	Peak	≥ 260 °C	조건	JEDEC
PGM명	2203-03399-01_DNW116F.rdf						

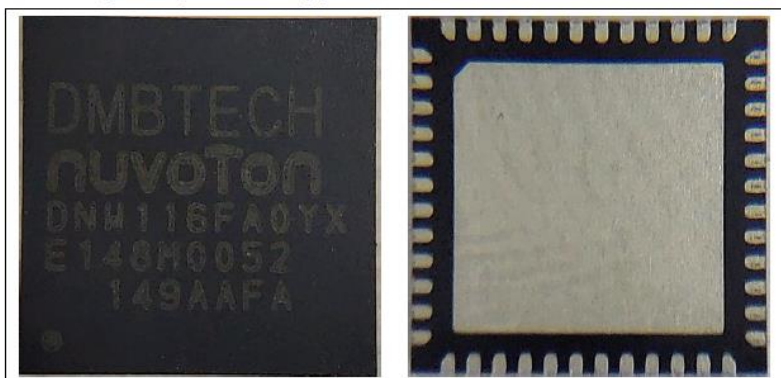


## Pb-Free Assembly

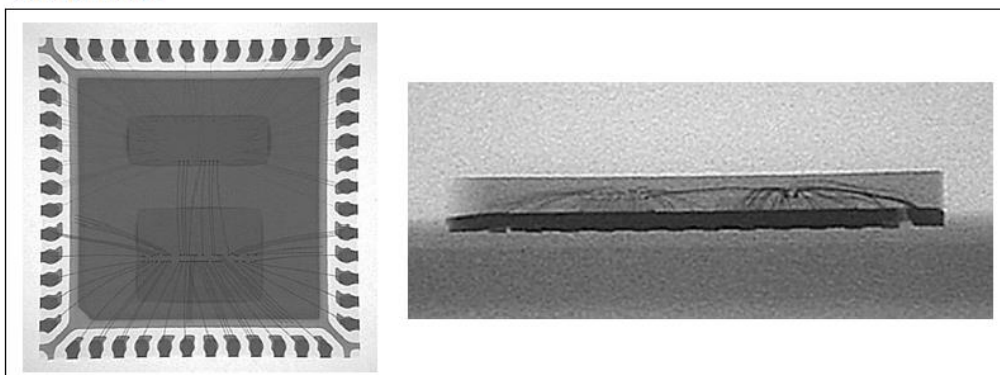
Item	Preheat/Soak	Ramp-up rate	217°C Maintained above	Peak package body temperature	Retention time of 255°C	Ramp-down rate
Scope	150°C~200°C 60-120 s	3 °C/s max.	217°C 60-150 s	260°C or more	30 s more	6 °C/s max.
Channel #1	102.00	0.50	105.00	263.60	48.00	+6.10
Channel #2	100.00	0.50	106.00	262.90	47.00	+4.70
Channel #3	104.00	0.50	106.00	261.90	44.00	-3.90

## Package Analysis

Marking & Top/Bottom appearance



X-ray image

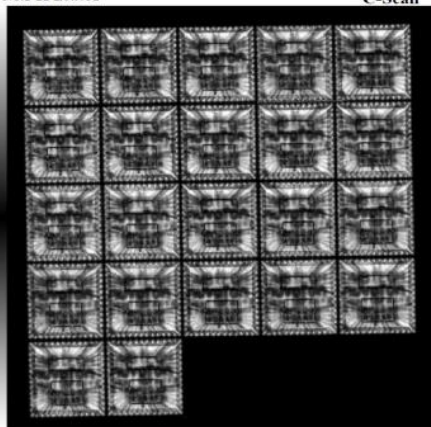


## Package Analysis

### Initial SAT images

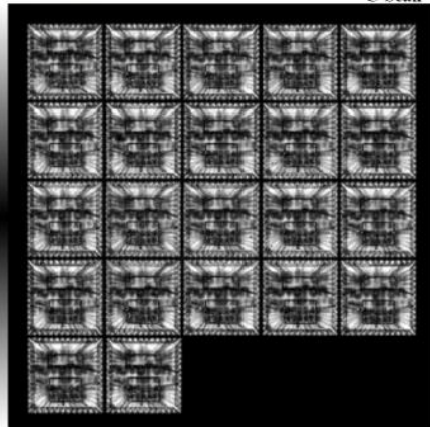
No.1-22 Lot.032

C-Scan



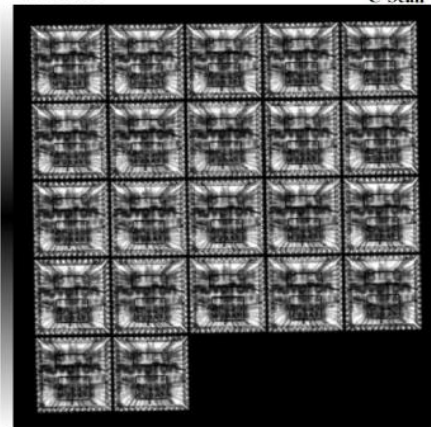
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C-Scan



No.1-22 Lot.052

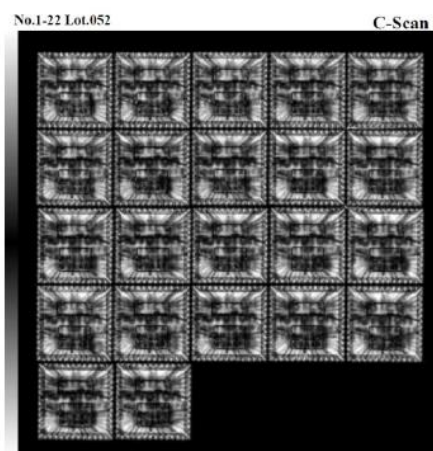
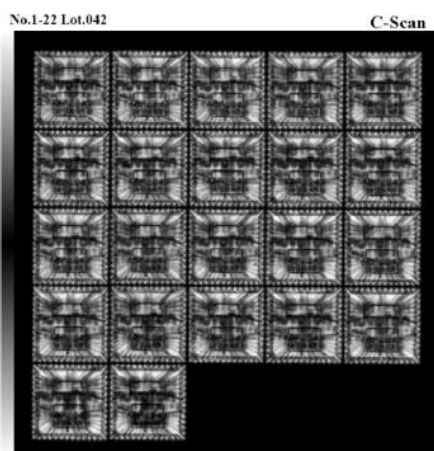
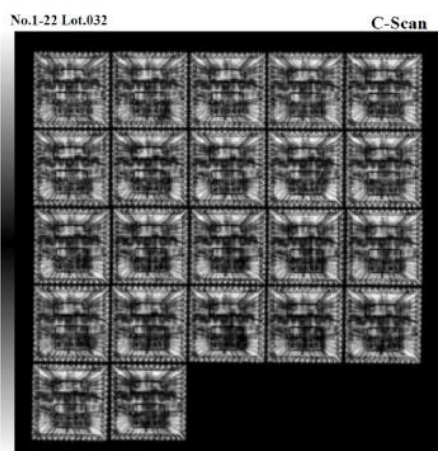
C-Scan



- No Package Crack & Delamination were found.

## Package Analysis

### SAT images after Preconditioning



- After MSL3 @260 °C test, no Package Crack & Delamination were found.