# 650V-45mΩ SiC FET

Rev. OBS, September 2021

DATASHEET

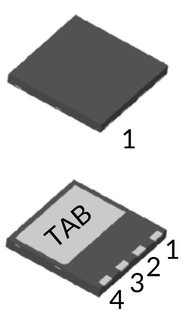
# UF3SC065040D8S

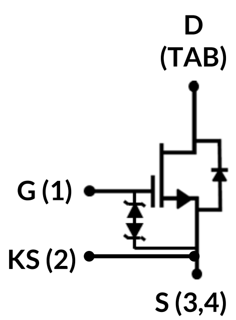
**Obsolete**

## Description

**The UF3SC065040D8S is now end-of-life and not recommended for new designs. The UF3SC065040B7S is recommended as a replacement.**

This SiC FET device is based on a unique 'cascode' circuit configuration, in which a normally-on SiC JFET is co-packaged with a Si MOSFET to produce a normally-off SiC FET device. The device's standard gate-drive characteristics allows for a true "drop-in replacement" to Si IGBTs, Si FETs, SiC MOSFETs or Si superjunction devices. Available in the DFN8X8-4L package, this device exhibits ultra-low gate charge and exceptional reverse recovery characteristics, making it ideal for switching inductive loads , and any application requiring standard gate drive.




## Features

- Typical on-resistance $R_{DS(on),typ}$ of 45mΩ
- Maximum operating temperature of 150°C
- Excellent reverse recovery
- Low gate charge
- Low intrinsic capacitance
- ESD protected, HBM class H2 (2000V to 4000V), CDM class C3 (>1000V)
- DFN8X8-4L package for faster switching, clean gate waveforms

## Typical applications

- EV charging
- PV inverters
- Switch mode power supplies
- Power factor correction modules
- Motor drives
- Induction heating

| Part Number | Package | Marking |
|---|---|---|
| UF3SC065040D8S | DFN8X8-4L | UF3SC065040D8S |

RoHS COMPLIANT Pb LEAD FREE HF HALOGEN FREE Green

## Maximum Ratings

| Parameter | Symbol | Test Conditions | Value | Units |
|---|---|---|---|---|
| Drain-source voltage | $V_{DS}$ | | 650 | V |
| Gate-source voltage | $V_{GS}$ | DC | -25 to +25 | V |
| Continuous drain current [1] | $I_D$ | $T_C$ < 120°C | 18 | A |
| Pulsed drain current [2] | $I_{DM}$ | $T_C$ = 25°C | 110 | A |
| Single pulsed avalanche energy [3] | $E_{AS}$ | L=15mH, $I_{AS}$ =3.19A | 76 | mJ |
| Power dissipation | $P_{tot}$ | $T_C$ = 25°C | 125 | W |
| Maximum junction temperature | $T_{J,max}$ | | 150 | °C |
| Operating and storage temperature | $T_J$, $T_{STG}$ | | -55 to 150 | °C |
| Reflow soldering temperature | $T_{solder}$ | reflow MSL 3 | 260 | °C |

1. Limited by bondwires
2. Pulse width $t_p$ limited by $T_{J,max}$
3. Starting $T_J$ = 25°C



## Thermal Characteristics

| Parameter | Symbol | Test Conditions | Value | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| Thermal resistance, junction-to-case | $R_{\theta JC}$ | | | 0.8 | 1 | °C/W |

## Electrical Characteristics ($T_J$ = +25°C unless otherwise specified)

### Typical Performance - Static

| Parameter | Symbol | Test Conditions | Value | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| Drain-source breakdown voltage | $BV_{DS}$ | $V_{GS}$=0V, $I_D$=1mA | 650 | | | V |
| Total drain leakage current | $I_{DSS}$ | $V_{DS}$=650V, $V_{GS}$=0V, $T_J$=25°C | | 0.7 | 150 | μA |
| | | $V_{DS}$=650V, $V_{GS}$=0V, $T_J$=150°C | | 5 | | |
| Total gate leakage current | $I_{GSS}$ | $V_{DS}$=0V, $T_J$=25°C, $V_{GS}$=-20V / +20V | | 6 | ± 20 | μA |
| Drain-source on-resistance | $R_{DS(on)}$ | $V_{GS}$=12V, $I_D$=20A, $T_J$=25°C | | 45 | 58 | mΩ |
| | | $V_{GS}$=12V, $I_D$=20A, $T_J$=125°C | | 67 | | |
| | | $V_{GS}$=12V, $I_D$=20A, $T_J$=150°C | | 70 | | |
| Gate threshold voltage | $V_{G(th)}$ | $V_{DS}$=5V, $I_D$=10mA | 4 | 5 | 6 | V |
| Gate resistance | $R_G$ | f=1MHz, open drain | | 4.5 | | Ω |



### Typical Performance - Reverse Diode

| Parameter | Symbol | Test Conditions | Value | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| Diode continuous forward current [1] | $I_S$ | $T_C$ < 120°C | | | 18 | A |
| Diode pulse current [2] | $I_{S,pulse}$ | $T_C$=25°C | | | 110 | A |
| Forward voltage | $V_{FSD}$ | $V_{GS}$=0V, $I_F$=10A, $T_J$=25°C | | 1.2 | 1.7 | V |
| | | $V_{GS}$=0V, $I_F$=10A, $T_J$=150°C | | 1.25 | | |
| Reverse recovery charge | $Q_{rr}$ | $V_R$=400V, $I_F$=20A, $V_{GS}$=-5V, $R_{G\_EXT}$=10Ω di/dt=1380A/μs, $T_J$=25°C | | 185 | | nC |
| Reverse recovery time | $t_{rr}$ | | | 29 | | ns |
| Reverse recovery charge | $Q_{rr}$ | $V_R$=400V, $I_F$=20A, $V_{GS}$=-5V, $R_{G\_EXT}$=10Ω di/dt=1380A/μs, $T_J$=150°C | | 169 | | nC |
| Reverse recovery time | $t_{rr}$ | | | 28 | | ns |

## Typical Performance - Dynamic

| Parameter | Symbol | Test Conditions | Value | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| Input capacitance | $C_{iss}$ | $V_{DS}$=100V, $V_{GS}$=0V f=100kHz | | 1500 | | pF |
| Output capacitance | $C_{oss}$ | | | 200 | | |
| Reverse transfer capacitance | $C_{rss}$ | | | 2.2 | | |
| Effective output capacitance, energy related | $C_{oss(er)}$ | $V_{DS}$=0V to 400V, $V_{GS}$=0V | | 146 | | pF |
| Effective output capacitance, time related | $C_{oss(tr)}$ | $V_{DS}$=0V to 400V, $V_{GS}$=0V | | 325 | | pF |
| $C_{OSS}$ stored energy | $E_{oss}$ | $V_{DS}$=400V, $V_{GS}$=0V | | 11.7 | | μJ |
| Total gate charge | $Q_G$ | $V_{DS}$=400V, $I_D$=20A, $V_{GS}$ = -5V to 12V | | 43 | | nC |
| Gate-drain charge | $Q_{GD}$ | | | 11 | | |
| Gate-source charge | $Q_{GS}$ | | | 19 | | |
| Turn-on delay time | $t_{d(on)}$ | $V_{DS}$=400V, $I_D$=20A, Gate Driver =-5V to +12V, Turn-on $R_{G,EXT}$=8.5Ω, Turn-off $R_{G,EXT}$=22Ω Inductive Load, FWD: same device with $V_{GS}$ = -5V, $R_G$ = 10Ω, $T_J$=25°C | | 24 | | ns |
| Rise time | $t_r$ | | | 18 | | |
| Turn-off delay time | $t_{d(off)}$ | | | 44 | | |
| Fall time | $t_f$ | | | 9 | | |
| Turn-on energy | $E_{ON}$ | | | 144 | | μJ |
| Turn-off energy | $E_{OFF}$ | | | 14 | | |
| Total switching energy | $E_{TOTAL}$ | | | 158 | | |
| Turn-on delay time | $t_{d(on)}$ | $V_{DS}$=400V, $I_D$=20A, Gate Driver =-5V to +12V, Turn-on $R_{G,EXT}$=8.5Ω, Turn-off $R_{G,EXT}$=22Ω Inductive Load, FWD: same device with $V_{GS}$ = -5V, $R_G$ = 10Ω, $T_J$=150°C | | 21 | | ns |
| Rise time | $t_r$ | | | 15 | | |
| Turn-off delay time | $t_{d(off)}$ | | | 47 | | |
| Fall time | $t_f$ | | | 8 | | |
| Turn-on energy | $E_{ON}$ | | | 118 | | μJ |
| Turn-off energy | $E_{OFF}$ | | | 6 | | |
| Total switching energy | $E_{TOTAL}$ | | | 124 | | |

## Typical Performance Diagrams

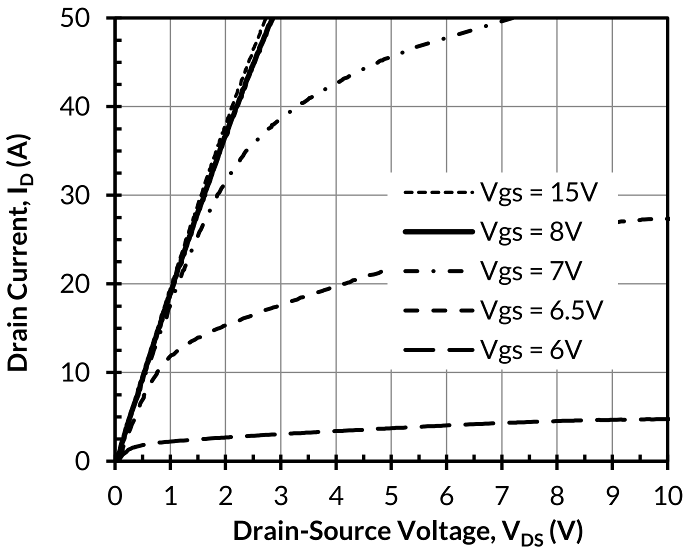



Figure 1. Typical output characteristics at $T_J$ = - 55°C, tp < 250μs

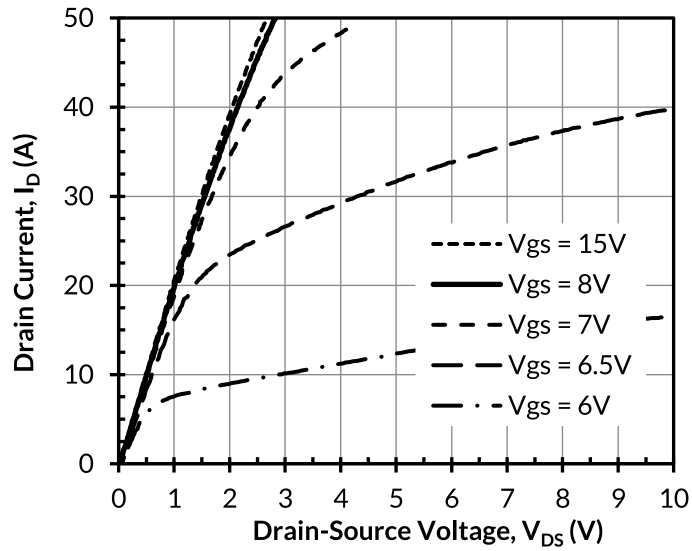



Figure 2. Typical output characteristics at $T_J$ = 25°C, tp < 250μs



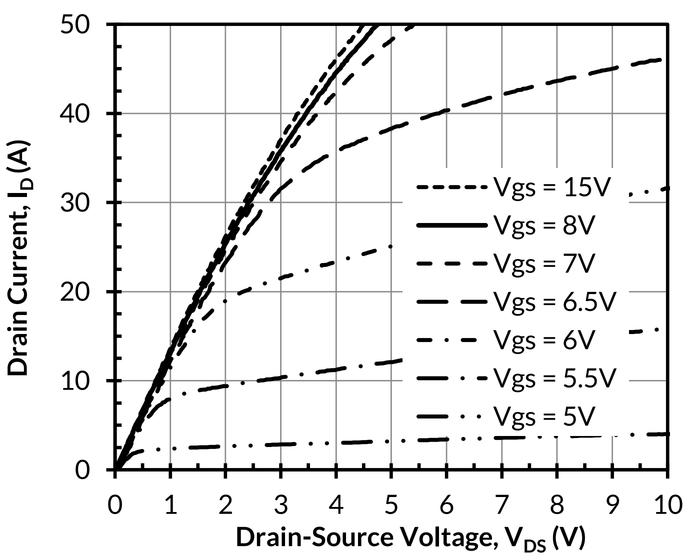



Figure 3. Typical output characteristics at $T_J$ = 150°C, tp < 250μs

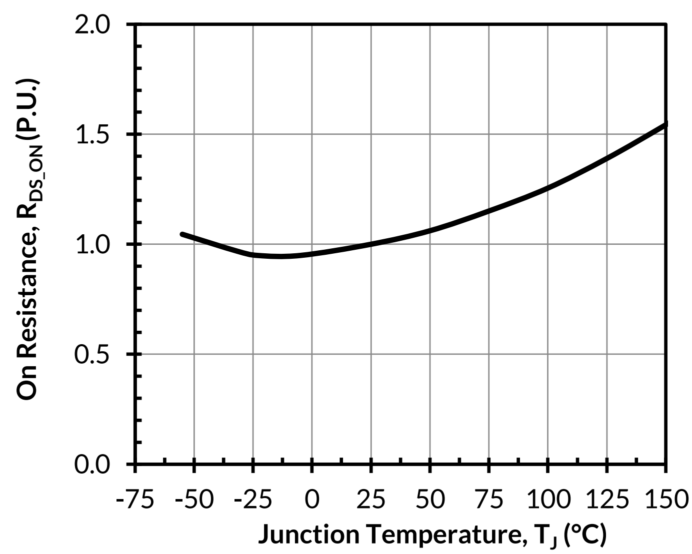



Figure 4. Normalized on-resistance vs. temperature at $V_{GS}$ = 12V and $I_D$ =20A

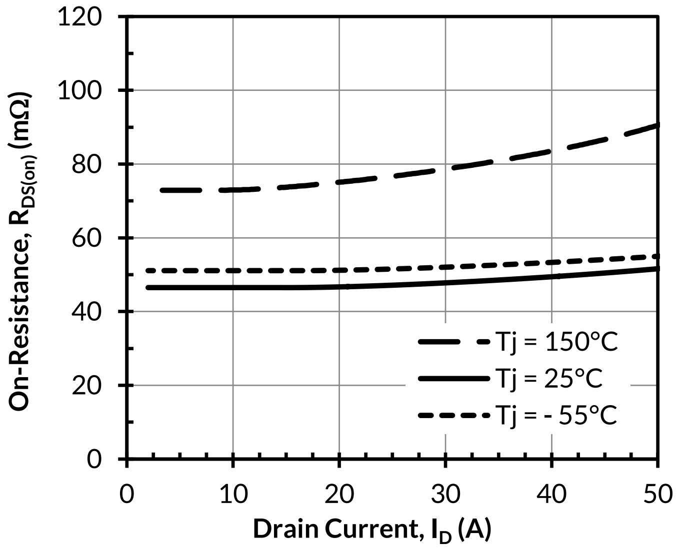



Figure 5. Typical drain-source on-resistances at $V_{GS}$ = 12V

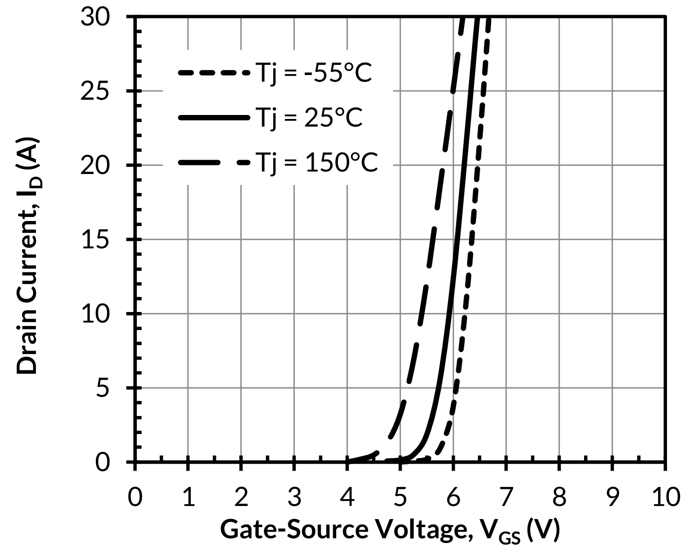



Figure 6. Typical transfer characteristics at $V_{DS}$ = 5V



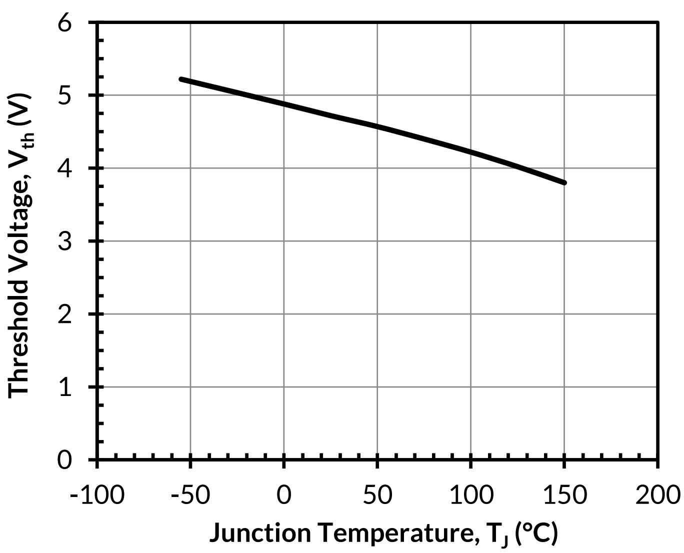



Figure 7. Threshold voltage vs. junction temperature at $V_{DS}$ = 5V and $I_D$ = 10mA

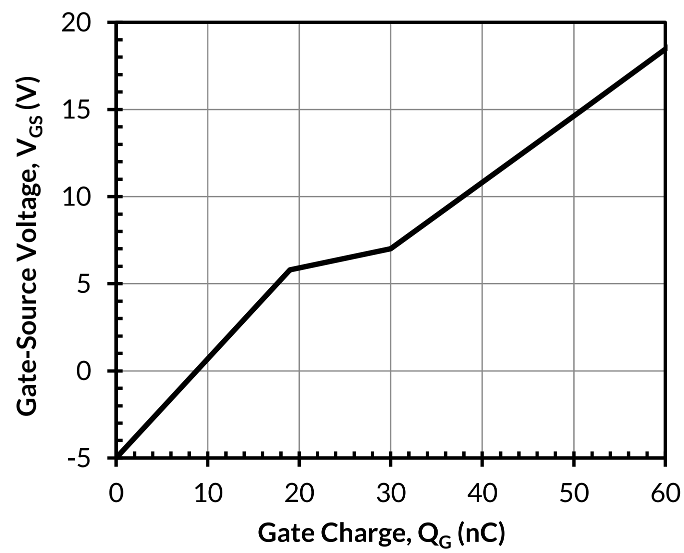



Figure 8. Typical gate charge at $V_{DS}$ = 400V and $I_D$ = 20A

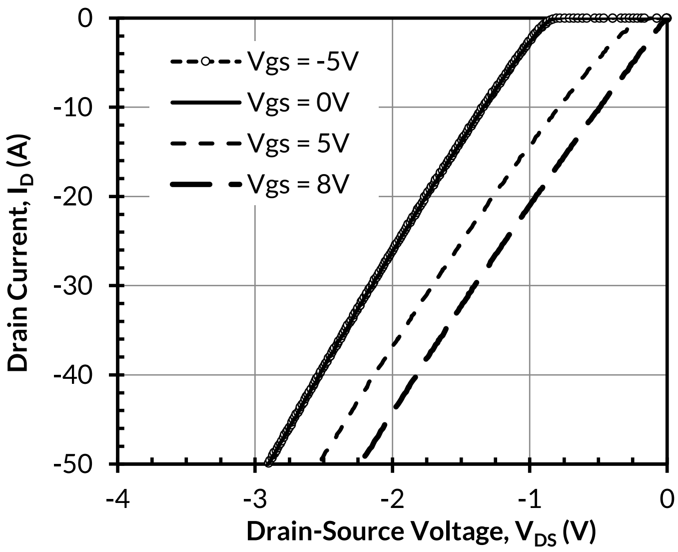



Figure 9. 3rd quadrant characteristics at $T_J$ = -55°C

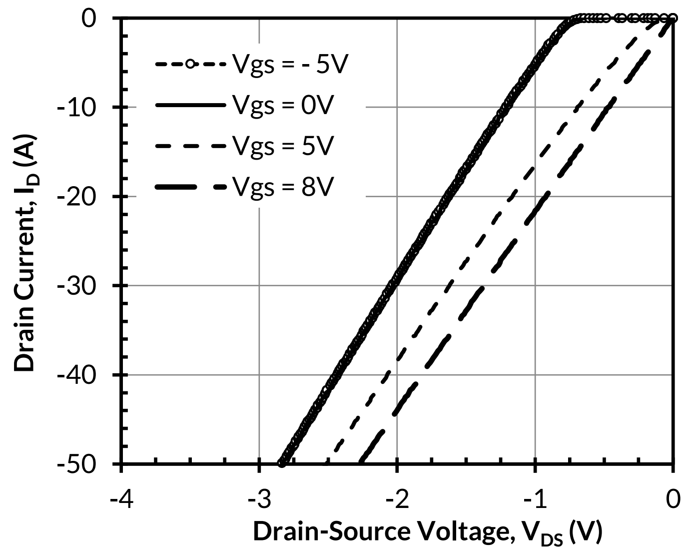



Figure 10. 3rd quadrant characteristics at $T_J$ = 25°C



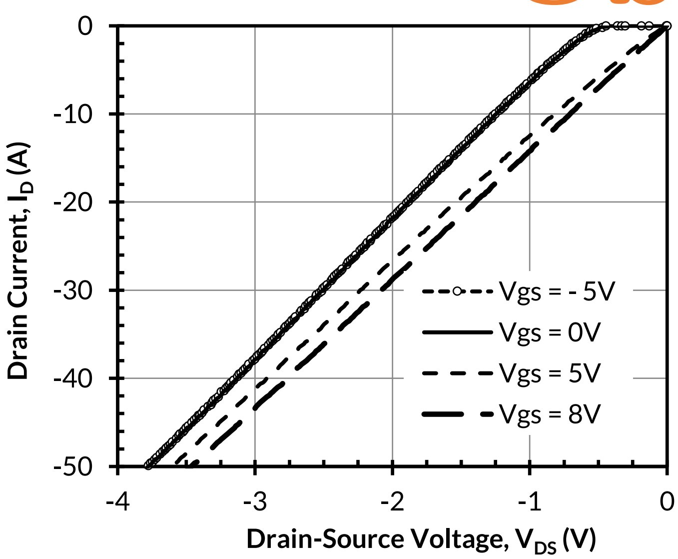



Figure 11. 3rd quadrant characteristics at $T_J$ = 150°C

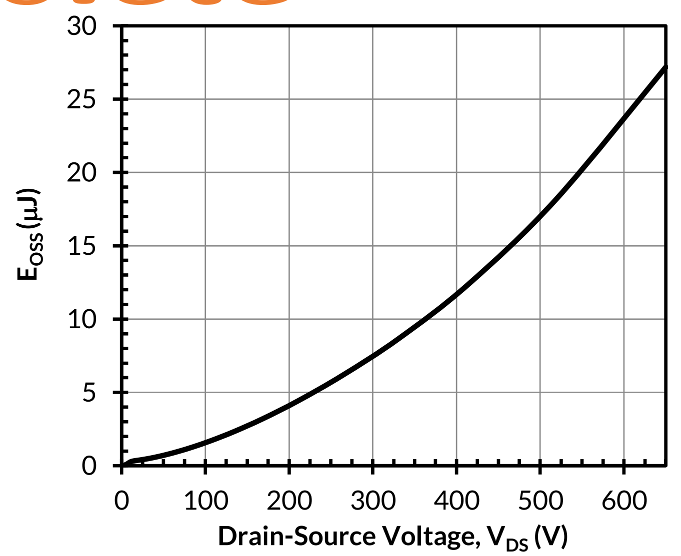
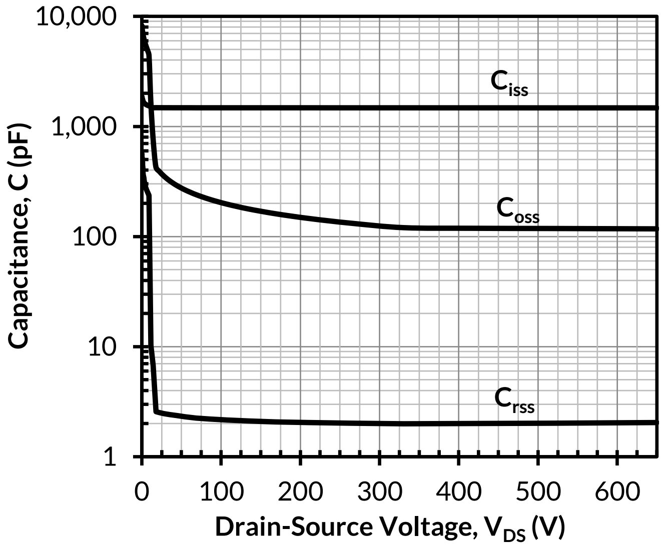



Figure 12. Typical stored energy in $C_{OSS}$ at $V_{GS}$ = 0V



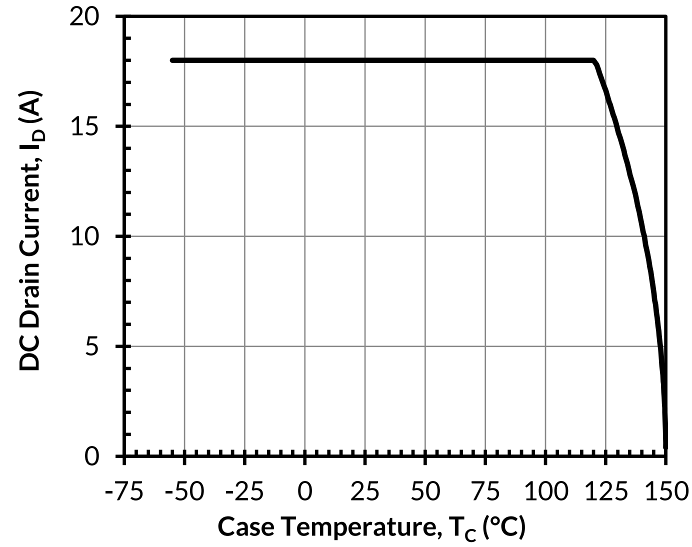
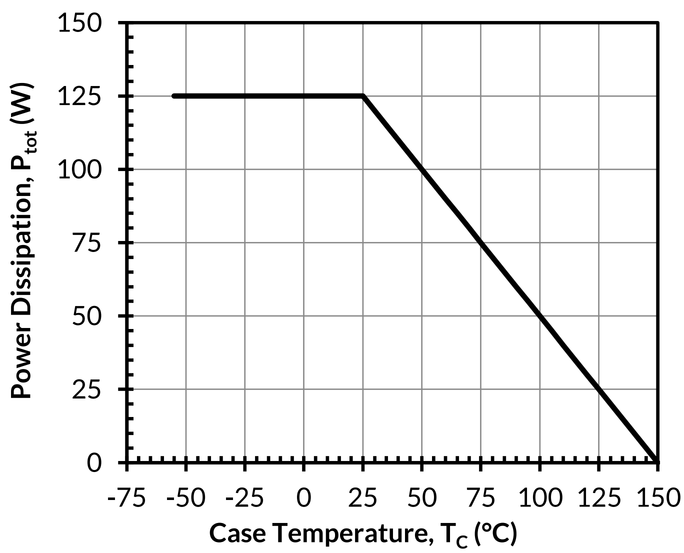




Figure 13. Typical capacitances at f = 100kHz and $V_{GS}$ = 0V

Figure 14. DC drain current derating





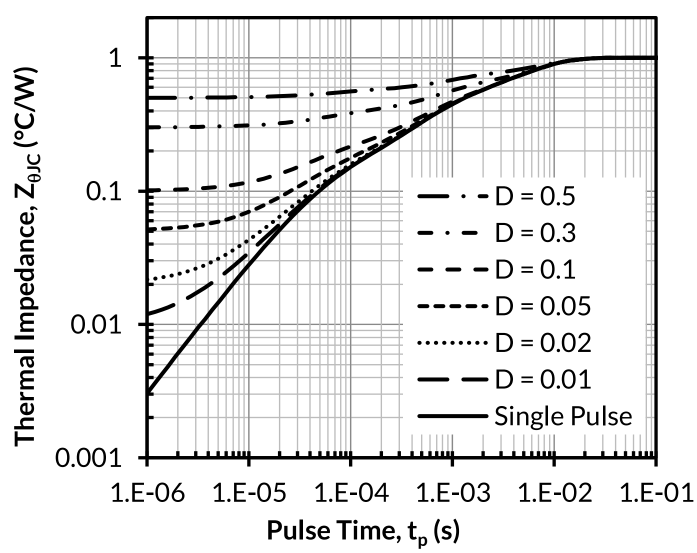




Figure 15. Total power dissipation

Figure 16. Maximum transient thermal impedance

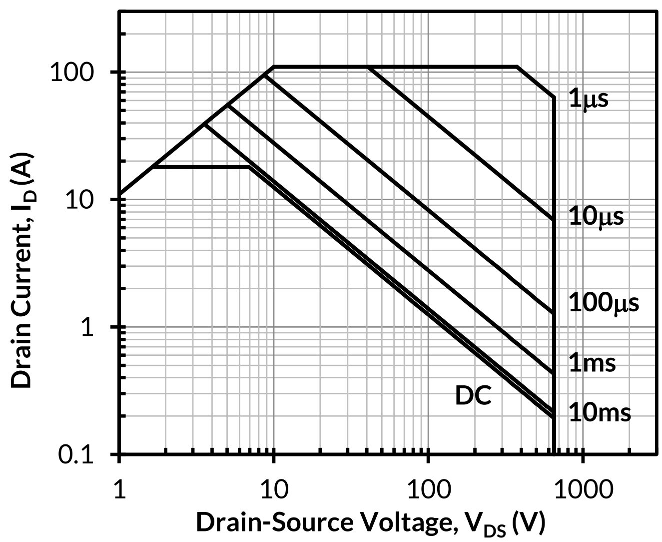



Figure 17. Safe operation area at $T_C$ = 25°C, D = 0, Parameter $t_p$

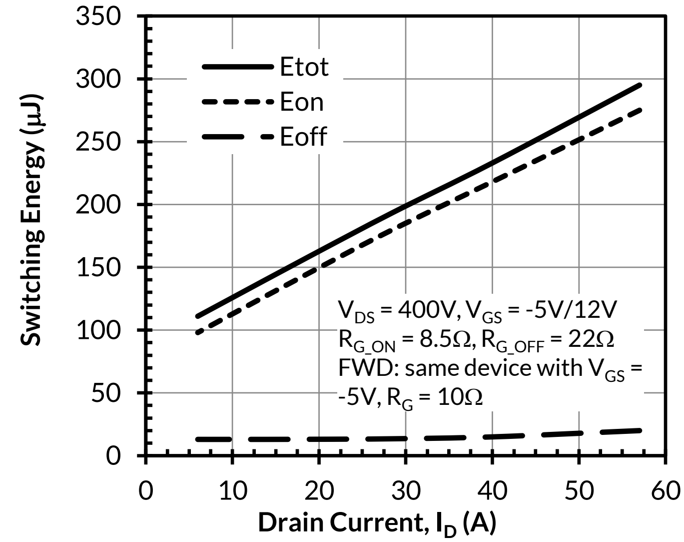



Figure 18. Clamped inductive switching energy vs. drain current at $T_J$ = 25°C



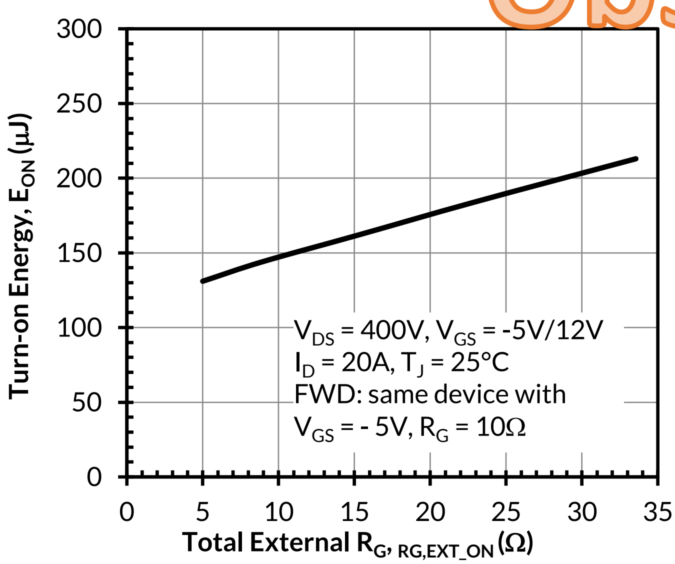



Figure 19. Clamped inductive switching turn-on energy vs. $R_{G,EXT\_ON}$

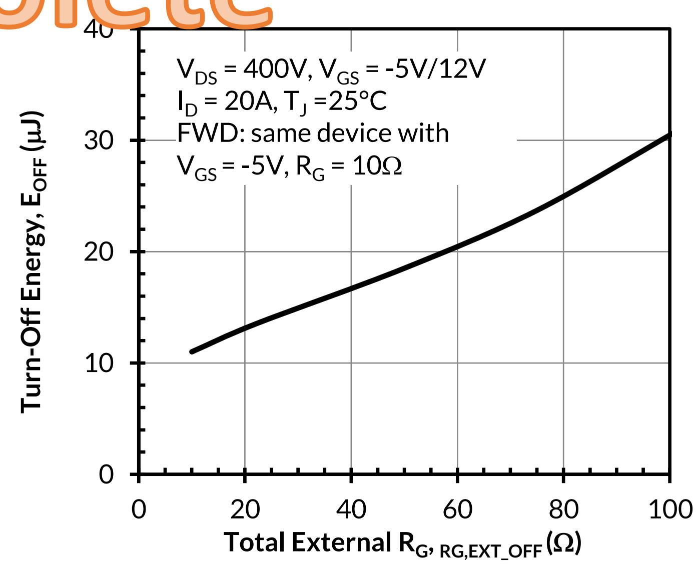



Figure 20. Clamped inductive switching turn-off energy vs. $R_{G,EXT\_OFF}$

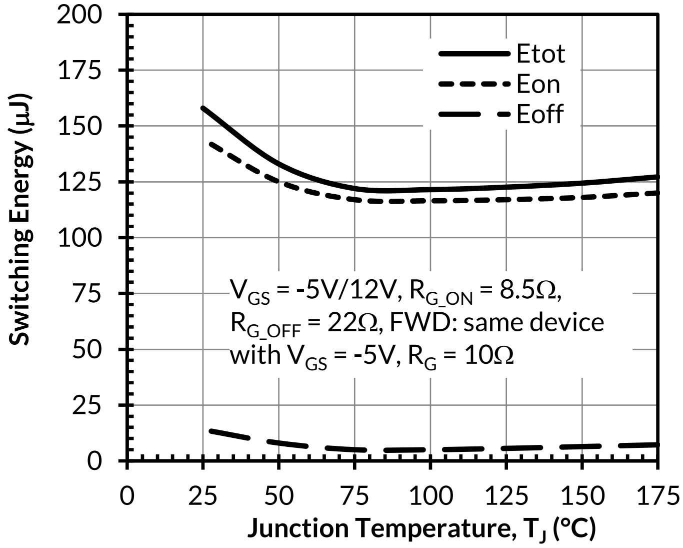



Figure 21. Clamped inductive switching energy vs. junction temperature at $V_{DS}$ = 400V and $I_D$ = 20A

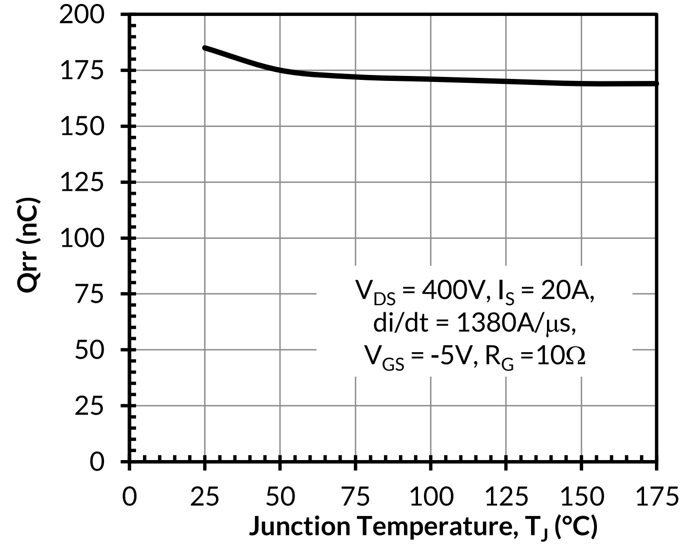



Figure 22. Reverse recovery charge Qrr vs. junction temperature

## Applications Information



SiC FETs are enhancement-mode power switches formed by a high voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ($R_{DS(on)}$), output capacitance ($C_{oss}$), gate charge ($Q_G$), and reverse recovery charge (Qrr) leading to low conduction and switching losses. The SiC FETs also provide excellent reverse conduction capability eliminating the need for an external anti-parallel diode.

Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high dv/dt and di/dt rates. An external gate resistor is recommended when the FET is working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on SiC FET operation, see www.unitedsic.com.

## Disclaimer

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