Mechatronics Product / Process Change Notification

B7530E24B-BSR

June 5, 2023

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Table 1. Change Identification

Product Family / Commercial Product	B7530E24B-BSR
Type of change	Integrated circuit change.
Reason for change	IC LB1868M is no longer availible for mass production.
Description of change	IC change from LB1868M to MLX90411B. No change in motor or fan performance.
Product Line(s) and/or Part Numbers	B7530E24B-BSR
Marking to identify changed product	By lot code
Manufacturing location(s)	China Plant

Table 2. Change Implementation Schedule

Forecasted implementation date for change	June 2023
Forecasted availability date of samples for customer	June 2023
Estimated date of changed product first shipment	June 2023

MLX90411B

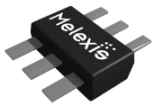
Datasheet

1. Features and Benefits

- All-In-One fan driver, including high sensitivity Hall-effect sensor
- Maximum Motor current up to 1A
- Supply range: [3.2, 40]V
- Low current Standby mode
- Adaptive Commutation control
- Commutation options (Programmable)
  - Maximum Torque
  - Low Acoustic Noise
  - Low Electromagnetic Emissions
- PWM input for on chip speed control:
  - Input frequency: [60 Hz, 100 kHz]
  - Open loop with Max duty cycle limiting
  - Closed loop speed control +/-1.5%
- FG and RD diagnostics output (Programmable)
- Intelligent Start-up (Programmable)
- Current limiting
  - FG/RD open drain output
  - Bridge Output driver
- Protections
  - Locked Rotor protection (Programmable)
  - Over Temperature protection
  - Over Voltage protection
  - Short circuit protection
  - Load dump (40V) protected
  - Pin to Pin Short protection
  - Integrated supply clamp
- Certifications
  - UL/VDE/CE capable
  - K Grade:
    - JEDEC qualified packages
  - L Grade:
    - AEC-Q100-Rev-H qualified packages,
    - Automotive PPAP (PSW)
    - ASIL ready
- **I2C programming**
  - Fast prototyping, End Of line programming

Package variants:

- SOT23-6L with straight leads
- Exposed pad UTDFN6 2.5x2x0.4
  - Ultra-Thin: 0.4mm height



2. Application Examples

- 5V, 12V and 24V fans for Consumer/IT/Home Appliance/Industrial
- Automotive fans on 12V and 24V battery

3. Description

The MLX90411 is a next generation All-In-One single-coil Brushless-DC (BLDC) fan driver, designed according to the Melexis automotive Design-For-Test(DFT) IC-design flow, and automotive package-design flow, targeting zero PPM failure rate in the field.

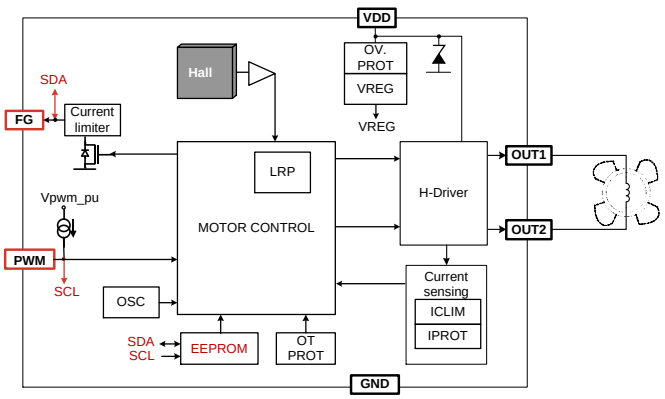
Extensive protections support UL/CE/VDE compliance, and avoid the need for external protection components when applied on an automotive battery.

The MLX90411 comes with the latest generation Adaptive motor control algorithms, which allows getting the best noise and torque performance out of any motor, regardless of the speed/load.

Thanks to small package footprints, the MLX90411 can be used in the smallest fans.

The low RDSon and Current Limiting allow driving of 24V fans up to 15W.

The optional End-Of-Line programming offers lead angle tuning for fast prototyping, and allows customizing the MLX90411 for a wide range of applications.



Contents

4. Ordering Information

Product	Grade	Package	Option Code	Packing Form
MLX90411	K (consumer)	ZE (straight leads)	Bxx xxx	RE
MLX90411	K (consumer)	LD (UTDFN6)	Bxx xxx	RE
MLX90411	L (automotive)	ZE (straight leads)	Bxx xxx	RE
MLX90411	L (automotive)	LD (UTDFN6)	Bxx xxx	RE

Table 1 Order codes

Legend:

Grade Code:	**K: Consumer grade** **L: Automotive grade (supported by PPAP)**
Package Code:	"ZE" for straight leads SOT23 6L package, die face down "LD" for UTDFN6 2x2.5x0.4

Option Code:	• **B- - - - -** : Production reference to MLX90411B
	• **- x x x - -** : Distinct order codes (EEPROM configurations).
	  ○ **– x x 9 - -**: reserved for ordering reprogrammed option codes
	• **- - - - 2/4 - : S**upply Clamping voltage
	  ○ 4: VDDclamp_min = 40V
	  ○ 2: VDDclamp_min = 20V
	• **- - - - - 3/6/8/9** : Current Limit See Electrical Specifications:
	  ○ 3: 330mA
	  ○ 6: 660mA
	  ○ 8: 800mA
	  ○ 9: 960mA

Packing Form:	"RE for Reeling with marking on top side"
Ordering Example:	"MLX90411KZE-BAA-046-RE": Default 24V consumer straight leads SOT, 1-coil fandriver, 40V minimum clamping voltage, ICLIM = 660mA, delivered in Reel.

Table 2 Order code description

5. Pin Definitions and Descriptions

UTDFN6	SOT23-6L	Name		Description
1	6	PWM	Input	Input pin for speed control (open loop and closed loop). SCL: In I2C programming mode: Clock input.
2	5	VDD	Power	
3	4	OUT1	Output	
4	3	OUT2	Output	
5	2	GND	Ground	
6	1	FG	Output (input/output)	Current limited output pin. Can be configured in E2PROM map, as: • FG (Frequency Generator) output • RD (Fan Ready) output SDA: In I2C programming mode: Serial Data I/O
EP		n/c		Not connected. Exposed pad to be shorted to GND on pcb.

Table 3

6. Glossary of Terms

Gauss (G), Tesla (T)	Units for the magnetic flux density – 1 mT = 10 G
PWM	Pulse Width Modulation
DCout	PWM output duty cycle [%] applied on the driver output stage
DCin	PWM input duty cycle [%] applied on the PWM input pin to regulate speed.
LSB	Least Significant Bit
MSB	Most Significant Bit

Table 4

7. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Condition
20V version					
Operating Supply Voltage	V_{DD_20}		18	V	
40V version					
Load dump Voltage	V_{DD_LD}		$V_{DDclamp\_40}$	V	Maximum applied voltage according to ISO7637-2, pulse 5b, Vov2 or Vov3 applied
Operating Supply Voltage	V_{DD_40}		32	V	For UTDFN package consider minimum pin spacing (footprint application note available on demand)
20V and 40V version					
Reverse Supply Voltage	V_{DDREV}	-0.3		V	
FG Output Voltage	V_{FG}	-0.3	V_{FG_CLAMP}	V	Maximum junction temperature (Tj_max) may not be exceeded (see also chapter 8.7 for detailed clamp description)
Reverse FG Output Current	I_{FG}	-50		mA	Max 1 hour, and Maximum junction temperature may not be exceeded
PWM voltage	V_{PWM}	-0.3	V_{DD} + 0.3V	V	
PWM input current	I_{PWM}		10	mA	Current flowing into PWM for VPWM > VDD
OUT1, OUT2 voltage	$V_{OUT1,2}$	-0.3	V_{DD} + 0.3V	V	
Maximum Output Current during LRP	I_{OUT}		I_{CLIM}	mA	Maximum junction operating temperature may not be exceeded. Limited by current limiting
E2PROM word writes End Of Line	$E2_{Write\_EOL}$		20	Write cycles	Maximum allowed word writes, cumulated over all words. Max programming temperature Tj < 50C.
Maximum Operating Junction	T_{j_max}	-40	Tprot	°C	
Storage Temperature Range	T_S	-55	+165	°C	
ESD Sensitivity – HBM	V_{hbm}		6000	V	HBM according AEC-Q100-002
ESD Sensitivity – CDM	V_{cdm}		1000	V	CDM according AEC-Q100-011

Table 5

- Exceeding the absolute maximum ratings may cause permanent damage.
- Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.
- Operation in extended temperature range (i.e. above maximum operating junction temperature and below absolute maximum junction temperature), may cause some analogue parameters to drift outside of the test specification, but chip function is guaranteed by characterisation.
- It is highly recommended for automotive applications (L grade covered by PPAP), to provide the mission profile to Melexis, to verify that the HTOL qualification covers the application requirements.

8. Electrical Specifications

8.1. General Electrical Specifications

Typical values are defined at Tj = +25°C and V_{DD} = 12V, unless otherwise specified

Unless otherwise specified, Min/Max values are valid for:

- Tj = [-40, 150]C
  - Tj_{LZE} = [-40, 125]C
- Applicable operating voltage:
  - V_{DD_40} = [3.2, 32]V
  - For 20V versions: V_{DD_20} = [3.2, 18]V

Electrical Parameter	Symbol	Min	Typ	Max	Units	Conditions
Supply Current	I_{DD}		3.5	5	mA	No load on OUT1, OUT2 and FG/RD output
Standby Supply Current	I_{DD_STDBY}			0.5	mA	DC_{IN} = 0%, DC_{OUT} = 0%, T_J = 25ºC, V_{DD} = 12V
Protections						
Clamping voltage	$V_{DDclamp\_20}$	21	23	26.5	V	IClamp=20mA see SOA Figure 21
Clamping voltage	$V_{DDclamp\_40}$	40	42	44	V	IClamp=20mA see SOA Figure 21
OverVoltage Protection threshold ON	V_{ov1_H}	17.3	18.3	19.3	V	
OverVoltage Protection threshold Hysteresis	V_{ov1_hyst}		1.2		V	
OverVoltage Protection threshold ON	V_{ov2_H}	20.8	22	23.2	V	
OverVoltage Protection threshold Hysteresis	V_{ov2_hyst}		0.9		V	
OverVoltage Protection threshold ON	V_{ov3_H}	33	35	37	V	
OverVoltage Protection threshold Hysteresis	V_{ov3_hyst}		1		V	
OverVoltage debounce time	t_{vov_deb}		80		us	Applying VDD > Vov during t > tvov_deb will disable the driver.
Overvoltage blanking time	t_{vov_blank}		4		ms	Additional Maximum Blanking time starting after the end of the rising slope
Thermal Protection Threshold	T_{PROT}	160	170	180	°C	Junction temperature

OverCurrent Protection HS	I_{PROT}	I_{CLIM} *1.3	I_{CLIM} *1.5	I_{CLIM} *2.2	mA	
OverCurrent Protection LS	I_{PROT}	I_{CLIM} *1.4	I_{CLIM} *1.5	I_{CLIM} *1.75	mA	DC current, T_J = 25°C, V_{DD} = 12V
OverCurrent debounce time	t_{IPROT_deb}		0.5		us	Icoil > Iprot during t > tiprot
Time between OverCurrent retrials	$t_{Iretrial\_PROT}$		5		ms	Auto restart after IPROT event.
Current Limit	I_{CLIM_xx3}	280	330	380	mA	DC current, T_J = 25°C, V_{DD} = 12V
Current Limit	I_{CLIM_xx6}	600	660	720	mA	DC current, T_J = 25°C, V_{DD} = 12V
Current Limit	I_{CLIM_xx8}	720	800	880	mA	DC current, T_J = 25°C, V_{DD} = 12V
Current Limit	I_{CLIM_xx9}	880	960	1050	mA	DC current, T_J = 25°C, V_{DD} = 12V
Current Limit debounce time	$t_{CLIMdeb}$		1.5		us	DC current, Icoil > Iclim during t > tclim
Hall Sensor						
Positive Magnetic Threshold	B_{OP}	0	1.5	3.0	mT	T_J = 150°C
Negative Magnetic Threshold	B_{RP}	-3.0	-1.5	0	mT	T_J = 150°C
PWM / FG						
PWM Input Low Voltage	V_{IL}			1.0	V	
PWM Input High Voltage	V_{IH}	2.3			V	V_{IH} <= VDD
PWM internal pull up voltage	V_{PWMPU}	3	3.3	3.6	V	VDD > 3.6V
PWM internal pull up voltage	V_{PWMPU_LV}	2.7		VDD	V	VDD < 3.6V
PWM internal source current	I_{PWMPU_act}	215	250	275	µA	Active mode
PWM internal source current	I_{PWMPU_sb}	30	50	65	µA	Standby mode
FG (SDA) Input Low Voltage	V_{IL}			1.0	V	in I2C mode
FG (SDA) Input High Voltage	V_{IH}	2.3			V	in I2C mode
FG Output Saturation Voltage	V_{FG_OL}	0.07	0.20	0.40	V	FG – low, I_{FG_OUT} = 6mA
FG Output Saturation Voltage	$V_{FG\_OL\_25}$	0.10	0.27	0.40	V	FG – low, I_{FG_OUT} = 8mA, Tj=25C
FG Output Current Limit	I_{FG_CL}	10	21	35	mA	FG – low, V_{FG} = 5V
FG Output Clamp Voltage	V_{FG_CLAMP}	19.0	21.5	23.5	V	FG – high, I_{FGOUT} = 5mA
FG Output Leakage Current	I_{FG_Leak}	0	0.1	1	µA	T_J = 25°C, V_{FG} = 12V, V_{DD} = 12V
Driver RDSon						
Full Bridge On Resistance	R_{DSON}	1.1	1.5	2.1	Ω	T_J = 25°C, V_{DD} = 12V, I = 0.5A
Full Bridge On Resistance	R_{DSON}	1.2	1.7	2.7	Ω	T_J = 25°C, V_{DD} = 3.2V, I = 0.1A
Full Bridge On Resistance	R_{DSON}		2.3		Ω	T_J = 150°C, V_{DD} = 12V, I = 0.5A
Oscillator						
RCO tolerance	Tol_rco_25	-1.0%		+2.0%		Tj=25C, Vdd=12V, trim accuracy

	Tol_rco	-5.0%		+5.0%		
Package						
Thermal resistance	RTh_{ja1s0p_ZE}		240		°K/W	SOT23: Single layer PCB, JEDEC standard test boards, still air (LFPM=0)
Thermal resistance	RTh_{ja2s2p_ZE}		135		°K/W	SOT23: 4- layer PCB, , still air (LFPM=0)
Thermal resistance	$RTh_{jc\_t\_ZE}$		14		°K/W	SOT23: junction to top
Thermal resistance	$RTh_{jc\_p\_ZE}$		37		°K/W	SOT23: junction to tip of pin 2
Thermal resistance	RTh_{ja1s0p_LD}		310		°K/W	UTDFN6[1]: Single layer PCB, JEDEC standard test boards, still air (LFPM=0)
Thermal resistance	RTh_{ja2s2p_LD}		45		°K/W	UTDFN6[2]: 2s2p, 2 thermal vias, JESD51 standard test board, still air (LFPM=0)
Thermal resistance	Th_{jc_LD}		8		°K/W	UTDFN6[2] junction to center of exposed pad

Table 6

[1] All Rthj for UTDFN6 are valid for footprint with GND pin shorted to the exposed pad on the pcb.

8.2. Timing Specifications

8.2.1. General timings

Electrical Parameter	Symbol	Typ (*)	Units	Comments
Output PWM frequency	F_{OUT}	24.0	kHz	
Output PWM period	t_{PWM}	41.7	us	
Output PWM resolution	DC_{OUT_RES}	8	bit	
Input PWM resolution	DC_{IN_RES}	8	bit	
PWM Input Integration time fast	t_{INT_fast}	21.3	ms	DPWMINT = 0, See E2PROM map PWM input frequency range = [240, 50k]Hz
PWM Input Integration time slow	t_{INT_slow}	85.3	ms	DPWMINT = 1, See E2PROM map PWM input frequency range = [60, 50k]Hz
Minimum duty cycle	DCout_min	2.3%		Minimum output duty cycle

(*)Typical values. For tolerances see oscillator characterisation graphs in paragraphs 11.9 and 11.10.

8.2.2. DCin, DCout calculation, Standby mode

The input integrator converts the signal applied on the PWMIN pin into an 8bit duty cycle: DCIN[7:0], using the integration time t_{INT_X}, selected in the E2PROM map.

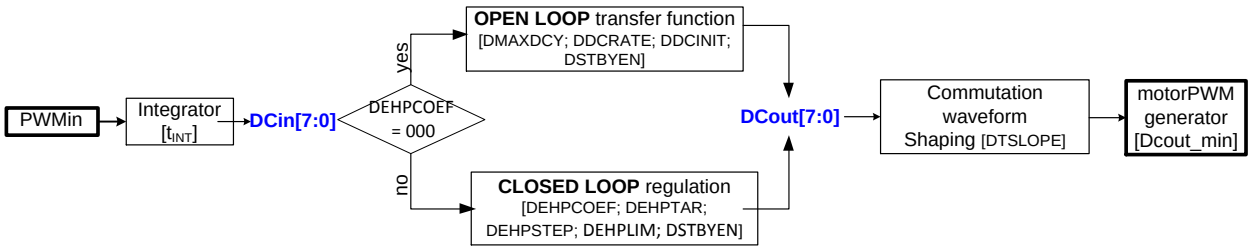


Figure 1: DCin, DCout definition

This implies that the fan does not immediately start when a PWM duty cycle > DCIN_START is applied. For the same reason DCout will not change its speed instantaneously when the PWM input Duty Cycle is modified.

8.2.2.1. Standby mode enabled

When DSTBYEN = 1, the MLX90411 enters standby to reduce standby current consumption.

Parameter	Symbol		Description
Input Duty Cycle Threshold for exit standby/fan start up	DCIN_START	9.0%	MLX90411 exits standby mode, and starts up the fan when DCIN[7:0] > DCIN_START (*)
Input Duty Cycle Threshold to enter standby	DCIN_STOP	7.8%	MLX90411 initiates the procedure to go into standby mode as soon as DCIN[7:0] < DCIN_STOP (**)

Notes:

- (*) In standby mode, the integration time is per default fixed to t_{INT_fast}, regardless of the selected DPWMINT in the EEPROM MAP. Therefore MLX90411 will leave standby mode t_{INT_fast} after applying a duty cycle > DCIN_START on the PWM input pin.

- (**) When DCIN < DCIN_STOP for longer than t_{INT}, the output driver will initiate the procedure to go into standby mode. First the bridge driver is switched to DCout=0% to brake the motor. The DCout=0% is applied until all coil current is gone. Then the bridge driver is switched to Z, and the MLX90411 will switch to standby mode, regardless if the motor is still spinning.

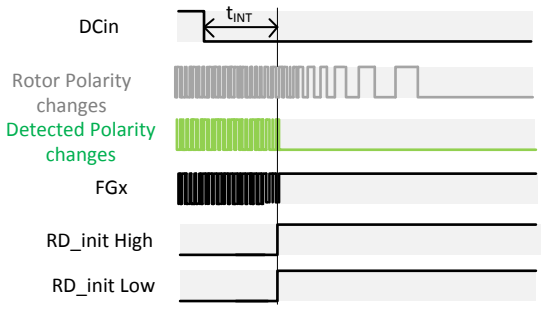


Figure 2 FG pin behaviour when entering Standby

- Standby mode is defined only by the PWM input, regardless if a protection mode is activated. See also paragraph 8.4.5 Forced restart after protection.

8.2.2.2. Standby mode disabled

When DSTBYEN = 0, the MLX90411 will not enter in standby mode, but will maintain the MINSP value down to DCin = 0%.

Note

- The DSTBYEN bit is interacting with the DFGCONFIG bit, and may limit the I2C access as described in below table. See I2C application note for more details.

DSTBYEN	DFGCONFIG	I2C access constraints
1	000: FG 001: FG FREQ DIV 2 111: FG FREQ MULTPL 2 100: RD initialized high 011: Thermometric current mode	No restriction on I2C access.
1	101: RD initialized low	I2C access only after entering standby mode (warm)
0	000: FG 001: FG FREQ DIV 2 111: FG FREQ MULTPL 2 100: RD initialized high 011: Thermometric current mode	I2C access only after POR (cold)
0	101: RD initialized low	After writing the combination of DSTBYEN=0 and DFGCONFIG = 101, the I2C access is blocked. No more I2C-read or -write access is possible.

8.2.3. Open loop transfer function with MAX DCout setting

Open loop speed control is selected in the E2PROM map by setting DEHPCOEF = 000.

E2PROM word 5, bits [12:11] are used to set DDCINIT, and bits [8:3] are used to set DMAXDCY.

- The maximum duty cycle DCoutmax, is calculated as (66 + DMAXDCY*3)/256. See table below.
- The initial duty cycle at start up is defined by the DDCINIT bits. See E2PROM map

DMAXDCY		DCOUTmax		DMAXDCY		DCOUTmax		DMAXDCY		DCOUTmax		DMAXDCY		DCOUTmax
000000	0	25.8%		010000	16	44.5%		100000	32	63.3%		110000	48	82.0%
000001	1	27.0%		010001	17	45.7%		100001	33	64.5%		110001	49	83.2%
000010	2	28.1%		010010	18	46.9%		100010	34	65.6%		110010	50	84.4%
000011	3	29.3%		010011	19	48.0%		100011	35	66.8%		110011	51	85.5%
000100	4	30.5%		010100	20	49.2%		100100	36	68.0%		110100	52	86.7%
000101	5	31.6%		010101	21	50.4%		100101	37	69.1%		110101	53	87.9%
000110	6	32.8%		010110	22	51.6%		100110	38	70.3%		110110	54	89.1%
000111	7	34.0%		010111	23	52.7%		100111	39	71.5%		110111	55	90.2%
001000	8	35.2%		011000	24	53.9%		101000	40	72.7%		111000	56	91.4%
001001	9	36.3%		011001	25	55.1%		101001	41	73.8%		111001	57	92.6%
001010	10	37.5%		011010	26	56.3%		101010	42	75.0%		111010	58	93.8%
001011	11	38.7%		011011	27	57.4%		101011	43	76.2%		111011	59	94.9%
001100	12	39.8%		011100	28	58.6%		101100	44	77.3%		111100	60	96.1%
001101	13	41.0%		011101	29	59.8%		101101	45	78.5%		111101	61	97.3%
001110	14	42.2%		011110	30	60.9%		101110	46	79.7%		111110	62	100.0%
001111	15	43.4%		011111	31	62.1%		101111	47	80.9%		111111	63	100.0%

Table 7 DCout_Max look up table See E2PROM map

Transfer function Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Input Duty Cycle Range	DC_{IN_LIN}	10.2		97.8	%	Linear zone of the transfer curve

Table 8

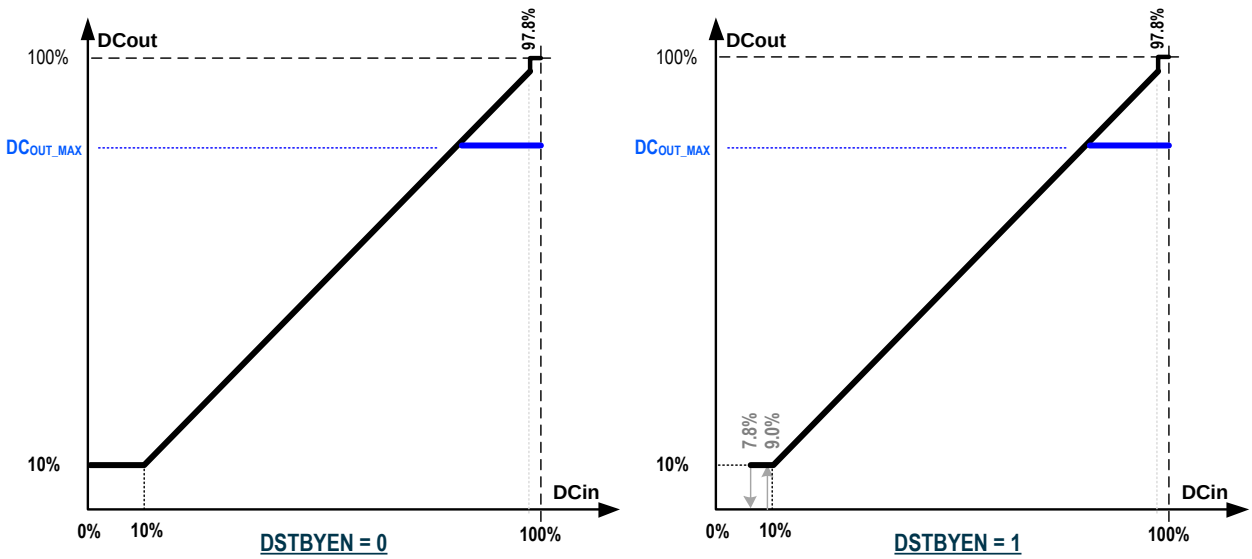


Figure 3: Open loop transfer function

8.2.4. Closed loop speed control

In closed loop control several regulations speeds can be selected using DEHPCOEF. Maximum speed is set using parameters DEHPTAR, DEHPSTEP, **DSPEED**. The actual speed can be regulated between MINSP and MAXSP via the PWM input pin. *See E2PROM map.*

Electrical Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Input Duty Cycle Range	DCIN_LIN	12.5		100	%	Input range corresponding to Linear transfer curve
Closed loop Max Speed range	MAXSP_e	2,835	-	90,000	e-rpm	Electrical speed Set by DEHPTAR, DEHPSTEP, DSPEED
Closed loop Max Speed range, DSPEED=0	*MAXSP_2pp*	*1,417*	-	*22,500*	*m*-rpm	*Mechanical speed for 2pole pairs motor, calculated as electrical speed DIV 2*
Closed loop Max Speed range, DSPEED=1	*MAXSP_2pp*	*1,895*	-	*45,000*	*m*-rpm	*Mechanical speed for 2pole pairs motor, calculated as electrical speed DIV 2*
Closed loop Max Speed range, DSPEED =0	*MAXSP_4pp*	*708*	-	*11,250*	*m*-rpm	*Calculated Mechanical speed for 4pole pairs motor, calculated as electrical speed DIV 4*
Closed loop Max Speed range, DSPEED =1	*MAXSP_4pp*	*947*	-	*22,500*	*m*-rpm	*Calculated Mechanical speed for 4pole pairs motor, calculated as electrical speed DIV 4*
Minimum Speed	MINSP_low		12.5%			DEHPLIM =1 Minimum speed % of the selected max speed
Minimum Speed	MINSP_high		20%			DEHPLIM =0 Minimum speed % of the selected max speed

Table 9

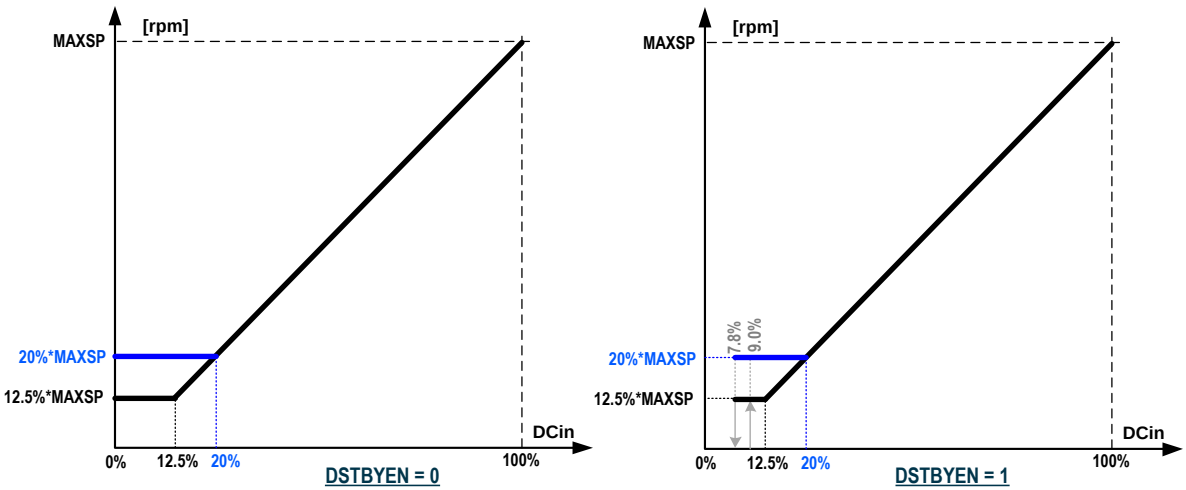


Figure 4: Closed loop speed control with minimum speed options for a speed set to MAXSP

DEHPSTEP	DEHPTAR	MAXSP_2pp	Res. Err, +/-%		DEHPSTEP	DEHPTAR	MAXSP_2pp	Res. Err, +/-%
0	0	22,500	0.8%		**2**	0	5,625	0.8%
	1	22,154	0.8%			1	5,538	0.8%
	8	20,000	0.7%			8	5,000	0.7%
	9	19,726	0.7%			9	4,932	0.7%
	16	18,000	0.6%			16	4,500	0.6%
	17	17,778	0.6%			17	4,444	0.6%
	26	16,000	0.6%			26	4,000	0.6%
	27	15,824	0.5%			27	3,956	0.5%
	46	13,091	0.5%			46	3,273	0.5%
	47	12,973	0.5%			47	3,243	0.5%
	56	12,000	0.4%			56	3,000	0.4%
	57	11,901	0.4%			57	2,975	0.4%
	58	11,803	0.4%			58	2,951	0.4%
	62	11,429	0.4%			62	2,857	0.4%
	63	11,339	0.4%			63	2,835	0.4%
DEHPSTEP	DEHPTAR	MAXSP_2pp	Res. Err, +/-%		**DEHPSTEP**	DEHPTAR	MAXSP_2pp	Res. Err, +/-%
1	0	11,250	0.8%		**3**	0	2,813	0.8%
	1	11,077	0.8%			1	2,769	0.8%
	8	10,000	0.7%			8	2,500	0.7%
	9	9,863	0.7%			9	2,466	0.7%
	16	9,000	0.6%			16	2,250	0.6%
	17	8,889	0.6%			17	2,222	0.6%
	26	8,000	0.6%			26	2,000	0.6%
	27	7,912	0.5%			27	1,978	0.5%
	46	6,545	0.5%			46	1,636	0.5%
	47	6,487	0.5%			47	1,622	0.5%
	56	6,000	0.4%			56	1,500	0.4%
	57	5,950	0.4%			57	1,488	0.4%
	58	5,902	0.4%			58	1,475	0.4%
	62	5,714	0.4%			62	1,429	0.4%
	63	5,669	0.4%			63	1,417	0.4%

Table 10 Closed loop speed control: MAXSP calculation examples for 2 pole pairs motor, DSPEED =0

Calculation formula, as function of the number of pole pairs (pp):

- MAXSP = (120/PP * F_{OUT}) / (2^(DEHPSTEP) * (**64** + DEHPTAR))

For instance for DEHPSTEP=2, DEHPTAR=56

- for 2pole pairs motor = 120/2*24e3 / (2^DEHPSTEP * (64+DEHPTAR) = 3000 mechanical rpm
- for 4pole pairs motor = 120/4*24e3 / (2^DEHPSTEP * (64+DEHPTAR) = 1500 mechanical rpm

DEHPSTEP	DEHPTAR	MAXSP_2pp	Res.Err,+/-%		DEHPSTEP	DEHPTAR	MAXSP_2pp	Res.Err,+/-%
0	1	43,636	1.5%		2	1	10,909	1.5%
	2	42,353	1.5%			2	10,588	1.5%
	16	30,000	1.0%			8	9,000	1.3%
	17	29,388	1.0%			9	8,780	1.2%
	25	25,263	0.9%			16	7,500	1.0%
	26	24,828	0.9%			17	7,347	1.0%
	32	22,500	0.8%			26	6,207	0.9%
	33	22,154	0.8%			27	6,102	0.8%
	36	21,176	0.7%			46	4,615	0.6%
	37	20,870	0.7%			47	4,557	0.6%
	40	20,000	0.7%			56	4,091	0.6%
	62	15,319	0.5%			62	3,830	0.5%
	63	15,158	0.5%			63	3,789	0.5%
DEHPSTEP	**DEHPTAR**	**MAXSP_2pp**	**Res.Err,+/-%**		**DEHPSTEP**	**DEHPTAR**	**MAXSP_2pp**	**Res.Err,+/-%**
1	1	21,818	1.5%		3	1	5,455	1.5%
	2	21,176	1.5%			2	5,294	1.5%
	3	20,571	1.4%			3	5,143	1.4%
	61	7,742	0.5%			61	1,935	0.5%
	62	7,660	0.5%			62	1,915	0.5%
	63	7,579	0.5%			63	1,895	0.5%

Table 11 Closed loop speed control: MAXSP calculation examples for 2 pole pairs motor, DSPEED =1

Calculation formula, as function of the number of pole pairs (pp):

- MAXSP = (120/PP * F_{OUT}) / (2^(DEHPSTEP) * (**32** + DEHPTAR))

For instance for DEHPSTEP=2, DEHPTAR=56

- for 2pole pairs motor = 120/2*24e3 / (2^DEHPSTEP * (32+DEHPTAR) = 4091 mechanical rpm
- for 4pole pairs motor = 120/4*24e3 / (2^DEHPSTEP * (32+DEHPTAR) = 2045 mechanical rpm

Notes:

- "Res. Err, +/-%": Refers to the Resolution error in %.
  For instance DEHPTAR=0 corresponds to the highest speed for a given DEHPSTEP. Therefor the step corresponds to the highest resolution error

- Minimum speed:
  - Theoretically the minimum closed loop speed can be found for the biggest DEHPSTEP, and the biggest DEHPTAR, and for a PWM input of 12.5%.
  - However mind that the minimum allowed operating speed -for which stable operation is guaranteed - is defined by the setting of the DSPEED bit in the *E2PROM map*..
  - For instance at the lowest value of MAXSP_2pp = 1417rpm, 12.5% PWMinput corresponds to 177rpm, which is below the minimum speed at which stable speed is guaranteed (234rpm).

- In case of closed-loop speed control:
  - the initial Duty cycle at start up is the percentage selected with DEHPINIT. *See E2PROM map*
  - During start up the DCout change rate is fixed at 110%/s. See also Figure 17.

- DEHPCOEF defines the speed of the regulation loop for closed control. Larger “division of error” means less compensation for error, meaning slower regulation.

8.2.4.1. Speed regulation

DEHPCOEF defines the speed of the regulation loop for closed control. Larger “division of error” means less compensation for error, meaning slower regulation.

DEHPCOEF	Division	GUI description
1 (001)	4	Fastest
2 (010)	8	Faster
3 (011)	16	Fast
4 (100)	32	Typical
5 (101)	64	Slow
6 (110)	128	Slower
7 (111)	256	Slowest

8.2.5. Locked Rotor Protection

If the fan driver did not detect a single transition in the magnetic field within t_{ON}, the bridge driver will switch to Z.

- **t_{ON}_start:** t_{ON} during start-up. **DLRPTON[1:0]** defines t_{ON}_start. See E2PROM map.
- **t_{ON}_run:** t_{ON} during normal operation (after start-up) is fixed at 0.33s

Also two different Toff values are considered, allowing fast start up trials to be combined with a longer delay time for cooling down of the fan, and/or for diagnostics by a remote controller:

- **t_{OFF}_trial:** Toff during trials. t_{OFF}_trial = t_{ON}_start
- **t_{OFF}_diagn:** t_{OFF} in between trials, or in case no retrials are configured (see bottom sequence in below fig. t_{OFF}_diagn can be set in a wide range using parameter DLRPRAT.

  t_{OFF}_diagn = t_{OFF}_start * **DLRPRAT**

- **DLRPTRI1:** Defines number of trials at first start up attempt
- **DLRPTRI2:** Defines number of trials for 2nd and later trial attempts

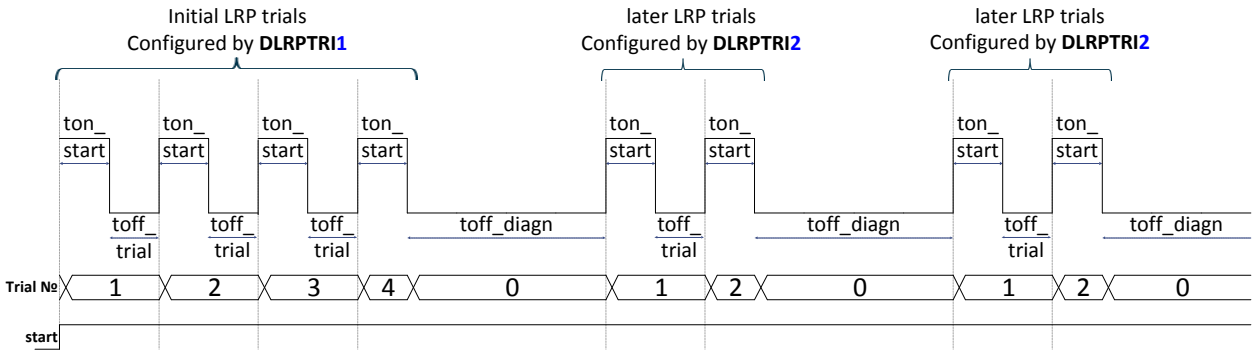


Figure 5 Start up programming options

Below table provides an overview of the t_{OFF}_diagn timing for any combination of E2PROM parameters DLRPTON and DLRPRAT.

tOFF_diagn_nom = Ratio * tON _start								
	DLPRAT Ratio							
tON_start [s]	8	10	12	16	24	28	32	36
0.33	2.6	3.3	4.0	5.3	7.9	9.2	10.6	11.9
0.43	3.4	4.3	5.2	6.9	10.3	12.0	13.8	15.5
0.51	4.1	5.1	6.1	8.2	12.2	14.3	16.3	18.4
1.02	8.2	10.2	12.2	16.3	24.5	28.6	32.6	36.7
tOFF_diagn_min = Ratio * tON _start * 0.95	**> 10s**							
	DLPRAT Ratio							
tON_start [s]	8	10	12	16	24	28	32	36
0.31	2.5	3.1	3.8	5.0	7.5	8.8	10.0	11.3
0.41	3.3	4.1	4.9	6.5	9.8	11.4	13.1	14.7
0.48	3.9	4.8	5.8	7.8	11.6	13.6	15.5	17.4
0.97	7.8	9.7	11.6	15.5	23.3	27.1	31.0	34.9

Table 12 t_{OFF}_diagn_nom calculation examples

In case of diagnostics by a remote controller the timing tolerance should be taken into account, therefore t_{OFF}_diagn_min is calculated as t_{ON}_start*0.95*DLRPRAT. For instance for MLX90411 configured with t_{ON}_start = 0.51s, and DLRPRAT Ratio t_{OFF}_diag/ t_{ON}_start = 24, the minimum t_{OFF}_diagn time = 11.6s.

8.2.5.1. Forced restart after Locked Rotor protection

t_{OFF} timing can be overruled by an external CPU.

See also paragraph 8.4.5 Forced restart after protection.

8.3. Current Limit

The current limit (ICLIM) cuts the output PWM duty cycle DCout_calc, which is calculated by the motor control algorithm, as soon as the ICLIM threshold has been reached:

The high side FET is switched OFF, and the Low Side FET is switched on, to recirculate the current. The motor control is not interrupted. The examples in Figure 6 show the condition with PWM applied on OUT1, and OUT2 switched low.

- **CASE 1. Icoil (DCout_Calc) < ICLIM (left picture in Figure 6**)
  The motor coil current is not reaching the ICLIM threshold, the output duty cycle results from the control algorithm:

  DCout_calc = t_{PWMON}/t_{PWM}

- **CASE 2. Icoil(DCout_Calc) > ICLIM (middle picture in Figure 6)**
  The motor coil current is limited by ICLIM, and the resulting output duty cycle which resulted from the control algorithm (DCout_calc), is truncated to:

  DCout_ICLIM = t_{PWMON}/t_{PWM} < DCout_calc.

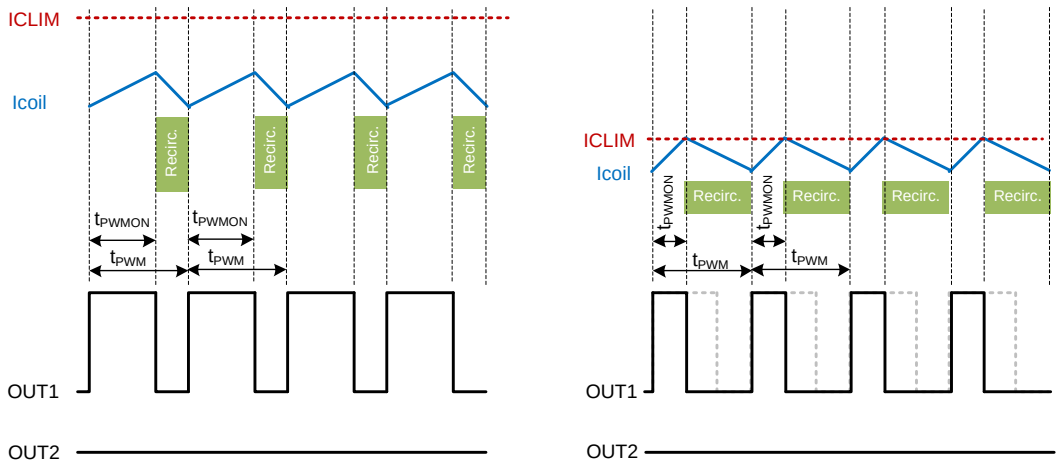


Figure 6 ICLIM current limiting

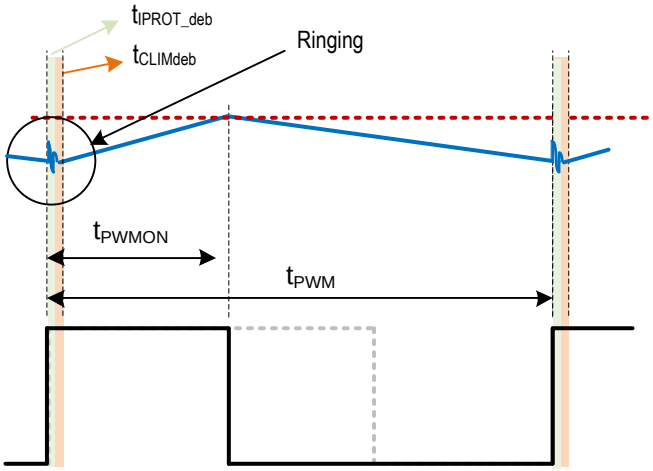


Figure 7 ICLIM Current-Limiting, and Over-Current debouncing

In Figure 7, the debounce timings for the overcurrent protection (t_{IPROT_deb}), and for the current limiting ($t_{CLIMdeb}$) are shown. During these debounce times respectively the IPROT and ICLIM are disabled, to avoid false triggering due to ringing.

8.4. Protections

8.4.1. Locked Rotor protection

See 8.2.5 Locked Rotor Protection

8.4.2. Over-temperature Protection

When the junction temperature of the MLX90411 reaches the over-temperature protection threshold Tprot, the half bridge drivers will switch to Z.

When the junction temperature of the MLX90411 drops below Tprot, the fan driver will wait for Toff, before restarting the fan. This Toff delay timing can be overruled by an external CPU (see below)

8.4.3. Over-current protection

8.4.3.1. Over-current protection on output driver

In case the short circuit protection on the OUTPUT drivers is triggered, the output driver will switch to Z.

The MLX90411 is protected against short circuit connection:

- Between OUT1 and OUT2.
- Between OUT1 and VDD, OUT1 or GND.
- Between OUT2 and VDD, OUT2 or GND.

The way an overcurrent event is handled, is defined by bit DIPROTRPT, see E2PROM map.

- DIPROTRPT = 0, then fan driver will remain in Z until protection is reset by POR
- DIPROTRPT = 1, then the MLX90411 will permanently try to start the fan, each time with max 3 trials interleaved with Toff_diagn

Over current protection debouncing time is ~0.5us. 5ms after an OC protection is triggered the output driver will attempt to restart. A maximum of three start-up trials will be attempted. If the over current protection has been triggered for 3 times within 41ms, the MLX90411 will move to the state defined by DIPROTRPT bit.

Summary:

- In case of DIPROTRPT = 0, this means maximum 3 overcurrent events will take place before remaining in Z state.
- In case of DIPROTRPT = 1, the MLX90411 will permanently retry to start.

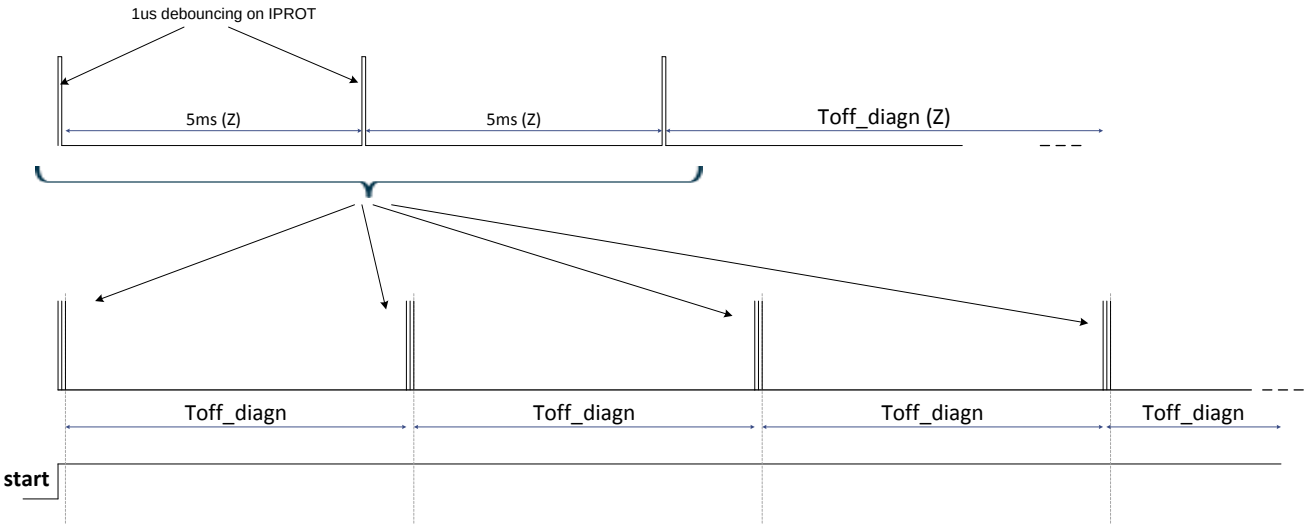


Figure 8 IPROT timings for DIPROTRPT = 1

8.4.3.2. Short circuit protection on other pins

The MLX90411 is protected for Short circuits between any neighbouring pin combinations on either side of the package.

Pin #	Name	Name	Pin #
1	FG / RD	PWM	6
2	GND	VDD	5
3	OUT1	OUT2	4

This means short circuit protections are available

- Between FG/RD and GND
- Between PWM and VDD.

Shorts between these pins

- Will not cause damage to the fan driver
- Will not switch the bridge driver to Z

Pin #	Name	Remarks
1-2	FG/RD – GND	In case FG is shorted to GND, the remote fan controller may consider the fan is in LRP. In case RD is shorted to GND, the remote fan controller will NOT detect a possible LRP condition.
5-6	PWM - VDD	In case PWM is shorted to VDD, the input duty cycle will be interpreted as DCin=100%, and may affect the speed.

8.4.4. Over-Voltage Protection

Activation

When the voltage on the VDD pin exceeds the set overvoltage threshold (Vovx), the driver will switch to Z.

Resuming operation

Depending on motor rotation speed there are two methods to resume driving, when the voltage level drops below the Vovx – Vovx_hyst level:

1) Motor rotation speed >= speed threshold as defined by DSPEED. In this case driving is resumed.

2) Motor rotation speed < speed threshold as defined by DSPEED. In this case the motor is assumed to have stopped. The fan will restart according to the soft start configuration settings, similar as in normal start-up.

Filtering:

- Debouncing window: The MLX90411 always applies debouncing windows to avoid false triggers.
- Blanking: During Blanking time, any Vov-events detected during the debouncing windows are neglected.
    - Vov protection is always blanked during the falling slope, the Flat and the Rising slope of each commutation (See Figure 9 Vov blanking/debounce filtering: CASE 1)
    - In case of filtered Overvoltage protection, an additional blanking time of tvov_blank = 4ms, is initiated at the start of tdrive.
        - ⇨ CASE 2: tdrive < tvov_blank:

          The blanking is removed for one tvov_deb window, just before the falling slope.
        - ⇨ CASE 3: tdrive > tvov_blank,

          The blanking time expires after tvov_blank. Until the end of tdrive the Overvoltage protection will react to an overvoltage event respecting the tvov_deb window.

Notes:

- Mind that the overvoltage values are specified on the VDD pin. In case a reverse voltage protection diode is applied, the supply voltage level on the fan connector pin is different from the voltage on the VDD pin.
- For the 20V-version (MLX90411xxx xxx 02x) the overvoltage protection should be set to Vov1.

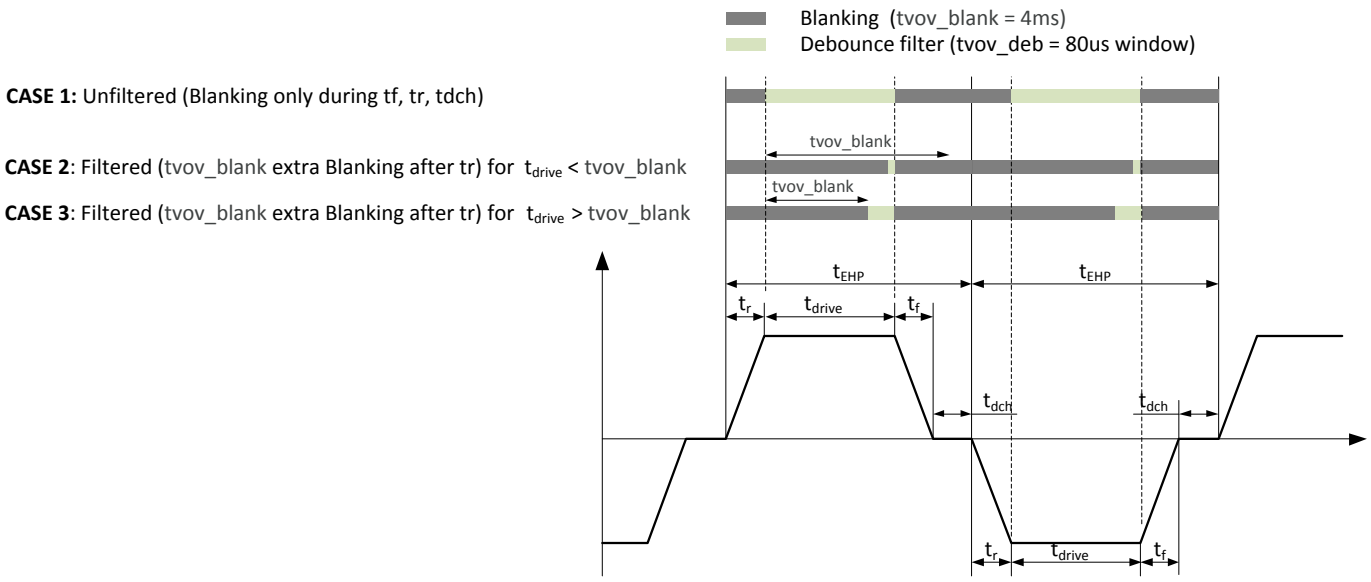


Figure 9 Vov blanking/debounce filtering

8.4.5. Forced restart after protection

When standby mode is enabled (DSTBYEN = 1), the protection timings may be overruled, and an earlier restart may be enforced by an external controller. In order to do so, the controller can pull the PWM input pin low for a time > 2* t_{INT}. By going into standby mode all protections flags are reset, and the MLX90411 can be restarted.

Note: Such forced restart is not possible when standby mode is disabled (DSTBYEN = 0).

8.4.6. Safety, ASIL

MLX90411 Safety Manual can be provided on request.

8.5. Motor Control

8.5.1. Soft-Switching Slope definition

Different Soft-Switching commutation slopes can be configured using parameter DTSLOPE[1:0], see E2PROM map.
The slope duration is automatically adjusted to the motor speed to realize the programmed Slope with $t_{FALL} = t_{RISE}$ at any speed. Therefore the change in PWM DCout duty cycle per PWM period depends on the fan speed, and the selected slope options.

Notes:

- Minimum t_{disch} value is one DCout PWM period (= t_{PWM}). (see next paragraph).
- T_{EHP} = Electrical Half Period = Torque Period (180 electrical degrees)
- "Slope": Refers to "Rising" or "Falling" slope of an EHP in case of soft-switching. Rising and Falling slopes are symmetrical.
- The actual output duty cycle during a slope is the value which is in the PWM counter at the start of the PWM period. This has some consequences as can be seen in the below figures B and C where soft-switching is applied: The first PWM duty cycle value of the rising edge is per definition 0%. Therefore the resulting minimum "Flat" is always at least 2* t_{PWM} in case soft switching is applied:
    - One PWM period (t_{PWM}) for tdisch + the first PWM period (t_{PWM}) of the rising edge.
    - This may appear in the current shape as a significant lag angle at high speeds. Therefore some lead time may be recommended to be applied.
- The minimum possible duty cycle (DCout) is limited by the dead-time of the switching of the LS FET and the HS FET. Therefore DCout values smaller than 2.3% are also rounded to zero. This can become visible with super-soft switching at low DCout duty cycles (example C).

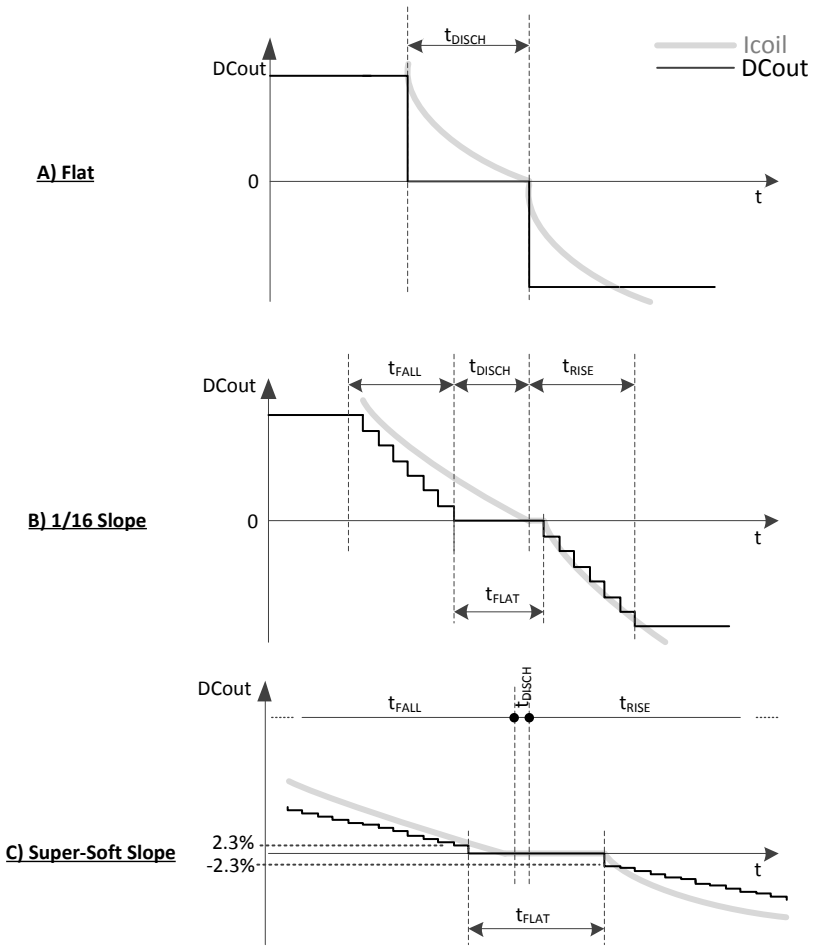


Figure 10: Rising/Falling Slope definition

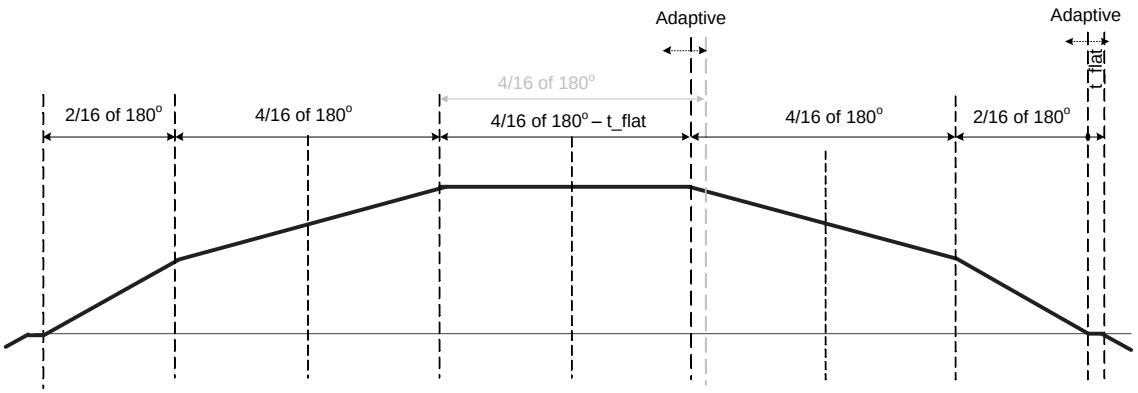


Figure 11: Super-Soft Slope commutation

DTSLOPE	Parameter	Tfall = Trise	Max t_{FALL} = t_{RISE}
00	Flat	0	n/a
01	1/16 Slope	1/16 of tEHP	2.6ms
10	2/16 Slope	2/16 of tEHP	5.2ms
11	Super soft	6/16 of tEHP	10.4ms

Table 13: DTSLOPE Commutation parameters

8.5.2. Adaptive algorithm with programmable lead time

The Soft-Switching Slopes are realized using PWM duty-cycle output control for minimum power losses and maximum motor efficiency. The motor voltage is controlled as VDD*DCout. The coil current may follow the motor voltage variation depending on coil inductance and present BEMF voltage. Therefore the optimal hall sensor position depends on the motor coil inductance, BEMF strength, motor speed … when using fixed commutation timings.
The MLX90411 features an **Adaptive falling slope algorithm**, which allows ensuring optimal commutation for any motor design at any speed. The algorithm initiates the falling edge of the commutation based on current measurement of the coil current at the start of the rising slope. As the falling edge shape is fixed, using parameter DTSLOPE, an advance of the falling edge implies an increase of the flat part of the commutation, represented in above images as an extra time the coil current gets to discharge from the coil: t_{disch}.

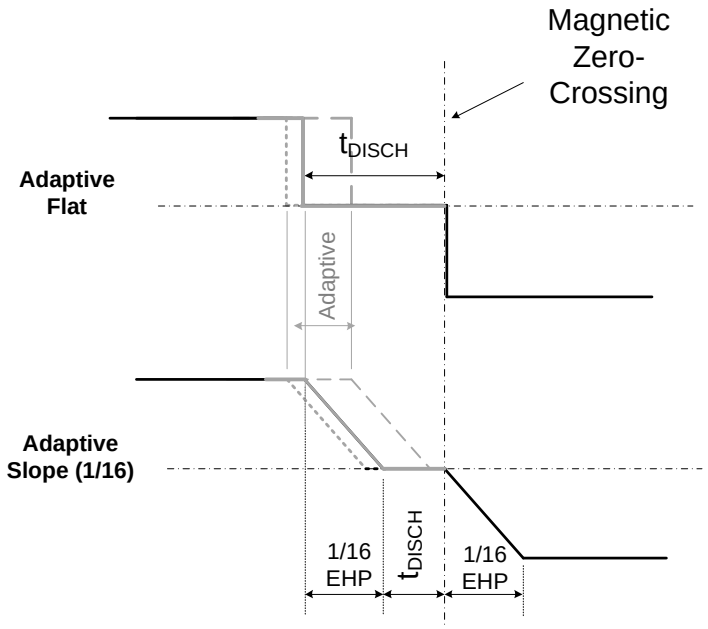


Figure 12: Adaptive commutation

The rising edge of the commutation will take place at a time defined by the magnetic zero crossing. A fixed **lead time** offset t_{LEAD} can be applied. In this case the rising edge is initiated t_{LEAD} before the hall sensor detects the change in magnetic field.

Note: The adaptive falling edge control is applied independent of the fixed lead time offset which is applied on the rising edge only.

The adaptive algorithm with programmable lead time is applied only from a minimum speed, defined by the E2PROM bit **DSPEED**. The resolution of the lead time also depends on the selected value for bit DSPEED. Below table gives an over of the resulting electrical angle for a certain fan speed. DSPEED =1 is not recommended for very low speed fans, while DSPEED0=0 is not recommended for high speed fans.

DTLEAD	Lead time [us]	Mechanical speed [rpm] (2pole pairs motor)																	
		1,000	1,500	2,000	2,500	3,000	3,500	4,000	4,500	5,000	6,000	7,000	8,000	10,000	12,000	15,000	20,000	25,000	28,000
0	0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
1	20.8	0.2	0.4	0.5	0.6	0.7	0.9	1.0	1.1	1.2	1.5	1.7	2.0	2.5	3.0	3.7	5.0	6.2	7.0
2	41.6	0.5	0.7	1.0	1.2	1.5	1.7	2.0	2.2	2.5	3.0	3.5	4.0	5.0	6.0	7.5	10.0	12.5	14.0
3	62.4	0.7	1.1	1.5	1.9	2.2	2.6	3.0	3.4	3.7	4.5	5.2	6.0	7.5	9.0	11.2	15.0	18.7	21
7	146	1.7	2.6	3.5	4.4	5.2	6.1	7.0	7.9	8.7	10.5	12.2	14.0	17.5	21	26	35	44	49
15	312	3.7	5.6	7.5	9.4	11.2	13.1	15.0	16.8	18.7	22	26	30	37	45				
16	333	4.0	6.0	8.0	10.0	12.0	14.0	16.0	18.0	20.0	24	28	32	40	48				
24	499	6.0	9.0	12.0	15.0	18.0	21	24	27	30	36	42	48						
32	666	8.0	12.0	16.0	20.0	24	28	32	36	40	48								
40	832	10.0	15.0	20.0	25	30	35	40	45	50									
48	998	12.0	18.0	24	30	36	42	48											
56	1165	14.0	21	28	35	42	49												
63	1310	15.7	24	31	39	47													

Calculated Lead angle for DSPEED = 0

DTLEAD	Lead time [us]	Mechanical speed [rpm] (2pole pairs motor)																	
		1,000	1,500	2,000	2,500	3,000	3,500	4,000	4,500	5,000	6,000	7,000	8,000	10,000	12,000	15,000	20,000	25,000	28,000
0	0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
1	41.6	0.5	0.7	1.0	1.2	1.5	1.7	2.0	2.2	2.5	3.0	3.5	4.0	5.0	6.0	7.5	10.0	12.5	14.0
2	83.2	1.0	1.5	2.0	2.5	3.0	3.5	4.0	4.5	5.0	6.0	7.0	8.0	10.0	12.0	15.0	20.0	25	28
3	125	1.5	2.2	3.0	3.7	4.5	5.2	6.0	6.7	7.5	9.0	10.5	12.0	15.0	18.0	22	30	37	42
7	291	3.5	5.2	7.0	8.7	10.5	12.2	14.0	15.7	17.5	21	24	28	35	42				
15	624	7.5	11.2	15.0	18.7	22	26	30	34	37	45								
16	666	8.0	12.0	16.0	20.0	24	28	32	36	40	48								
24	998	12.0	18.0	24	30	36	42	48											
32	1331	16.0	24	32	40	48													
40	1664	20.0	30	40	50														
48	1997	24	36	48															
56	2330	28	42																
63	2621	31	47																

Table 14: Calculated electrical lead angle corresponding to a DTLEAD setting at a given mechanical speed.

8.6. Magnetic definition

Parameter	Test Conditions	OUT 1	OUT2	FG
South pole	$B > B_{OP}$	Low	High	High
North pole	$B < B_{RP}$	High	Low	Low

Output behaviour versus magnetic pole, magnet facing top side of the package (see par 12 Package Information)

8.7. FG (RD) output

The FG open drain output pin can be configured by setting the corresponding bit in the E2PROM map.

8.7.1. FG Protections

The FG pin is protected by a current limit and by a voltage clamp.

- The **FG current limit** protects the open drain when it is switched ON. The pull up resistance should be defined such that it never exceeds the minimum current limit level IFG_CLmin. Additionally the pull up current will add to the self-heating of the fandriver.

- The **FG clamp** will protect the FG pin in case of ESD and/or EOS events.
  Minimum pull up resistance value depends on the maximum pull up voltage in normal operation:

  - Vpu_fg =[VDDmin, $V_{FG\_CLAMPmin}$]V: FG clamp not active, when open drain is switched off.
    ⇨ Rpu_fg ≥ 2.2 kOhm

  - Vpu_fg =[$V_{FG\_CLAMPmin}$, 32]V: FG clamp active, when open drain is switched off.
    ⇨ Rpu_fg ≥ 4.7 kOhm

  - Vpu_fg =[32, V_{DD_40}]V: FG clamp active, when open drain is switched off.
    ⇨ Rpu_fg ≥ 10 kOhm

Note:

- For applications subject to short (<0.5us) pulses > V_{DD_40}, like Load-dump pulses up to 40V, Rpu_fg ≥ 4.7 kOhm
- In case Vpu_fg > $V_{FG\_CLAMPmin}$, a current will be drawn from Vpu_fg, even when FG is switched off. See Par. 11 Performance Graphs for clamping currents for 4.7kOhm and 10kOhm in case of Vpu_fg =24V and Vpu_fg =32V.
- In case Vpu_fg < $V_{FG\_CLAMPmin}$, only leakage current is drawn. Voltages smaller than $V_{FG\_CLAMPmin}$ may be applied directly on the FG pin. See Par. 11 Performance Graphs for leakage currents up to VFG =18V.

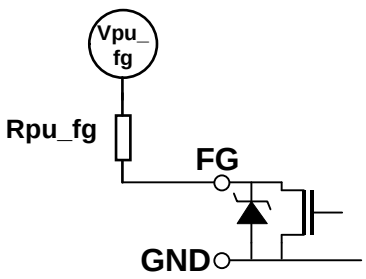


Figure 13

8.7.2. FG options

The FG output is configured in the E2PROM map using DFGCONFIG bits.

1. In the default FG configuration (FG) the FG output is reflecting the electrical commutations.

2. In a second FG configuration (FG DIV2) , the FG output is toggling every other commutation.

3. In a third FG configuration (FG *2), the FG output is toggling at double frequency of the actual commutation frequency.
   Note:
   - The maximum low time of the FG signal is limited to 42ms. Therefore at motor speeds lower than 176 rpm (2pp motor), the duty cycle of FG will not be 50% (see below Figure 14) .
   - The FG output will toggle at 4 times the mechanical speed for a 2 pole pair motor: a 2 pole pair motor spinning at 200rpm, will have an electrical commutation speed of 400rpm, and the FG output will toggle at a rate of 800rpm.

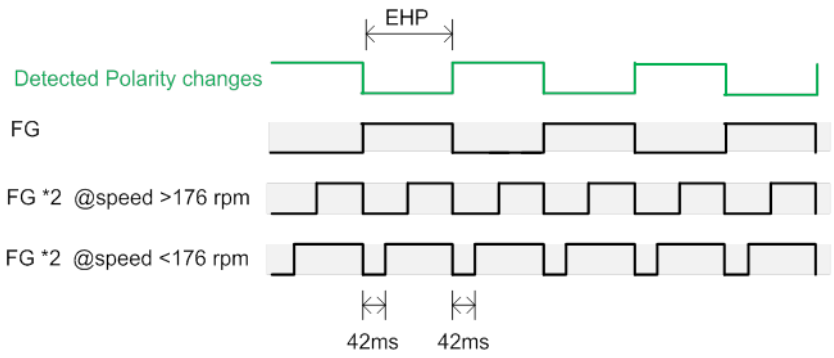


Figure 14 FG doubler output generation above and below 176rpm

8.7.3. RD level at POR

The DFGCONFIG bits allow configuring two different RD options as well.

The difference is only at start up. (see also the figures in 8.8 Start-up)

- In the default setting RD is LOW at power on (POR)
- An alternative setting is available with RD HIGH at POR.

8.7.4. Thermometric mode

The FG pin can also be configured as temperature sensor output. A current source scales as function of Tj. See application note.
This mode is interesting during application validation. It is not intended for application use in production.

8.8. Start-up examples

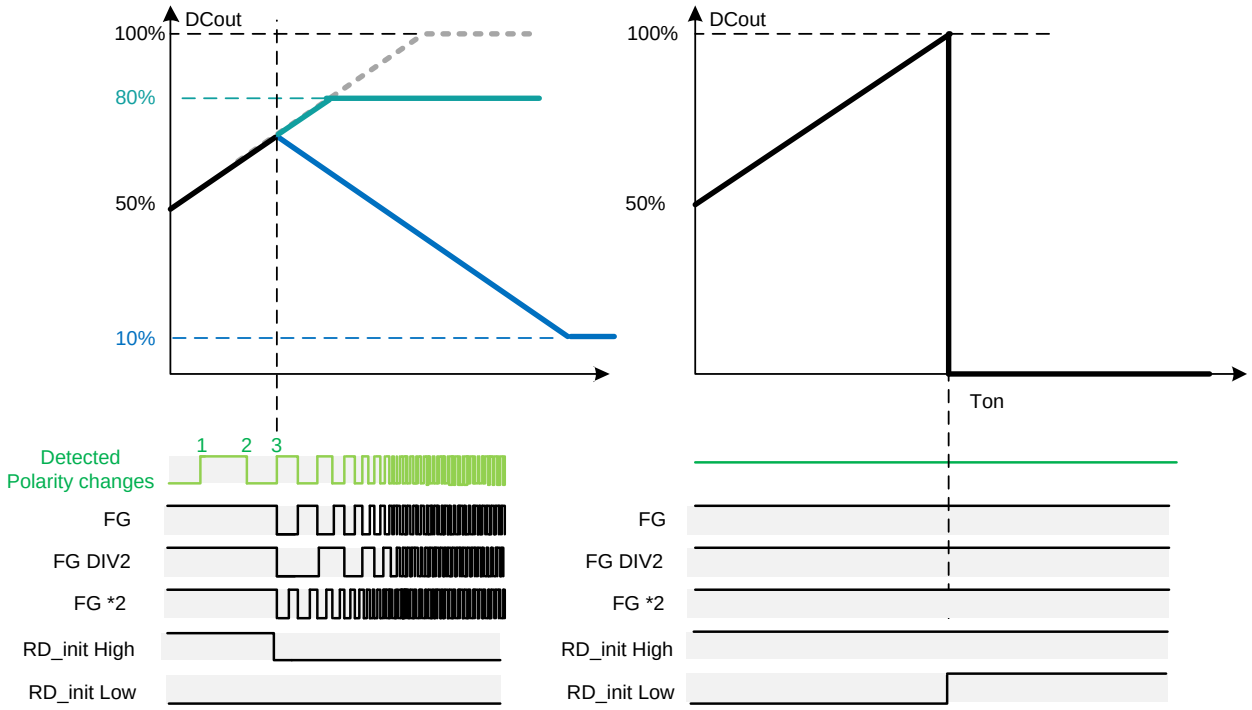


Figure 15 Soft start 50%, Ton=0.5s, DDCRATE=100%/s

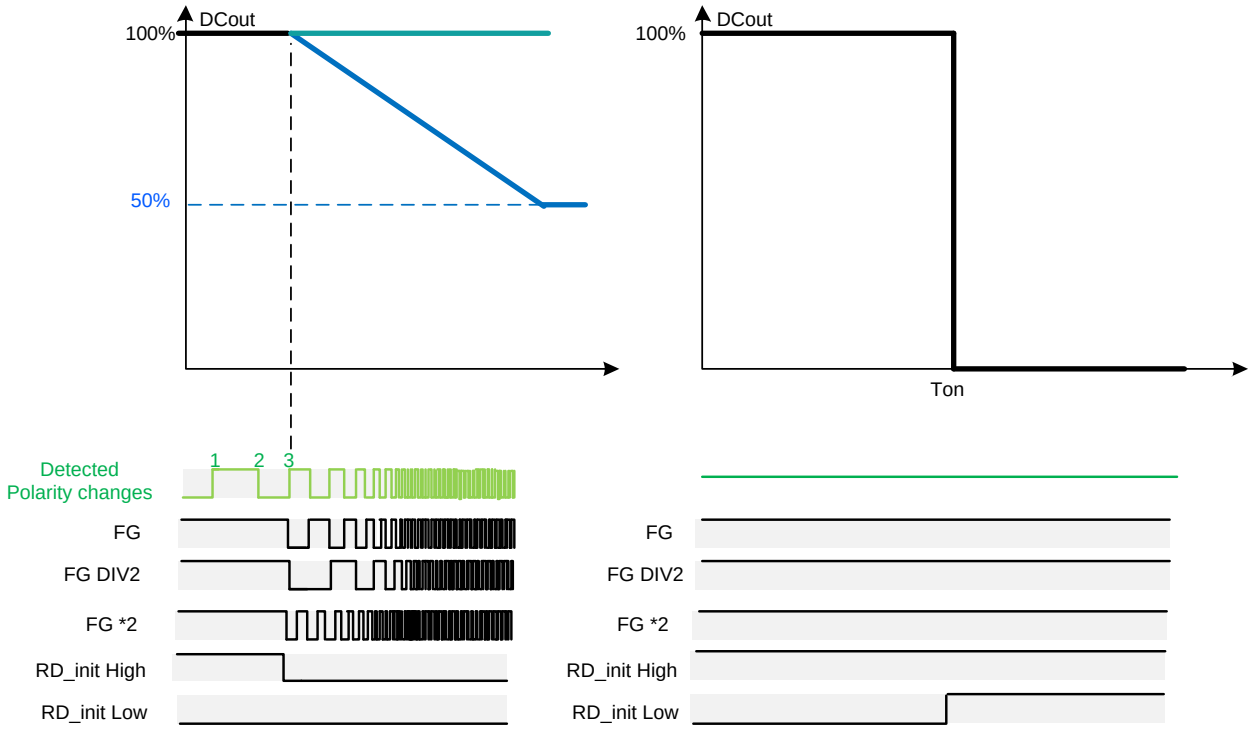


Figure 16 Quick start 100%, Ton=0.5s, DDCRATE=100%/s

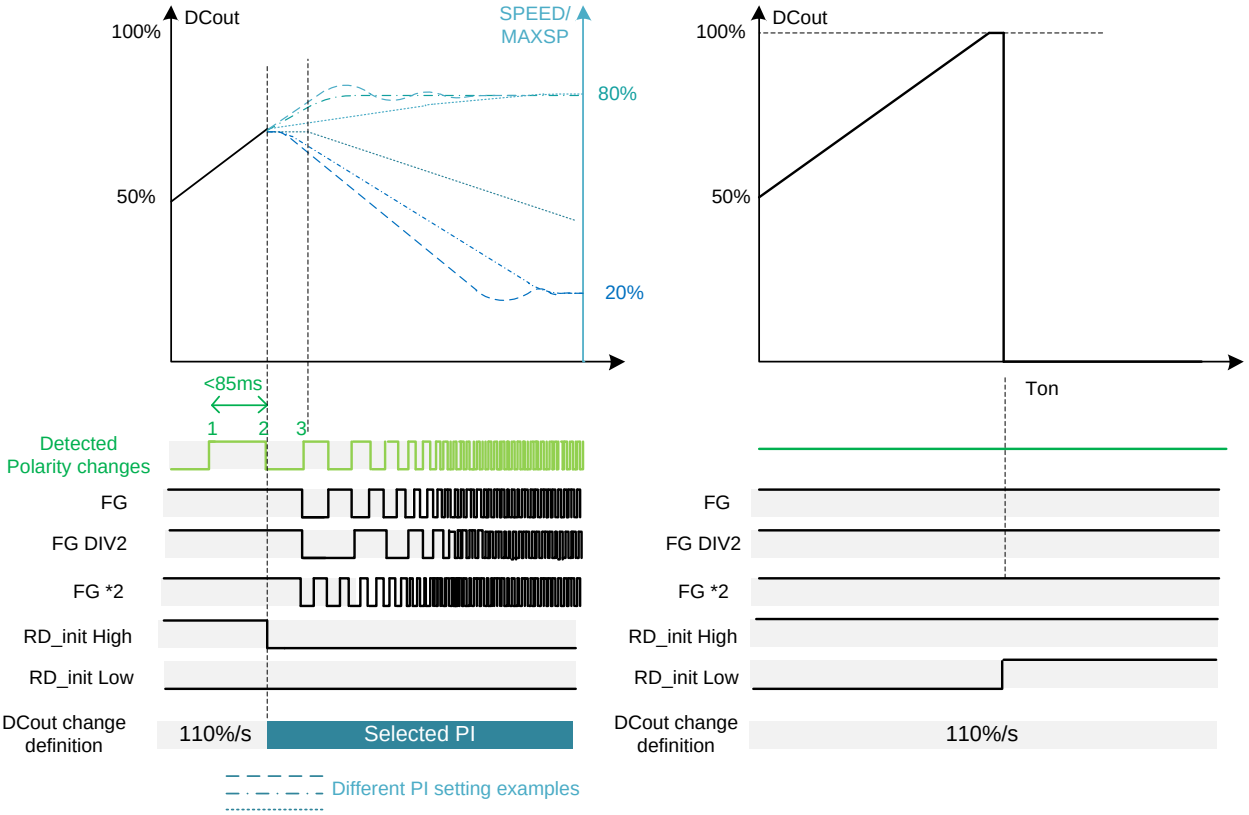


Figure 17 Soft Start 50%, with closed loop speed control, Ton=0.5s

In case of closed loop control, the selected softstart DCout is applicable. The Duty cycle change rate is fixed to 110%/s, independent of the selected DDCRATE. As soon as an EHP < 85ms is reached, the PI control takes over the DCout definition.

9. E2PROM map

ADDR	bit	Bit Name	Description	Consumer Default	Automotive Default
0x0000	**15:0**	ID1	Chip ID 1	n/a	n/a
0x0002	**15:0**	ID0	Chip ID 0	n/a	n/a
0x0004	**5:0**	DTlead	Lead time values for DSPEED = 0 (for DSPEED=1, values are half, see Table 14: Calculated electrical lead angle corresponding to a DTLEAD setting at a given mechanical speed.Table 14) 000000: 0sec 000001: 1*tpwm (~41.7us) 000010: 2*tpwm (~83.3us) 000011: 3*tpwm (~125us) … 111111: 63*tpwm (~2.62ms)	000000	000000
	7:6	X	Internal MLX	n/a	n/a
	9:8	DTslope	Soft Switching 0: Flat ; 1: 1/16; 2: 2/16; 3: Super-soft	1	0
	15:10	X	Internal MLX	n/a	n/a
0x0006	**1:0**	DLRPTRI1	After first Toff_diagn: Number of LRP trials with LRP t_{OFF} = LRP t_{ON}_start 00: 1 01: 2 10: 3 11: 4	00	01
	3:2	DLRPTRI2	Initial number of LRP trials with LRP t_{OFF} = LRP t_{ON}_start 00: 1 01: 2 10: 3 11: 4	00	01
	6:4	DLRPRAT	t_{OFF}_diagn / t_{ON}_start ratio selection 000: 8 001: 10 010: 12 011: 16 100: 24 101: 28 110: 32 111: 36	010	010

	8:7	DLRPTON	t_{ON}_start: Locked Rotor Protection ON time during start-up: 00: 0.33s 01: 0.43s 10: 0.51s 11: 1.02s Note : t_{ON}_run = 0.33s (fixed)	01	01
	15:9	X	Internal MLX	n/a	n/a
0x0008	**2:0**	DOVCMP	Overvoltage protection Voltage detector thresholds select 001: OVP 35V with filtering 101: OVP 22V with filtering 011: OVP 18V with filtering 111: VPROT_Disabled	001	101
	3:3	X	Internal MLX	n/a	n/a
	4:4	DIPROTRPT	IPROT endless repeat enable 0: Up to 3 consecutive IPROT activations 1: Unlimited number of IPROT activations	1	1
	5:5	DLRPDIS	Locked Rotor Disabled bit 0: Locked Rotor Protection enabled 1: Locked Rotor Protection disabled	0	0
	6:6	DSPEED	<table><tr><th></th><th>DSPEED=0</th><th>DSPEED=1</th></tr><tr><td>Minimum Speed for stable motor control **High**</td><td>**234 rpm**</td><td>469 rpm</td></tr><tr><td>Minimum Speed for stable motor control **Low**</td><td>**194 rpm**</td><td>388 rpm</td></tr><tr><td>Lead time resolut.</td><td>**41.7 us**</td><td>20.8 us</td></tr><tr><td>MAXSP_2pp</td><td>**[1417; 22,500] rpm**</td><td>[1895; 45,000] rpm</td></tr></table> Rpm: mechanical rpm assuming 2 pole pairs	0	0
	9:7	DFGCONFIG	Configure FG/RD output (see 8.7 FG (RD) output) 000: FG 001: FG FREQ DIV 2 111: FG FREQ MULTPL 2 100: RD initialized high 101: RD initialized low 011: Thermometric current mode	000	000

	10:10	X	Internal MLX	n/a	n/a
	12:11	X	Internal MLX	n/a	n/a
	13:13	DPWMINT	Input PWM integration period select bit 0: Tint = 21.3ms 1: Tint = 85.3ms	0	1
	14:14	DSTBYEN	Enable standby mode 0: DCin < 7.8%, maintains MINSP value 1: DCin < 7.8%, activates Standby mode	1	1
	15:15	X	Internal MLX	n/a	n/a
0x000A	**1:0**	X	Internal MLX	n/a	n/a
	2:2	DEHPLIM	**For DEHPCOEF ≠ 000 (closed loop speed ctrl):** Minimum SPEED for closed loop control 0: 20% 1: 12.5%	n/a	n/a
	2:2	DDCRATE	**For DEHPCOEF = 000 (open loop):** Duty cycle change rate select 0: duty ratio change rate DCRATE = 50%/s 1: duty ratio change rate DCRATE = 100%/s	0	1
	8:3 (*)	DEHPTAR	**For DEHPCOEF ≠ 000 (closed loop speed ctrl):** EHP Regulation target EHP value See Table 10 Closed loop speed control: MAXSP calculation examples for 2 pole pairs motor above	n/a	n/a
	8:3 (*)	DMAXDCY	**For DEHPCOEF = 000 (open loop):** Maximum Target duty cycle set by EEPROM DCout_max[7:0] = [3 * DMAXDCY[5:0] + 66] /256 6'b00: Calculated Minimum DCout = 25.9% 6'h3F: Calculated Maximum DCout = 99.21% *Note: all DCout_calc > 97.8% are rounded to 100%*	111111	111111
	10:9	DEHPSTEP	EHP Regulator target EHP step size 00: Step size is ~10.4 us 01: Step size is ~20.8 us 10: Step size is ~41.7 us 11: Step size is ~83.3 us See Table 10 Closed loop speed control: MAXSP calculation examples for 2 pole pairs motor above	n/a	n/a
	12:11 (*)	DEHPINIT	**For DEHPCOEF ≠ 000 (closed loop speed ctrl):** Start-up DCout in case of closed loop control 00: 12.5% 01: 25% 10: 50% 11: 100% (quick start)	n/a	n/a

	12:11 (*)	DDCINIT	**For DEHPCOEF = 000 (open loop):** Initial DCout at start up, as percentage of DMAXDCY 00: 12.5% of DMAXDCY 01 25% of DMAXDCY **10: 50% of DMAXDCY** **11: 100% of DMAXDCY**	10	11
	15:13	DEHPCOEF	Closed loop speed regulation 000: EHP regulation is disabled (open loop) 001: division of error is by 4 010: division of error is by 8 011: division of error is by 16 100: division of error is by 32 101: division of error is by 64 110: division of error is by 128 111: division of error is by 256	000	000

Table 15

(*) Note: in word 5, the meaning of bits [8:3], and bits [12:11] depend on the value of DEHPCOEF

10. Detailed General Description

10.1. Block diagram

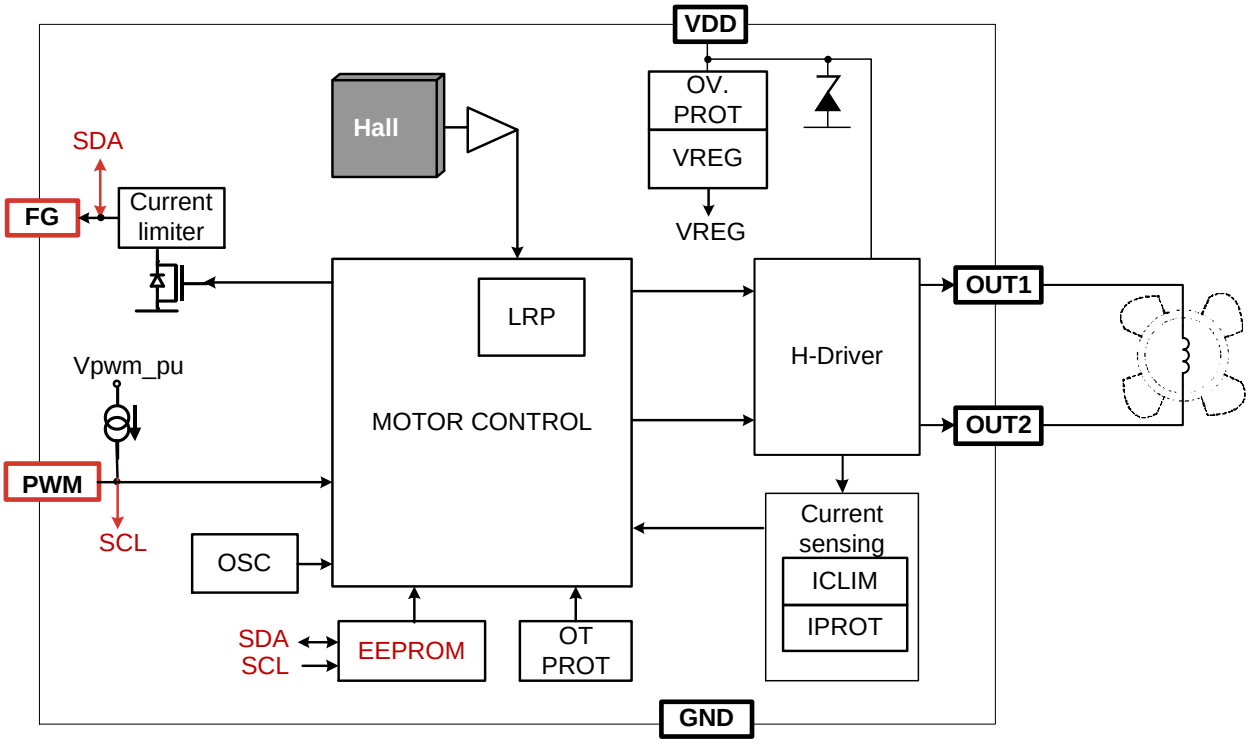


Figure 18

10.2. ESD protection functional Schematic

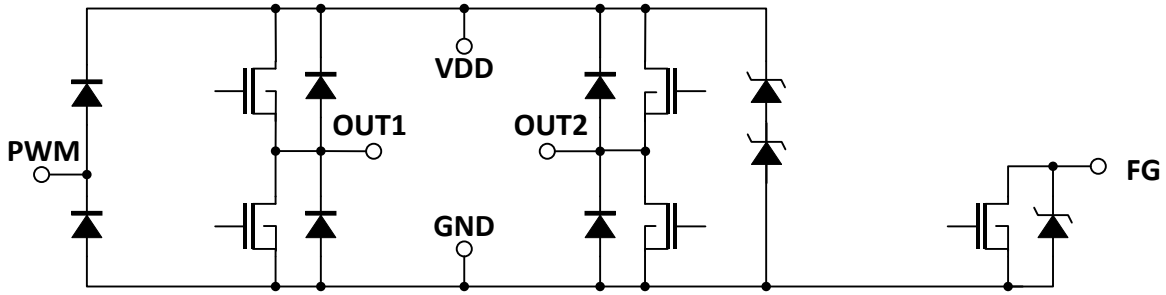


Figure 19 Functionally equivalent ESD circuit schematic

10.3. I2C interface

See application note.

I2C Slave address 88d/58h

10.4. Application schematic

- A decoupling capacitor of minimum 100nF should be placed as close as possible to the MLX90411 VDD and GND pins.
  Larger capacitor size may be required as function of the motor current to increase the stability and protect against external noise and power surge.

- The MLX90411 integrates a supply clamping function. In case the energy push back may exceed the Safe-Operating-Area of the integrated clamp, an external clamping Zener/TVS (*) may be required as described in the next paragraph.

- A series diode should be applied for reversed polarity protection.

- A pull up resistor Rpu_fg is necessary to connect FG pin to VDD, see par 8.7.1 FG Protections

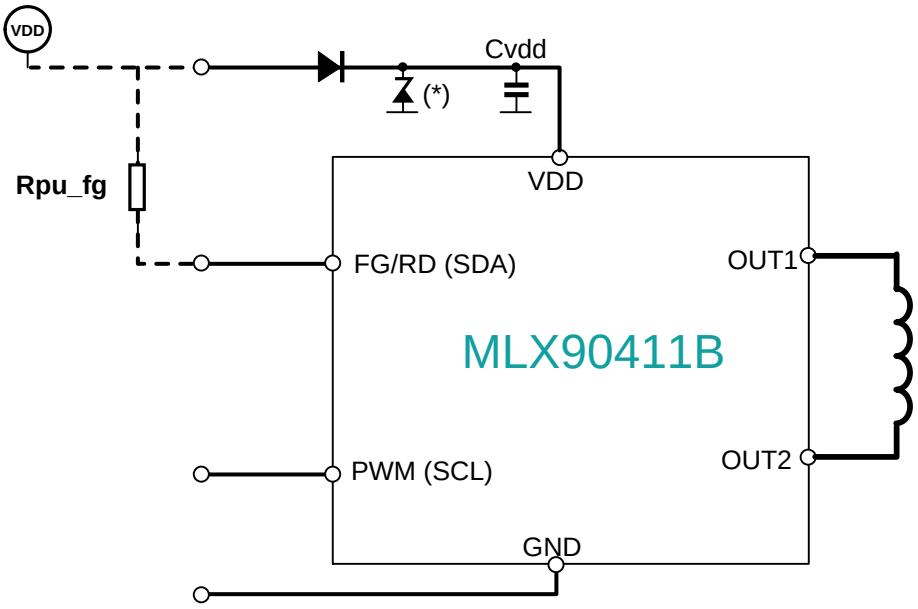


Figure 20

10.5. Integrated Supply-Clamp SOA

The MLX90411 integrates a clamping circuit on the supply pin (VDD). The Supply Clamping voltage is the voltage at which the internal supply clamping structure will trigger in case energy is pushed back from the motor onto the decoupling capacitance, and can not be pushed back into the supply, for instance because of the presence of a reverse polarity diode, or because of a hot unplug condition.

The Supply Clamping Voltage level ensures by-design that such energy push-back does not exceed the technology breakdown level of the driver. The clamping circuit is capable to absorb a limited amount of energy as shown in Figure 21. This is referred to as the Safe Operation Area (SOA) of the integrated supply clamp. The SOA is a function of the height of the current peak, and the duration of the clamping time, as well as from the clamping voltage, and the junction temperature at the time when the clamping is triggered. In case clamping only occurs due to hot unplug condition, in practice the maximum clamping current will be limited in line with the applied current limit.

For instance:

- For the 40V clamp, at Tj=150C, a current of 1.0A can be clamped during maximum 230us.
- While for the 20V clamp at Tj = 100C, 1.0A can be clamped safely up to 1.9ms.

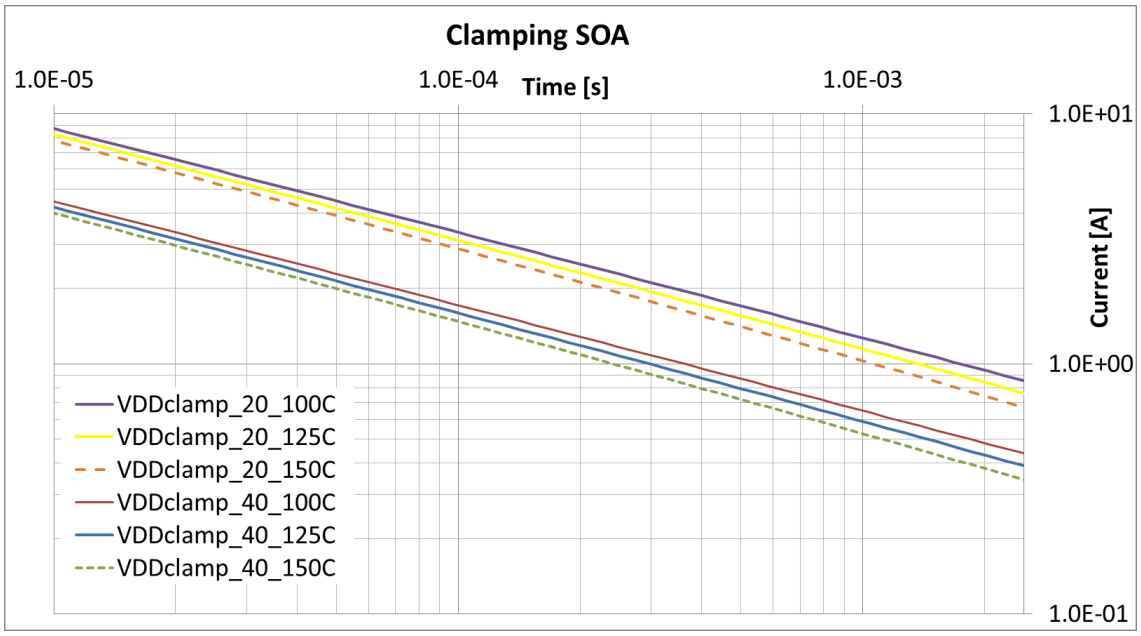


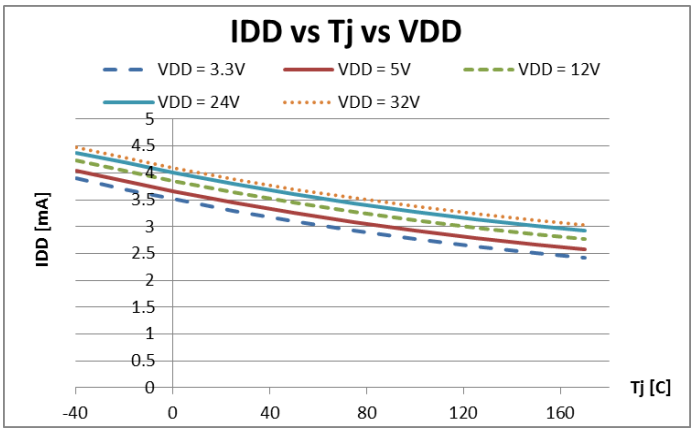
Figure 21, SOA Supply clamp, single pulse

Notes:

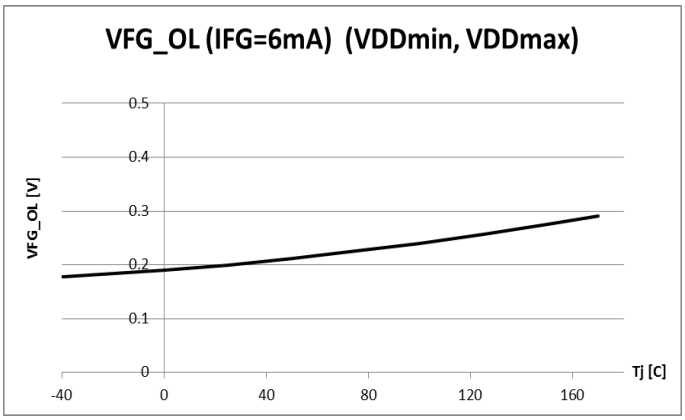
- The clamp SOA is validated on bench as well as by simulation, and is applicable over the full operating voltage, operating temperature, and over worst case corner process variation.
- Applications which are subject to flyback energy pulses beyond the SOA, should apply external protection circuitry, such as TVS.
- See the application notes for a detailed discussion on the SOA of the supply clamp. In this application note also quick reference tables are available which allow to evaluate the SOA based on basic motor parameters such as Lcoil and Rcoil.

11. Performance Graphs

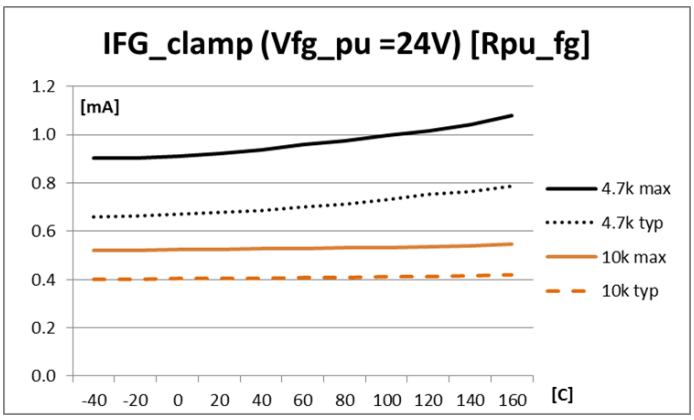
11.1. IDD



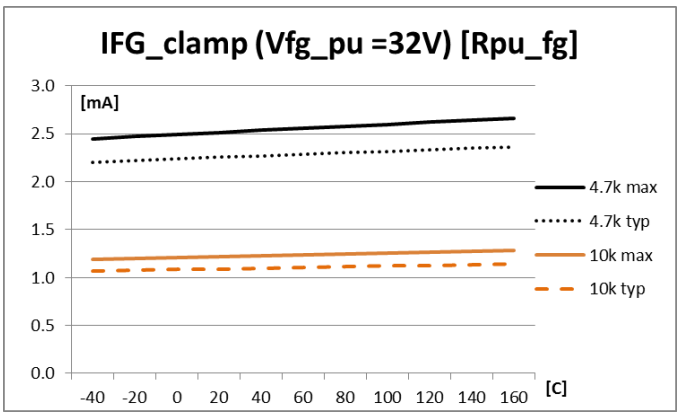
11.2. VFG_OL



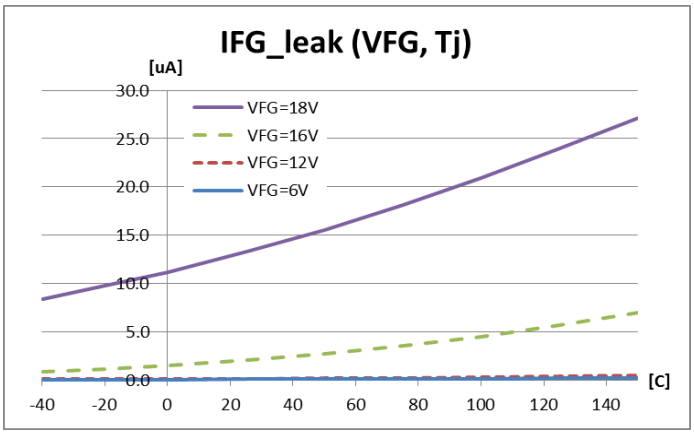
11.3. IFG_Clamp, Vpu_fg = 24V



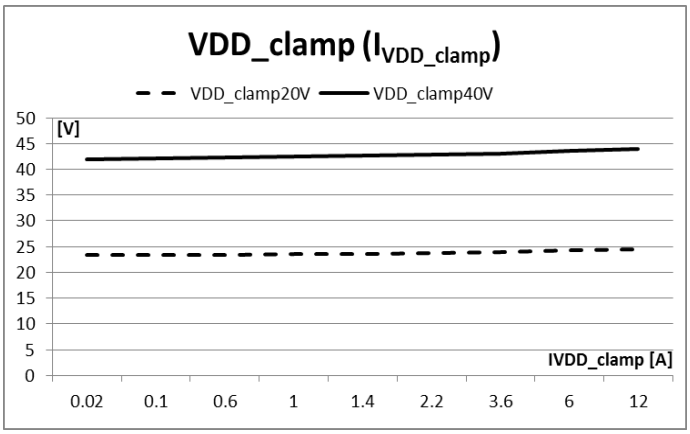
11.4. IFG_Clamp, Vpu_fg = 32V



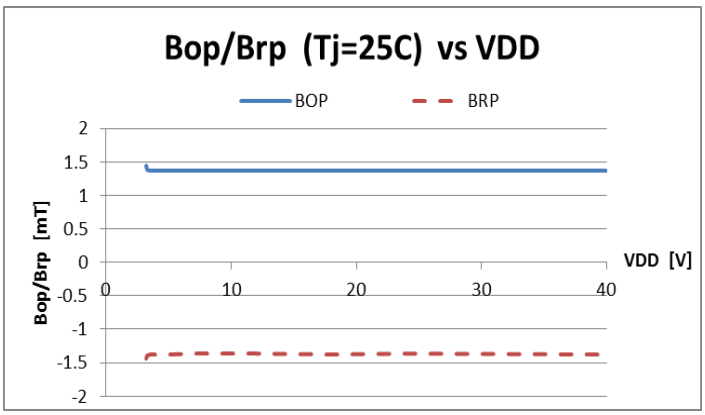
11.5. IFG_leak , Vpu_fg < 18V



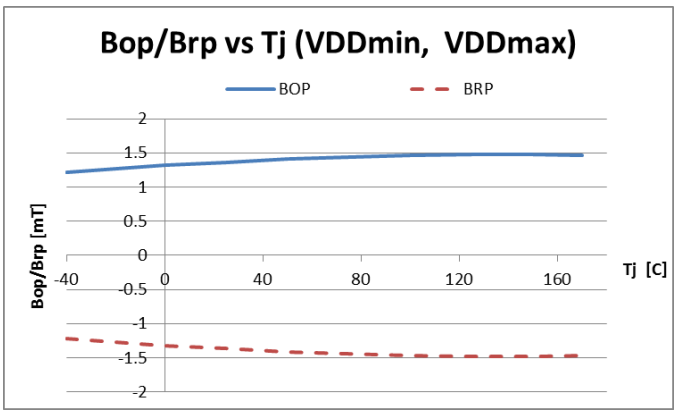
11.6. VDD_clamp



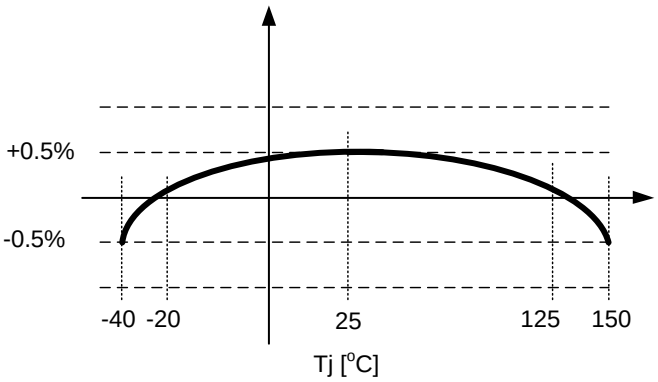
11.7. Bop/Brp (VDD)



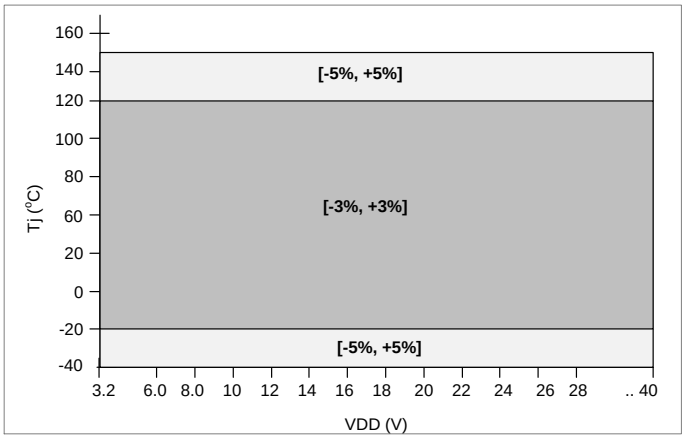
11.8. Bop/Brp (Tj)



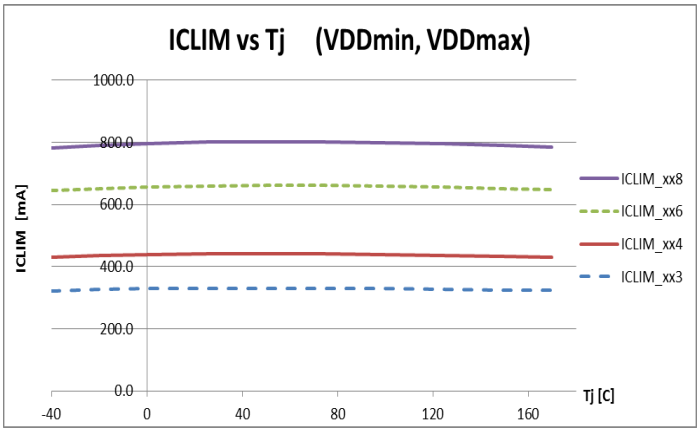
11.9. Typical RC oscillator variation (Tj)



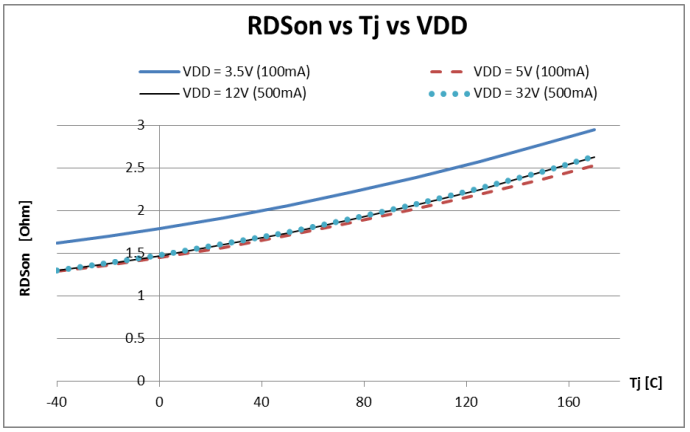
11.10. RC oscillator (VDD, Tj)



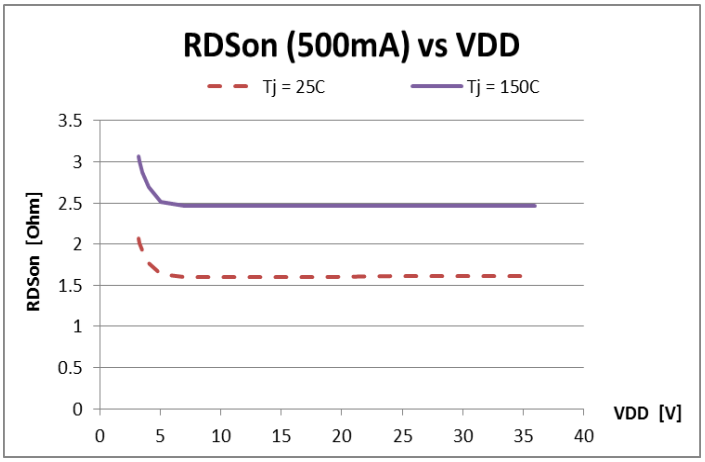
11.11. ICLIM



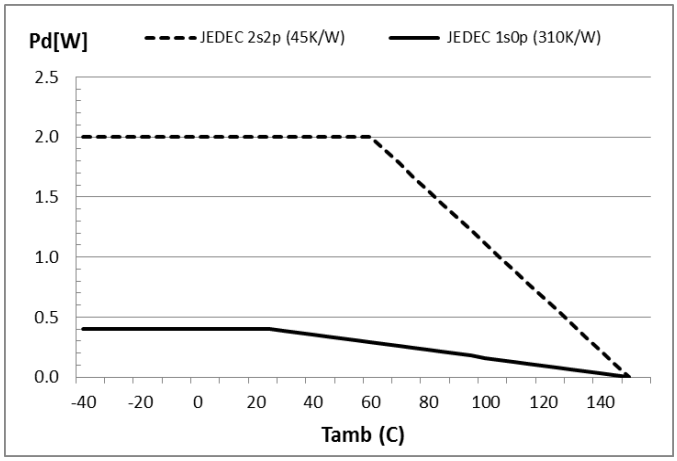
11.12. RDSon (Tj)



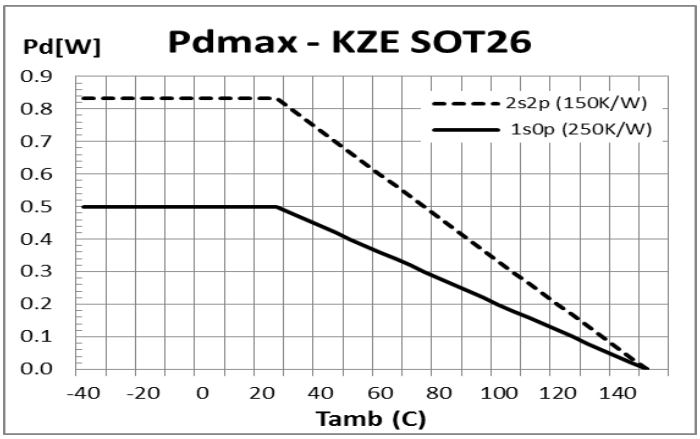
11.13. RDson(VDD)



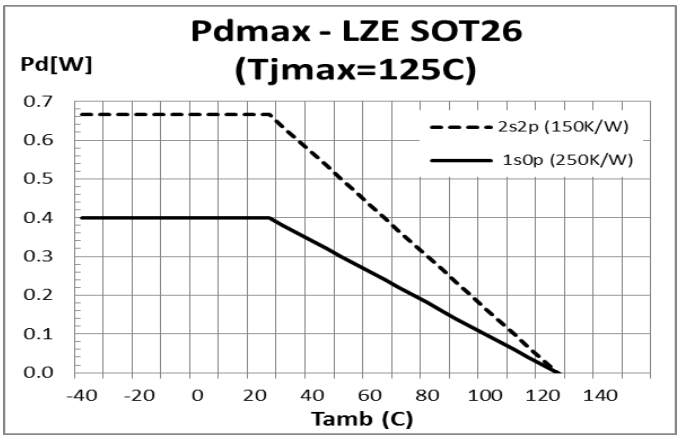
11.14. Pdmax –LD



11.15. Pdmax KZE



11.16. Pdmax LZE



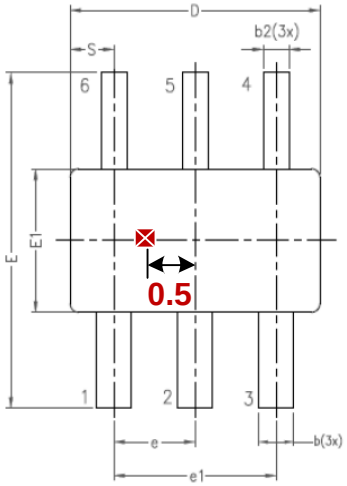
Notes on Power derating:

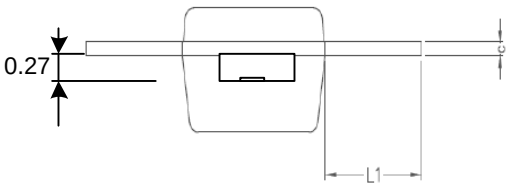
- Power derating curves serve as reference for the maximum amount of dissipation allowed at a given ambient temperature, for given thermal resistance Rthja. It is calculated based on the maximum allowed Tj for a given Thermal resistance: Pd(Tamb) = (Tjmax – Tamb) / Rthja
- Mind that in reality the Rthja for a given package depends on IC size, power dissipation, package temperature, convection. This means it should be evaluated taking into account pcb layout, nr of pcb layers, wind flow, self-heating of the motor, etc.
- Mind also that JEDEC standard recommends to limit the heating in packages, depending on Rthja:
  - < 1Watt for Rthja up to 60K/W
  - < 0.75W for Rthja up to 100K/W
  - < 0.5W for Rthja > 100K/W

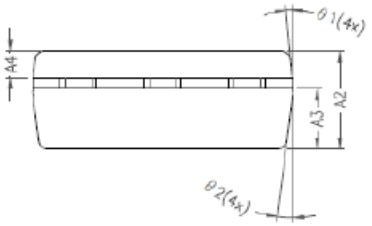
12. Package Information

12.1. ZE Package (SOT23-6L with straight leads)

	A2	A3	A4	b	b2	c	D	E	E1	e	e1	L1	s	Θ1	Θ2
min	1.00	0.62	0.25	0.40	0.30	0.08	2.80	3.60	1.50	0.95	1.90	1.00	0.46	5°	15°
max	1.20	0.72	0.35	0.50	0.40	0.22	3.00	4.00	1.70	BSC	BSC	1.20	0.56		

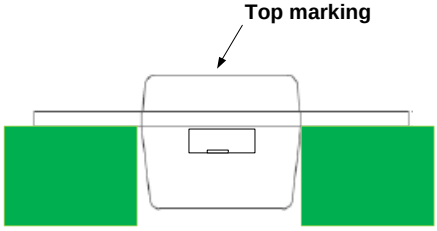


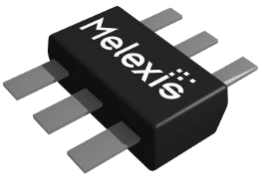




NOTE :

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER END. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE.
3. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
4. DIMENSION "b & b2" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 mm TOTAL IN EXCESS OF THE "b & b2" DIMENSION AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm.
5. LEAD FRAME MATERIAL : EFTEC-64T
6. LEAD 1,2,3 MAY BE WIDER THAN LEADS 4,5,6 FOR PACKAGE ORIENTATION.





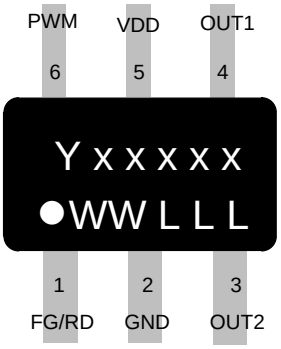
Marking: on package top side, die: face **down**

12.1.1. Marking ZE package options

Top side Marking:

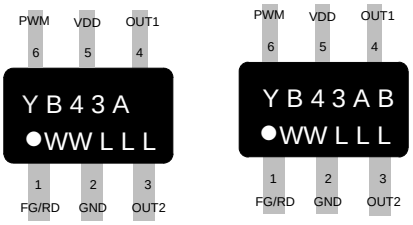
Line 1 : Yxxxxx

- Y : Date code last digit of year
- xxxxx: optional for distinction between E2 programming options
  - x1: "B" or "Z" or "P" other Letter referring to MLX90411B, to distinguish from "1" which refers to 90411A
  - x2: voltage rating
    - 2: automotive: LZE 20V
    - 3: consumer: KZE 20V
    - 4: automotive LZE 40V
    - 5: consumer KZE 40V
  - x3: current limit code
  - x4: third letter of option code
  - x5:
    - Default blank (unmarked)
    - If marked, it indicates part has been programmed a second time (reprogrammed). Meaning of this new marking will be defined as part of RMA procedure.



Example marking, for Order code LZEBAA043:

Left normal, Right reprogrammed

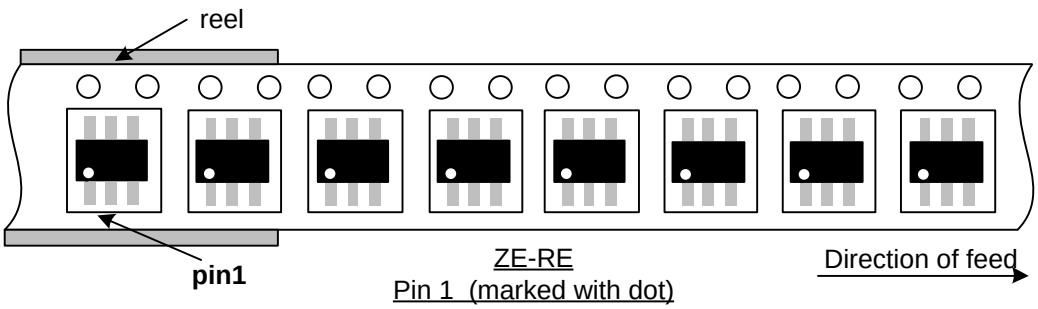


Line 2 : "dot" WWLLL

- "dot" : Indication of pin 1
- WW : Calendar week date code
- LLL: Lot number (Letter + 2 last digits)

Note: Package marking is subject to change in case multiple options will be released in production in the same package, in order to allow distinction between the different options. Such change will be subject to PCN for –L grade variants.

12.1.2. SOT (ZE) Tape & Reel information



12.2. UTDFN6 2.5*2*0.4mm

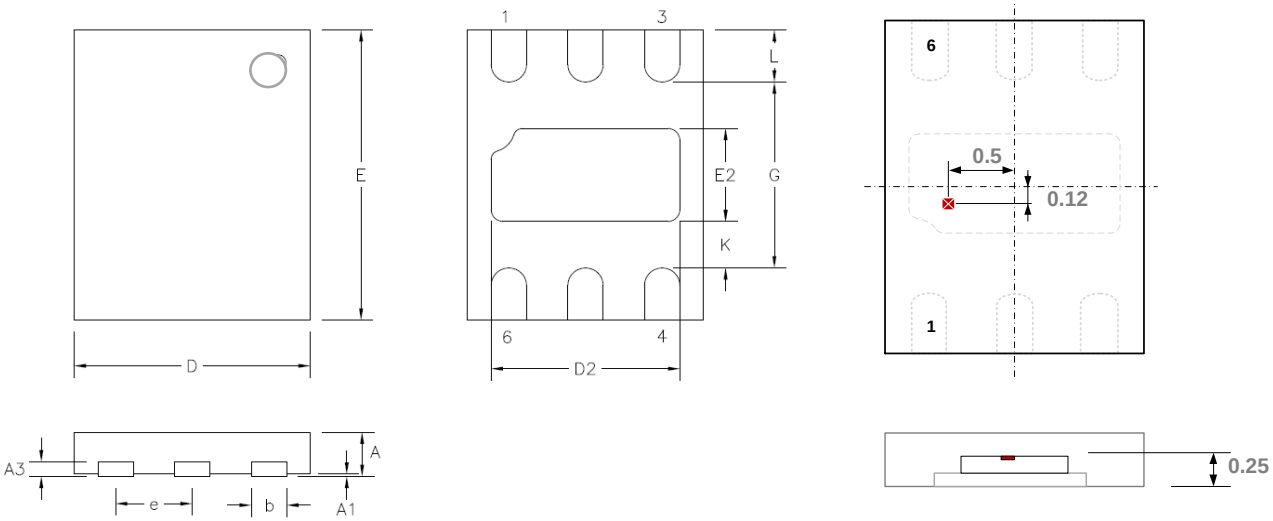


Figure 22 UTDFN6 Package dimensions

***Figure 23* Hall plate location:**
Top view and Cross-sectional view

D x E	N	e		A	A1	A3	D2	E2	G	L	K	b
2 x 2.5	6	0.65	min	0.31	0	0.12 REF	1.45	0.75	1.55	0.35	0.35	0.25
			max	0.4	0.05		1.7	0.85	1.65	0.55	–	0.35

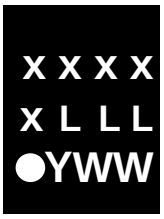
1. All dimensions are in millimeters.
2. If the terminal has a radius on the other end of it, dimension b should not be measured in that radius.
3. Coplanarity applies to the terminals and all other bottom surface metallization.
4. Dimension shown is excluding burr (0.05mm).
5. Laser marked dot is Pin 1 marker

12.2.1. Marking UTDFN6 package

Top side :

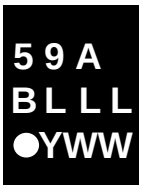
Line 1 : xxxx: optional for distinction between E2 programming options

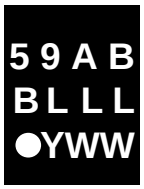
- X1: voltage rating
  - 2: automotive: LLD 20V
  - 3: consumer: KLD 20V
  - 4: automotive: LLD 40V
  - 5: consumer KLD 40V
- X2: current limit code
- X3: third letter of option code
- X4:
  - Default blank (unmarked)
  - If marked, it indicates the part has been programmed a second time (reprogrammed). Meaning of this new marking will be defined as part of RMA procedure.



Example marking: for Order code KLDBAA049, 40V, 960mA:

Left normal - Right reprogrammed





Line 2: x LLL

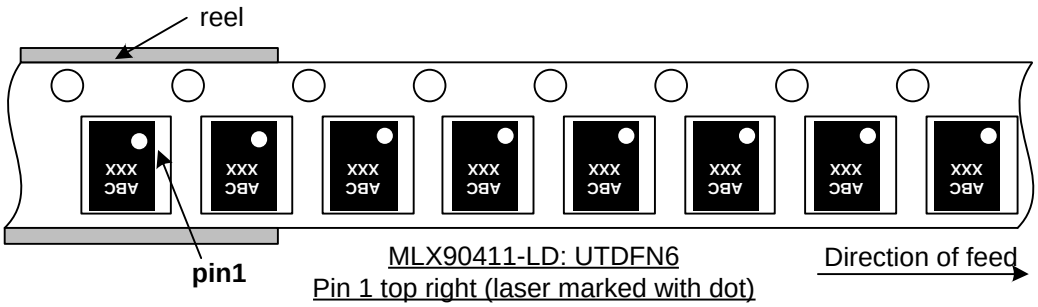
- x: "B" or "Z" or other Letter referring to MLX90411B, to distinguish from "1" which refers to 90411A.
- LLL: Lot number (Letter + 2 last digits)

Line 3: "dot"YWW :

- "dot" : Indication of pin 1
- Y : Date code last digit of year
- WW : Calendar week date code

Note: Package marking is subject to change in case multiple options will be released in production in the same package, in order to allow distinction between the different options. Such change will be subject to PCN for –L grade variants.

12.2.2. UTDFN6 Tape & Reel information



13. Annex

13.1. Revision history table

5 AUG 2020	• First release, aligned with PPAP release

7 DEC 2020	• Marking UTDFN6 package: Document layout update
	• DSTBYEN bit documented
	  ○ In Par. 8.2.2 DCin, DCout calculation, Standby mode,
	  ○ In Par. 8.4.5 Forced restart after protection
	  ○ In Par. 9 E2PROM map
	• Added in par 4 Ordering Information "9 - -: for ordering reprogrammed parts"

20 Jan 2021	• Corrected typo in
	  ○ In Par. 8.2.2 DCin, DCout calculation, Standby mode,
	  ○ In Par. 9 E2PROM map

Table 16

13.2. Disclaimer

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