

RH4Z2501-KIT - HW revision 3

Hardware application note

Introduction

This document explains the hardware design of the RH4Z2501-KIT, its main features and the necessary hardware setup to implement an IO-link device.

Target Device

RH4Z2501: IO-Link transceiver with integrated protection

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1. Overview

1.1 RH4Z2501 Features

The RH4Z2501-KIT is an Evaluation Board for the RH4Z2501 Renesas silicon solution that implements an IO-Link device. The board also integrates an Advanced ARM based Sensor Signal Conditioner: ZSSC3281.

The main purpose of the RH4Z2501-KIT is to enable the communication between the user and the RH4Z2501 device with the GUI (Graphical User Interface). The RH4Z2501_Evaluation_SW establishes the communication via a USB port (configured as a virtual COM port) to the SSC Communication Board (CB). The microcontroller on the SSC CB interprets these commands, converts them according to the digital interface (I2C, SPI or OWI), and build the frame for to the RH4Z2501 and ZSSC3281 mounted on RH4Z2501 EVB.

The RH4Z2501 offers the following features:

- Voltage range from 9V to 36V
- Over voltage peak robustness of +/-60V
- Configurable driver output current 50mADC to 600mA DC
- Rdson of less than 2.50hm
- Adjustable driver slew rate
- Integrated Wake-Up detection
- MCU assisted Wake-up generation (typ. 600mA)
- · OWI digital communication and calibration interface
- Integrated Linear Voltage Regulators 3.3V and 5V
- Ambient Temperature range -40°C ... 125°C
- Glitch filter for receiver
- Integrated Protection
 - +/-1.25kV/2.5A(peak) surge protection for VDD, CQ, GND (8/20 μs pulse acc. IEC xyz)
- Reverse polarity protection for VDD, CQ, GND
- · On-chip diagnostics:
 - o Over temperature detection
 - Supply voltage monitor
 - Broken chip detection

For more information, please refer to the RH4Z2501 Datasheet.

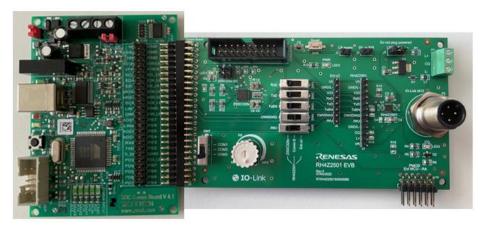
1.2 Kit Contents

RH4Z2501 Evaluation Board - RH4Z2501-KIT SSC Communication Board - SSCCOMMBOARDV4P1C USB Cable



1.3 RH4Z2501-KIT Capabilities

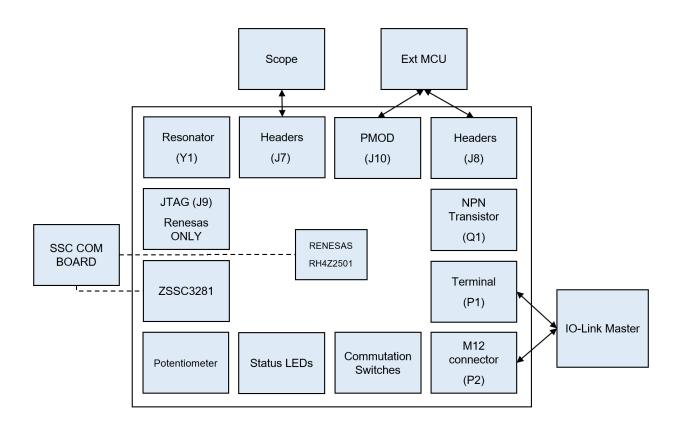
The RH4Z2501-KIT integrates all the necessary components to quickly evaluate the IO-Link Fieldbus technology.



Do **NOT** close J2 when using the SSC Communication Board at the same time as powering the board via the IO-Link line!

2. Getting Started

2.1 System Block Diagram



2.2 Default Board Configuration

Jumper/Switch	Default position
J1	LDO (J1_2-3)
J5	open
J2	open
J4	open
J6	open
SW1	ZSSC328x position
SW2	ZSSC328x position
SW3	ZSSC328x position
SW4	Com B position
SW5	ZSSC328x position
SW7	COM3

3. RH4Z2501-KIT Components

3.1 Power Requirements

3.1.1 Power Supply Options

3.1.1.1 Option 1: P2 Connector

P2 is a male 4-pin M12-A-coded connector. It enables an easy connection between the RH4Z2501-KIT and an IO-Link Master.

If powering RH4Z2501-KIT from the IO-Link Master:

- Set J1 to position LDO if you want to use the internal LDO to regulate the voltage
- Set J1 to position NPN if you want to use the internal external NPN transistor to regulate the voltage

3.1.1.2 Option 2: P1 Connector

The P2 connector signals are also accessible from P1.

3.1.1.3 Option 3: J3 Comm Board Connector

The SSCCOMMBOARDV4P1C can power the RH4Z2501-KIT via J3_3 (KS5V).

- Close J2 to enable the 5V signal to supply the transceiver

Be aware that some OWI commands need to be executed in order to enable the supply. The PSU can also be enabled via the GUI.

3.1.1.4 Option 4: J7 RH4Z2501

J7 can directly supply the 5V to the RH4Z2501 via J7_1.

3.1.1.5 Option 5: J8 Ext uC Connector

J8 can directly supply the 5V to the RH4Z2501 via J8_1.



3.1.2 Voltage regulation Options

The RH4Z2501-KIT enables 2 methods to regulate the voltage supplied from the IO-Link Master:

3.1.2.1 Option 1: Integrated transceiver LDOs

Set J1 to position "LDO" if you want to use the internal PHY LDO to regulate the voltage.

3.1.2.2 Option 2: External NPN Transistor

Set J1 to position "NPN" if you wish to improve the thermal performance of the device and allow a higher current supply.

3.1.3 IO Voltage operation

Close J5 if you wish to operate the IOs under a 5V logic level. The PHY digital IOs will operate at 3V3 if left open.

3.2 Signal Sensor Conditioner: ZSSC3281

3.2.1 Enable I2C communication

Close J4 and J6 to enable the SSC Comm Board to establish an I2C communication with the ZSSC3281. This interface is used to configure the device via a GUI.

3.2.2 JTAG/SWD Connector

Use J9 to connect a J-Link probe to update the firmware running on the ZSSC3281. (Only Renesas internally)

3.2.3 AFE circuit

The bridge circuit attached to the SSC'AFE is composed of a potentiometer R9 and 4 resistors. This simple configuration is implemented to provide an easy way to act on the input signal of the SSC.

3.2.4 Oscillator

The ZSSC3281 is equipped with an on-chip oscillator. As an alternative, it is also possible to use Y1 as external resonator to achieve a better clock precision. This selection is implemented in its firmware and Y1 is used by default.

3.2.5 COM selection

SW7 enables the IO-Link baudrate selection at startup. Make sure to press the reset switch SW6 after each COM update.



3.3 Commutation Switches

The 5 onboard 3 position switches are used to select the target (ZSSC3281, SSCCOMMBOARDV4P1C or ext MCU) the RH4Z2501 will communicate with.

3.3.1 SW1 - RxD Signal selection

This switch enables the path between RH4Z2501 pin RxD:

- GPIO3 of ZSSC3281
- PE4 of SSCCOMMBOARDV4P1C
- Pin 4 of J8 (PMOD)

3.3.2 SW2 - TxD Signal selection

This switch enables the path between RH4Z2501 pin TxD:

- GPIO2 of ZSSC3281
- PE5 of SSCCOMMBOARDV4P1C
- Pin 5 of J8 (PMOD)

3.3.3 SW3 – TxEN Signal selection

This switch enables the path between RH4Z2501 pin TxEN:

- GPIO11 of ZSSC3281
- PE6 of SSCCOMMBOARDV4P1C
- Pin 6 of J8 (PMOD)

3.3.4 SW4 – OWI/D Signal selection

This switch enables the path between RH4Z2501 pin OWI/D:

- GPIO7 of ZSSC3281
- OWI of SSCCOMMBOARDV4P1C
- Pin 7 of J8 (PMOD)

3.3.5 SW1 – /WU Signal selection

This switch enables the path between RH4Z2501 pin /WU:

- GPIO10 of ZSSC3281
- PE7 of SSCCOMMBOARDV4P1C
- Pin 8 of J8 (PMOD)

3.4 LEDs

3.4.1 Power status

LED3 is powered from the 3V3 power rail regulated by the RH4Z2501. It therefore signals if the IO-Link transceiver is powered.

3.4.2 SSC status

LED1 connected to GPIO1 of ZSSC3281 signals if the SSC is operating.

3.4.3 IO-link communication status

LED2 is used to easily visualize the status of the C/Q line. Its signal is simply regulated by NPN transistor Q2 and its voltage divider.

Revision History

		Descript	Description	
Rev.	Date	Page	Summary	
0.1	01/12/2021		Preliminary	
0.2	02/06/2022		Modification for HW v2	
1.0	09/08/2022		Minor modifications	
1.1	19/12/2022		Modification for HW v3	

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1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

- 6. Voltage application waveform at input pin
 - Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
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