20230829005.2 **PCN Number:** PCN Date: August 30, 2023 Qualification of new Fab site (RFAB) using qualified Process Technology and Die Title: change for select devices **Customer Contact:** Change Management team Dept: Quality Services **Estimated Sample Proposed 1st Ship Date:** Feb 29, 2024 Sep 29, 2023* **Availability:** *Sample requests received after September 29, 2023 will not be supported. **Change Type:** Assembly Site Design Wafer Bump Material M Assembly Process Data Sheet Wafer Bump Process M Assembly Materials Part number change Wafer Fab Site **Mechanical Specification** Test Site M Wafer Fab Materials Packing/Shipping/Labeling Test Process \boxtimes Wafer Fab Process

PCN Details

Description of Change:

Texas Instruments is pleased to announce the qualification of a new fab & process technology (RFAB, LBC9) for selected devices listed in the "Product Affected" section of this document.

С	urrent Fab Site	e	Additional Fab Site				
Current Fab Site	Process	Wafer Diameter	Additional Fab Site	Process	Wafer Diameter		
DP1DM5	LBC8	200mm	RFAB	LBC9	300mm		

The die was also changed as a result of the process change.

Qual details are provided in the Qual Data Section.

Reason for Change:

Continuity of supply

Anticipated impact on Form, Fit, Function, Quality or Reliability (positive / negative):

None

Changes to product identification resulting from this PCN:

Fab Site Information:

Chip Site	Chip Site Origin Code (20L)	Chip Site Country Code (21L)	Chip Site City
DP1DM5	DM5	USA	Dallas
RFAB	RFB	USA	Richardson

Die Rev:

Current Die Rev [2P] Die Rev [2P] Α В

Sample product shipping label (not actual product label)



(1P)SN74LS07NSR (a) 2000 (D) 0336 31T)LOT: 3959047MLA 4W) TKY(1T) 7523483SI2 (2P) REV: (V) 9033317 (Z1L) CCO:USA (Z3L) ACO:MYS (20L) CSO: SHE (22L) ASO: MLA

Product Affected:									
	DRV5013ADELPGMQ1	DRV5013ADQLPGQ1	DRV5013AGQLPGMQ1	DRV5013BCELPGQ1					
	DRV5013ADELPGQ1	DRV5013AGELPGMQ1	DRV5013AGQLPGQ1	DRV5013BCQLPGMQ1					
	DRV5013ADQLPGMQ1	DRV5013AGELPGQ1	DRV5013BCELPGMQ1	DRV5013BCQLPGQ1					

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Туре	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: DRV5013AGELPGMQ1	Qual Device: DRV5013ADELPGMQ1	Qual Device: DRV5013BCELPGMQ1	QBS Reference: TMP6131ELPGMQ1	QBS Reference: DRV5015A2EDBZRQ1	QBS Reference: DRV5015A3EDBZRQ1
Test Group /	Test Group A - Accelerated Environment Stress Tests												
PC	A1	JEDEC J- STD-020 JESD22- A113	3	77	Preconditioning	MSL1 260C	-	-	-	-	-	1/0/0	2/0/0
HAST	A2	JEDEC JESD22- A110	3	77	Biased HAST	130C/85%RH	96 Hours	-	1/77/0	-	3/231/0	1/77/0	2/156/0
AC/UHAST	А3	JEDEC JESD22- A102/JEDEC JESD22- A118	3	77	Autoclave	121C/15psig	96 Hours	-	-	-	-	1/77/0	2/154/0
AC/UHAST	А3	JEDEC JESD22- A102/JEDEC JESD22- A118	3	77	Unbiased HAST	130C/85%RH	96 Hours	-	1/77/0	-	3/231/0	-	-
тс	A4	JEDEC JESD22- A104 and Appendix 3	3	77	Temperature Cycle	-55C/150C	2000 Cycles	-	1/77/0	-	-	-	-
тс	A4	JEDEC JESD22- A104 and Appendix 3	3	77	Temperature Cycle	-65C/150C	2000 Cycles	-	-	-	3/231/0	-	-
TC-BP	A4	MIL-STD883 Method 2011	1	5	Post Temp Cycle Bond Pull	-	-	-	1/5/0	-	-	-	-
HTSL	A6	JEDEC JESD22- A103	1	45	High Temperature Storage Life	150C	2000 Hours	-	1/45/0	-	-	-	-
HTSL	A6	JEDEC JESD22- A103	1	45	High Temperature Storage Life	175C	1000 Hours	-	-	-	1/45/0	-	1/77/0
Test Group E	B - Acce	lerated Lifetime	e Simula	tion Tes	ts								
HTOL	B1	JEDEC JESD22- A108	1	77	Life Test	150C	1000 Hours	-	1/77/0	-	3/231/0	-	3/231/0
ELFR	B2	AEC Q100- 008	1	77	Early Life Failure Rate	150C	48 Hours	-	-	-	3/2400/0	-	2/1600/0
Test Group (C - Pack	age Assembly	Integrity	Tests									
WBS	C1	AEC Q100- 001	1	30	Wire Bond Shear	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	-	1/30/0	-	3/90/0	-	-
WBP	C2	MIL-STD883 Method 2011	1	30	Wire Bond Pull	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	-	1/30/0	-	3/90/0	-	-
SD	C3	JEDEC J- STD-002	1	15	PB Solderability	>95% Lead Coverage	-	-	-	-	1/15/0	-	1/15/0
SD	C3	JEDEC J- STD-002	1	15	PB-Free Solderability	>95% Lead Coverage	-	-	-	-	1/15/0	-	1/15/0
PD	C4	JEDEC JESD22- B100 and B108	1	10	Physical Dimensions	Cpk>1.67	-	0/0/0	1/10	0/0/0	3/30/0	0/0/0	0/0/0
Test Group I	D - Die F	abrication Relia	ability Te	sts									
EM	D1	JESD61	-	-	Electromigration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements

Туре	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device	Qual Device	Qual Device	QBS Reference	QBS Reference	QBS Reference
Additional T	Tests												
ED	E5	AEC Q100- 009	3	30	Electrical Distributions	Cpk>1.67 Room, hot, and cold	-	1/30/0	1/30/0	1/30	3/90/0	1/30/0	1/30/0
LU	E4	AEC Q100- 004	1	6	Latch-Up	Per AEC Q100-004	-	Device specific data [1]	1/6/0	Device specific data [1]	1/6/0	2/12/0	2/12/0
ESD	E3	AEC Q100- 011	1	3	ESD CDM	-	500 Volts	Device specific data [1]	1/3/0	Device specific data [1]	1/3/0	-	-
ESD	E3	AEC Q100- 011	1	3	ESD CDM	-	2000 Volts	Device specific data [1]	1/3/0	Device specific data [1]	1/3/0	1/3/0	1/3/0
ESD	E2	AEC Q100- 002	1	3	ESD HBM	-	5000 Volts	-	-	-	1/3/0	1/3/0	1/3/0
ESD	E2	AEC Q100- 002	1	3	ESD HBM	-	2000 Volts	Device specific data [1]	1/3/0	Device specific data [1]	1/3/0	-	-
Test Group	E - Elect	rical Verificatio	n Tests										
SM	D5	-	-	-	Stress Migration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
NBTI	D4	-	-	-	Negative Bias Temperature Instability	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
HCI	D3	JESD60 & 28	-	-	Hot Carrier Injection	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
TDDB	D2	JESD35	-	-	Time Dependent Dielectric Breakdown	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements

- Note[1] The DRV5013AG and DRV5013BC devices have the same process technology, assembly, and build material as DRV5013AD where the only difference is the top metal for the respective threshold adjustments. Hence, they are QBSed to
- Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable
- The following are equivalent HTOL options based on an activation energy of 0.7eV : 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours
 The following are equivalent HTSL options based on an activation energy of 0.7eV : 150C/1k Hours, and 170C/420 Hours
 The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles

Ambient Operating Temperature by Automotive Grade Level:

- Grade 0 (or E): -40C to +150C
- Grade 1 (or O): -40C to +125C
- Grade 2 (or T): -40C to +105C
- Grade 3 (or I): -40C to +85C

E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):

- Room/Hot: THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU
- Room : AC/uHAST

Quality and Environmental data is available at TI's external Web site: http://www.ti.com/

TI Qualification ID: R-CHG-2210-042

ZVEI ID: SEM-PW-13, SEM-PW-02, SEM-PW-09

For questions regarding this notice, e-mails can be sent to the Change Management team or your local Field Sales Representative.

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