PCN Number:		20230702011.0		PCN Date:	July 12, 2023
Title: Datasheet for		r TMS320F2838x			
Customer Contact:		Change Management team	Dept:	Quality Services	
Change Type:		Electrical Specification			
PCN Details					

Description of Change:

Texas Instruments Incorporated is announcing an information only notification.

The product datasheet(s) is being updated as summarized below.

The following change history provides further details.



TMS320F28388D, TMS320F28386D, TMS320F28386D-Q1 TMS320F28384D, TMS320F28384D-Q1, TMS320F28388S TMS320F28386S, TMS320F28386S-Q1, TMS320F28384S, TMS320F28384S-Q1 SPRSP14E - MAY 2019 - REVISED JUNE 2023

С	hanges from February 2, 2021 to June 28, 2023	Page
•	This Revision History lists the changes from SPRSP14D to SPRSP14E.	1
•	Global: Changed "CAN-FD" to "CAN FD"	
•	Global: Changed the Pin Type of ESC_TX0_ENA and ESC_TX1_ENA from "I/O" to "O"	1
•	Features section: Added "Functional Safety-Compliant" feature and "Safety-related certification" feature	re.
	Added "Hardware Built-in Self Test (HWBIST)" feature. Deleted "MCAN (CAN FD)" feature from "Con	nectivity
	Manager (CM)" group. Added "MCAN (CAN FD)" to "CM-C28x shared communications peripherals" of	roup1
•	Description section: Added reference paragraph to Getting Started With C2000™ Real-Time Control	•
	Microcontrollers (MCUs) Getting Started Guide	2
•	Package Information table: Changed table title from Device Information to Package Information.	
	Updated table	2
•	Functional Block Diagram figure: Changed blue MUX arrow of "1x CAN FD"	4
•	Device Comparison table: Updated CAN with Flexible Data-Rate (CAN FD) by changing value to "1 (c	
	assigned to CPU1 or CM)".	
•	Pin Attributes table: Updated table. Changed Ball H4 on 337-ball ZWT package from "NC" to "NC1" a removed pin assignment 119 from 176-pin PTP package. Added "NC2" (Ball J18 on 337-ball ZWT papin 119 on 176-pin PTP package). Changed the description of TRSTn. Deleted duplicate sentence frod description of XRSn. Changed the VSS Description and pin number for the 176-pin package	ckage; om the 18
•	Analog Signals table: Updated table	51
•	Digital Signals table: Updated table	51
•	Power and Ground table: Updated table. Changed the VSS Description and pin number for the 176-	
	pin package	51
•	Test, JTAG, and Reset table: Updated table. Changed "NC" to "NC1". Changed "337 BGA" ball number "H4, J18" to "H4". Deleted "176 Pin" pin number 119. Added "NC2" (337 BGA ball number J18, 176 P number 119). Changed the description of TRSTn. Deleted duplicate sentence from the description of XRSn	in
•	Specifications section: Moved "Stresses beyond those listed under Absolute Maximum Ratings" patext to Absolute Maximum Ratings table as footnotes	

•	Absolute Maximum Ratings table: Added "Stresses beyond those listed under Absolute Maximum Rating	
	footnote and "All voltage values are with respect to VSS, unless otherwise noted" footnote	
•	Recommended Operating Conditions table: Deleted tyddio-RAMP	90
•	ESD Ratings – Commercial table: Removed JEDEC specification JESD22-C101 from Charged-device n	nodel
	(CDM) description. Added CDM values for corner pins	90
•	Power Management Module (PMM) section: Added section	
•	Power Sequencing section: Changed section	
•	Reset Circuit figure: Replaced 4-way tie dot	106
•	Reset Sources section: Updated lead-in paragraph. Added Reset Signals table	106
•	Clocking System figure: Added CLB	
•	Internal Clock Frequencies table: Changed MIN f _(INTCLK) and MIN f _(AUXINTCLK) from 10 MHz to 2 MHz. At f _(CLBTILECLK) and f _(CLBREGCLK)	114
•	XTAL Oscillator section: Changed section title from Crystal Oscillator to XTAL Oscillator. Updated section	n. 115
•	Flash Parameters table: Changed "Nwec Write/Erase Cycles" to "Nwec Write/Erase Cycles per sector". A	dded
	"N _{wec} Write/Erase Cycles for entire Flash (combined all sectors)" and its associated footnote. Added	
	"t _{retention} Data retention duration at T _J = 125°C" and its associated footnote	123
•	RAM Specifications section: Added section	124
•	ROM Specifications section: Added section.	
•	Connecting to the 14-Pin JTAG Header figure: Added 2.2-kΩ pullup resistor on TMS	
•	Connecting to the 20-Pin JTAG Header figure: Added 2.2-kΩ pullup resistor on TMS	
•	EMIF Asynchronous Memory Switching Characteristics table: Updated MIN and MAX values of parameters	
	10, 15, and 24 for EW = 1. Added "Maximum wait timeout condition" footnote	
•	Single-Ended Input Model section: Added "The user should analyze the ADC input setting assuming wo	
	case initial conditions on C _h " paragraph	
	-11 3 1	
	Differential Input Model section: Added references to the Charge-Sharing Driving Circuits for C2000 AD	Cs
	(using TINA-TI simulation tool) Application Note and the ADC Input Circuit Evaluation for C2000 MCUs	
	TINA-TI simulation tool) Application Note	
	Differential Input Model section: Deleted "The user should analyze the ADC input setting assuming wors	
	case initial conditions on C _h " paragraph	
	ADC Timings in 12-Bit Mode (SYSCLK Cycles) table: Added footnote about t _{INT}	
	ADC Timings in 16-Bit Mode table: Added footnote about t _{INT}	
	Comparator Electrical Characteristics table: Added MIN and MAX Hysteresis values	
	CMPSS DAC Dynamic Error section: Added section	
	PMBus Electrical Data and Timing section: Deleted lead-in paragraph	
	PMBus Fast Mode Switching Characteristics table: Added F _{mod} , PMBus Module Clock Frequency	
	PMBus Standard Mode Switching Characteristics table: Added F _{mod} , PMBus Module Clock Frequency	
Ī	Universal Serial Bus (USB) Controller section: Changed Note about the accuracy of the on-chip zero-	223
•	pin oscillator	230
	Modular Controller Area Network (MCAN) [CAN FD] section: Changed first two paragraphs	2/1
	MCAN Module Overview figure: Changed figure	241
Ī	MCAN Module Overview figure: Changed figure	262
:	C28x Memory Map table: Added MCAN Message RAM	
:	Peripheral Registers Memory Map section: Added section	
:	CM Memory Map table: Changed the START ADDRESS and END ADDRESS of "EtherCAT RAM	207
•		274
	(direct access)"	
•		276
•	CM Bus Master Peripheral Access table: Added "Y" to "CPU1 SUBSYSTEM" column of "MCAN (CAN	200
	FD)" row	
•	All Available Boot Modes table: Added footnote about USB Bootloader	205
•	Configurable Logic Block (CLB) section: Added "For normal operation, the clock frequency of the CLB	204
	peripheral is derived from device SYSCLK" paragraph	304
•	CM Clocking System figure: Changed figure title from "Clocking System" to "CM Clocking System".	040
	Removed MCAN	
•	Functional Safety section: Added section.	316
_	Applications Implementation and Layout section: Undated section	247
•	Applications, Implementation, and Layout section: Updated section	
•	Getting Started and Next Steps section: Added section.	
•	Tools and Software section: Added C2000 Third-party search tool	334

The datasheet number will be changing.

Device Family	Change From:	Change To:
TMS320F2838x	SPRSP14D	SPRSP14E

These changes may be reviewed at the datasheet links provided. http://www.ti.com/product/TMS320F28388D

Reason for Change:

To accurately reflect device characteristics.

Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):

No anticipated impact. This is a specification change announcement only. There are no changes to the actual device

Changes to product identification resulting from this PCN:

None.

L	Product Affected:			
	F28384DPTPQR	F28384SZWTS	F28386DZWTS	F28388DZWTS
	F28384DPTPS	F28386DPTPQ	F28386SPTPQR	F28388DZWTSR
	F28384DZWTQR	F28386DPTPQR	F28386SPTPS	F28388SPTPS
	F28384DZWTS	F28386DPTPS	F28386SZWTS	F28388SPTPSR
	F28384SPTPQR	F28386DZWTQ	F28388DPTPS	F28388SZWTS
	F28384SPTPS	F28386DZWTQR	F28388DPTPSR	F28388SZWTSR

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