Product Change Notification / SYST-20MMPB386

Date:

21-Jun-2023

Product Category:

32-bit Microcontrollers

PCN Type:

Document Change

Notification Subject:

Data Sheet - SAM L21 Family Data Sheet

Affected CPNs:

SYST-20MMPB386_Affected_CPN_06212023.pdf
SYST-20MMPB386_Affected_CPN_06212023.csv

Notification Text:

SYST-20MMPB386

Microchip has released a new Datasheet for the SAM L21 Family Data Sheet of devices. If you are using one of these devices please read the document located at SAM L21 Family Data Sheet.

Notification Status: Final

Description of Change:
Section Changes

General
• The SPI, I2S, and I2C standards use the terminology "Master" and "Slave". The equivalent Microchip terminology used in this document is "Host" and "Client" respectively. These terms have been updated throughout this document for this revision.
• This revision contains numerous typographical updates, and formatting updates. Large sections of this data sheet were rewritten to conform to updated standards. Features
• Added new information for PWM outputs using the TC and TCC peripherals SERCOM I2C Pins
• Updated the table header to remove Hs Memories
• Added a new note to table 11-4 in NVM User Row Mapping Processor and Architecture
• Added a new row for the MPU to table 12-2 in Cortex M0+ Address Map PAC
• Updated the register reset property and the bitfield reset for the DSU bit for the STATUSB Register Clock System
• Updated the diagram, changing CLKEN to CHEN in On Demand Clock Requests GCLK
• Updated the GENCTRLn Register with new reset and access properties for the bitfields MCLK

• Updated the text of Clock Ready Flag
• Updated the verbiage for the CKRDY bit in the INTFLAG Register PM
• Removed an erroneous note from Sleep Mode Controller
• Updated the verbiage for the PLRDY bit in the INTFLAG Register OSCCTRL
• Updated the verbiage for the AMPGC bit in the XOSCCTRL Register OSC32KCTRL
• Clarified the verbiage for 1.024 kHz in 32kHz External Crystal Oscillator (XOSC32K) Operation
• Clarified the verbiage for 1.024 kHz in 32kHz Internal Crystal Oscillator (OSC32K) Operation SUPC
• Updated the voltage for BANDGAP in Voltage Reference System Operation
• Updated the verbiage for the BOD33RDY bitfield in the STATUS Register RTC
• Updated the following registers with new Register properties and/or new notes: – CTRLA in COUNT32 Mode – COUNT in COUNT32 Mode – CTRLA in COUNT16 Mode – COUNT in COUNT16 Mode – CTRLA in Clock/Calendar Mode – CLOCK in Clock/Calendar Mode DMAC
• Updated the verbiage for the BASEADDR bitfield in the BASEADDR Register
• Updated the verbiage for the WRBADDR bitfield in the WRBADDR Register
• Updated the verbiage for the SRCADDR bitfield in the SRCADDR Register
• Updated the verbiage for the DSTADDR bitfield in the DSTADDR Register EIC
• Removed erroneous content in Asynchronous Edge Detection Mode (No Debouncing) SAM L21 Datasheet Revision History Complete Data Sheet © 2023 Microchip Technology Inc. and its subsidiaries DS60001477D - 1162 .....continued Section Changes NVMCTRL
• Updated the Overview with new text explaining RWWEE
• Updated the verbiage for the ADDR bitfield in the ADDR Register
• Updated the Register reset property for the LOCK Register and for the LOCK bitfield PORT
• Updated Figure 29-2 in Functional Description with a new note
• Added a note to Events
• Updated table 29-5 in the PIDx bitfield for the EVCTRL Register EVSYS
• Updated the last item in Features
• Added a new column to table 30-1 in Sleep Mode Operation SERCOM
• Added a new item for Fractional Baud rate generation to Features SERCOM USART
• Updated I/O Lines with new verbiage SERCOM SPI
• Updated all instances of Client Select to SPI Select SERCOM I2C
• Updated the links in the Signal Description
• Clarified transmission and reception verbiage for the DRDY bit in the Client INTFLAG Register
• Corrected the bitfield reset values for QCEN in the CTRLB Register
• Updated the bitfield width for the ADDR bitfield in the Host ADDR Register TC
• Updated all instances of INVEN to INVENx
• Updated all instances of TCEINV to TCINV
• Updated Capture Operations with new notes
• Updated the Register properties for the following registers: – CTRLA in 8-bit, 16-bit, and 32-bit Registers – COUNT 8-bit Mode – CCx 8-bit Mode – COUNT 16-bit Mode – COUNT 32-bit Mode TCC
• Updated the following registers with new Register Properties: – CTRLA – COUNT – CCx – PATTBUF – WAVEBUF – PERBUF – CCBUF SAM L21 Datasheet Revision History Complete Data Sheet © 2023 Microchip Technology Inc. and its subsidiaries DS60001477D - 1163 ..... continued Section Changes USB
• Updated table formatting for the FMSTATE bitfield in the FMSTATUS Register
• Removed erroneous bitfields OPMODE2 and TSTPCKT from the CTRLB Register
• Updated bitfield reset properties in the EPINTFLAGn Register
• Updated the register description for the EPINTENSETn Register
• Updated the SPDCONF bitfield of the Host Common CTRLB Register with a new value for 0x3
• Removed an erroneous table from the FLENCE bitfield of the HSOFC Register
• Updated the table for the SPEED bitfield in the STATUS Register
• Updated the table for the FLENHIGH bitfield in the FLENHIGH Register
• Removed an erroneous table from the BINTERVAL bitfield of the BINTERVAL Register
• Updated the table for the SIZE bitfield in the PCKSIZE Register CCL
• Updated the Block Diagram to remove erroneous layers
• Updated the Signal Description with new Pin name information and new verbiage
• Updated figure 40-5 in Truth Table Inputs Selection ADC
• Removed an erroneous note from the Overview
• Removed information regarding erroneous ADC0 from Features
• Updated the verbiage for the SAMPLEN bitfield in the SAMPCTRL Register AC
• Updated the verbiage in VDD Scaler DAC
• Added a note to Events
• Updated Bandgap to voltage for the REFSEL bitfield in the CTRLB Register
• Updated the verbiage for several bitfields in the EVCTRL Register 46. Electrical Characteristics

- Updated Absolute Maximum Ratings with new VPIN specifications
- Updated table 46-8 in Power Consumption with new conditions for OFF mode
- Updated the conditions in table 46-15 in Buck Converter
- Removed an erroneous segment from the equation in Analog-to-Digital Converter (ADC) Characteristics
- Added a note for conditions to table 46-38 in the OPAMP Packaging Information
- Replaced the table in Thermal Resistance Data with a new table 51. Schematic Checklist
- Added notes to the Introduction
- Added a note to Power Supply Connections for table 51-1
- Added a note and removed obsolete content in External Reset Circuit

Impacts to Data Sheet: See above details.

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 21 Jun 2023

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices::N/A

Attachments:

SAM L21 Family Data Sheet

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Affected Catalog Part Numbers (CPN)

ATSAML21E15B-ANT
ATSAML21E15B-AUT
ATSAML21E15B-MNT
ATSAML21E15B-MUT
ATSAML21E16B-ANT
ATSAML21E16B-AUT
ATSAML21E16B-MNT
ATSAML21E16B-MUT
ATSAML21E17B-ANT
ATSAML21E17B-AUT
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