PCN Number:	20230619004.0	PCN Date:	June 21, 2023
Title:	Datasheet for AM62x		
Customer Contact:	Change Management team	Dept:	Quality Services
Change Type:	Electrical Specification		

PCN Details

Description of Change:

Texas Instruments Incorporated is announcing an information only notification.
The product datasheet(s) is being updated as summarized below.
The following change history provides further details.

Changes from November 12, 2022 to June 15, 2023 (from Revision A (NOVEMBER 2022) to Revision B (JUNE 2023)) **Page**

- **Global:** Changed the document product status from "Production Mixed Status" to "Production Data", where both the ALW and AMC packaged devices are fully-qualified with Production Data....1
- **Global:** Added automotive AEC - Q100 device-specific information for the AM625-Q1 and AM620-Q1 devices supported in the 17.2 mm × 17.2 mm AMC package....1
- (Features): Changed the CSI data rate from 2.5Gbps to 1.5Gbps to match the rate defined in the CSI-2 timing section....1
- (Features): Updated the Security features to clarify what is supported....1
- (Features): Included Multi-Media Card (MMC) in the first bullet describing MMC/SD features....1
- (Description): Added AM625-Q1 and AM620-Q1 and updated the descriptions for each device....4
- (Package Information): Updated the table to match the new content standard and added automotive "-Q1" devices....4
- (Functional Block Diagram): Added the Software Build Sheet note....5
- (Device Comparison): Added AM625-Q1 to the AM625 columns and added new columns for the AM620-Q1 devices....9
- (Device Comparison): Corrected the name of the JTAG User ID register....9
- (Pin Connectivity Requirements): Updated the second note to include the meaning of "no connect"....84
- (Pin Connectivity Requirements): Updated the second paragraph of the note following the Connectivity Requirements table. The update clarifies the operation of configurable device IOs and includes precautions that must be taken to prevent floating signals from damaging device input buffers....84
- (ESD Ratings for Devices which are not AEC - Q100 Qualified): Changed the title to clarify the ESD ratings defined in this table apply to devices which are not AEC - Q100 qualified....90
- (ESD Ratings for AEC - Q100 Qualified Devices in the AMC Package): Changed the title to clarify the ESD ratings defined in this table only apply to AEC - Q100 qualified devices in the AMC package....90
- (Recommended Operating Conditions): Created separate table notes for VDD_CANUART and VDDSHV_CANUART....91
- (Operating Performance Points): Changed the Maximum Operating Frequency of the Device/Power Manager (Cortex-R5F) for speed grades "S" and "T" from 800 to 400....93
- (DDR Electrical Characteristics): Added references to the respective JEDEC standards....98
- (Power-Up Sequencing): Added Power-Up Sequencing – Supply / Signal Assignments table with waveform references and notes. Added a new waveform for VDD_CANUART to show its sequence requirements relative to VDD_CORE when powered from a separate always on power source....104

- (Power-Down Sequencing): Added Power-Down Sequencing – Supply / Signal Assignments table with waveform references and notes. Added a new waveform for VDD_CANUART to show its sequence requirements relative to VDD_CORE when powered from a separate always on power source.....107
- (MCU_RESETSTATz, and RESETSTATz Switching Characteristics): Changed the minimum value of parameter RST13 from "0" to "960".....110
- (LFXOSC Modes of Operation): Changed the value of PD_C for BYPASS mode from "X" to "0".....123
- (DSS Switching Characteristics): Added external pixel clock mode "EXTPCLKIN" to parameters D2, D3, D4, and D5. Also changed the "Internal PLL" mode min value for parameters D2 and D3 from "0.0475P" to "0.0475P - 0.3".....137
- (MCASP): Updated each AHCLKR/X table note to include a TRM reference for clock source options. Also corrected a typographical error on the signal name associated with the first waveform in each timing diagram by changing "MCASP[x]_ACLKR/X" to "MCASP[x]_AHCLKR/X".....169
- (MMC0 DLL Delay Mapping): Changed the OTAPDLYENA and OTAPDLYSEL values for Legacy SDR and High Speed SDR modes.....179
- (MMC1/MMC2 DLL Delay Mapping for all Timing Modes): Changed the "UHS-I DR50" mode name to "UHS-I DDR50" to correct a typographical error.....191
- (OSPI Switching Characteristics – PHY Data Training): Added maximum values to the OSPI0_CLK Cycle Time parameter (O1) to define a minimum operating frequency of 133MHz. Also updated Note 1 and Note 4, where "in ns" was added to the OSPI_CLK cycle time reference in Note 1 and "refclk" was changed to "reference clock" in Note 4 so it matches the clock name used in the TRM.....203
- (OSPI0 Switching Characteristics – PHY SDR Mode): Updated Note 1 and Note 4, where "in ns" was added to the OSPI_CLK cycle time reference in Note 1 and "refclk" was changed to "reference clock" in Note 4 so it matches the clock name used in the TRM.....205
- (OSPI0 Switching Characteristics – PHY DDR Mode): Updated Note 1 and Note 4, where "in ns" was added to the OSPI_CLK cycle time reference in Note 1 and "refclk" was changed to "reference clock" in Note 4 so it matches the clock name used in the TRM.....207
- (OSPI0 Timing Requirements – Tap SDR Mode): Updated the constant values associated with the minimum setup and minimum hold formulas in parameters O19 and O20. Note 2 was also updated to change "refclk" to "reference clock" so it matches the clock name used in the TRM.....209
- (OSPI0 Switching Characteristics – Tap SDR Mode): Updated Note 1 and Note 4, where "in ns" was added to the OSPI_CLK cycle time reference in Note 1 and "refclk" was changed to "reference clock" in Note 4 so it matches the clock name used in the TRM.....209
- (OSPI0 Timing Requirements – Tap DDR Mode): Updated the constant values associated with the minimum setup and minimum hold formulas in parameters O13 and O14. Note 2 was also updated to change "refclk" to "reference clock" so it matches the clock name used in the TRM.....211
- (OSPI0 Switching Characteristics – Tap DDR Mode): Updated the minimum data output delay and maximum data output delay formulas in parameter O6. Also updated Note 1 and Note 5, where "in ns" was added to the OSPI_CLK cycle time reference in Note 1 and "refclk" was changed to "reference clock" in Note 5 so it matches the clock name used in the TRM.....211
- (PRUSS PRU Switching Characteristics – Direct Output Mode): Changed the maximum skew value for the GPO to GPO parameter (PRDO1) from 3ns to 2ns.....213
- (PRUSS UART Switching Characteristics): Added a maximum value and units to the start bit low pulse width parameter (4).....218
- (Device Nomenclature): Updated the orderable part number example in the first paragraph by removing the "X" prefix.....241
- (Device Nomenclature): Changed "ALV package type" in the last paragraph to "ALW or AMC package types".....241
- (Device Naming Convention): Added AM620x devices.....243
- (Device Naming Convention): Changed "ppp" to "PPP" to match the upper case letters used in the Standard Package Symbolization figure.....243

The datasheet number will be changing.

Device Family	Change From:	Change To:
AM62x	SPRSP58A	**SPRSP58B**

These changes may be reviewed at the datasheet links provided.
http://www.ti.com/product/AM62x5

Reason for Change:

To accurately reflect device characteristics.

Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):

No anticipated impact. This is a specification change announcement only. There are no changes to the actual device

Changes to product identification resulting from this PCN:

None.

Product Affected:

AM6231ASGGGAALW	AM6231ATCGHAALW	AM6232ATCGGAALW	AM6232ATCGHAALW
AM6234ATCGGAALW	AM6234ATCGHAALW	AM6251ATCGHAALW	AM6252ATCGGAALW
AM6252ATCGHAALW	AM6254ATCGGAALW	AM6254ATCGHAALW	

For questions regarding this notice, e-mails can be sent to the Change Management team or your local Field Sales Representative.