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|--|---------------------------------------|--------------------------|---------------------------|--------------------------|--------------------------|
| PCN Number: | 20230425000.0 | | PCN Date: | April 25, 2023 | |
| Title: | TPS53685 and TPS536C5 Firmware change | | | | |
| Customer Contact: | PCN Manager | | Dept: | Quality Services | |
| Change Type: | | | | | |
| <input type="checkbox"/> | Assembly Site | <input type="checkbox"/> | Assembly Process | <input type="checkbox"/> | Assembly Materials |
| <input checked="" type="checkbox"/> | Design | <input type="checkbox"/> | Electrical Specification | <input type="checkbox"/> | Mechanical Specification |
| <input type="checkbox"/> | Test Site | <input type="checkbox"/> | Packing/Shipping/Labeling | <input type="checkbox"/> | Test Process |
| <input type="checkbox"/> | Wafer Bump Site | <input type="checkbox"/> | Wafer Bump Material | <input type="checkbox"/> | Wafer Bump Process |
| <input type="checkbox"/> | Wafer Fab Site | <input type="checkbox"/> | Wafer Fab Materials | <input type="checkbox"/> | Wafer Fab Process |
| | | <input type="checkbox"/> | Part number change | | |
| PCN Details | | | | | |
| Description of Change: | | | | | |
| <p>This notification is to communicate and update the Firmware for the TPS53685 and TPS536C5 devices. Affected devices are listed in the Product Affected section of this document.</p> <p>The FW_VERSION_INFO.PATCH_VERSION is changing from 01020500h to 01020600h.</p> <p>Additional changes include:</p> <ol style="list-style-type: none"> Factory default checksum updated from 0x39D8 / 0xCEB8 to 0x31D4 / 0xC6B4 (8ph / 12ph): <ul style="list-style-type: none"> OCF pin factory default setting updated from push-pull to open-drain (bit 89 in reg 0xCD) Impact #1: None, it is overwritten by user config file Added/enabled available features as options: disabled by default <ul style="list-style-type: none"> Option to use single threshold for phase shedding / adding all phases simultaneously, consistent with SVI3 specification Support for power stages with CS pin supplied in current instead of voltage Impact #2: None, default setting is unchanged. Default value of SVI3 VID_MAX will be pulled from PMBus VOUT_MAX instead of defaulting to 00h (disabled), consistent with SVI3 VOUT_MAX_SUPPORTED <ul style="list-style-type: none"> Prevents errors if SVI3 OVP_REF is changed to VID_MAX instead of VID Impact #3: None, no change in normal operation. Fixed bug preventing NVM storage of Rail B phase adding / shedding threshold changes <ul style="list-style-type: none"> Enables programming the load current thresholds for different phase add/shed. Impact #4: None, existing thresholds are maintained. Only relevant to customers using DPS and with non-default thresholds. | | | | | |
| Reason for Change: | | | | | |
| Improved device functionality | | | | | |
| Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative): | | | | | |
| None. | | | | | |
| Product Affected: | | | | | |
| TPS53685RSBR | | TPS536C5RSLR | | | |

For questions regarding this notice, e-mails can be sent to the contact shown below or your local Field Sales Representative.

| Location | E-Mail |
|-------------|--|
| WW PCN Team | PCN_ww_admin_team@list.ti.com |

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