Product Change Notification / SYST-29ULUQ503

Date:

30-Mar-2023

Product Category:

Ethernet PHYs

PCN Type:

Document Change

Notification Subject:

Data Sheet - LAN8840 Gigabit Ethernet Transceiver with RGMII and IEEE 1588v2 Support

Affected CPNs:

SYST-29ULUQ503_Affected_CPN_03302023.pdf
SYST-29ULUQ503_Affected_CPN_03302023.csv

Notification Text:

SYST-29ULUQ503

Microchip has released a new Datasheet for the LAN8840 Gigabit Ethernet Transceiver with RGMII and IEEE 1588v2 Support of devices. If you are using one of these devices please read the document located at LAN8840 Gigabit Ethernet Transceiver with RGMII and IEEE 1588v2 Support.

Notification Status: Final

Description of Change:

Section/Figure/Entry	Correction
Throughout Document	Updated “master” to leader and “slave” to follower where appropriate. Grammatical and formatting updates.
Features	Removed “Tolerant” from I/O bullet descriptions
Table1-2, "Buffer Type Descriptions"	Removed VO24, VO5 and PD buffer types.

Table1-2, "Buffer Type Descriptions"	Updated VO8, VOD8 and VOS8 buffer types and 8 mA source and sink descriptions to VO10, VOD10, VOS10 and 10 mA source and sink descriptions.
Section 1.3, "Reference Documents"	Updated reference documents to current 802.3 specification.
Section 2.1, "General Description"	Updated “master or slave modes” to “server or client modes”.
Section 3.1, "Pin Assignments"	Updated Pin Assignment figures to remove preliminary schematic advisory.
Table3-5, "Miscellaneous"	In General Purpose I/O Pin Description, updated “clock” to “Local Time Counter”.
Section 3.3, "Configuration Straps" and Section 3.4, "Pin Alternate Functions"	The following Application Note has been added to the beginning of Section 3.3 and the end of Section 3.4: “Extreme care must be taken on strap input pins that may be used for General Purpose inputs. The General Purpose Inputs must be conditioned or otherwise disabled such that they do not drive incorrect strap input values during the strap loading time.”
Section 3.3.1, "Device Mode Select (MODE[4:0])"	The following note has been removed: “MODE[4:0] definitions are preliminary and subject to change.”
Table3-9, "Device Mode Selections"	Updated “master” to “Leader PHY” and “slave” to “Follower PHY”.
Table3-9, "Device Mode Selections"	The following Application Note has been added to Modes 01010 and 01101: “Normally, Auto-Negotiation is required for operation at 1000Mbps. These forced settings allow manual configuration without Auto-Negotiation, however both the local and link partner devices must support this operation.”
Figure4-1, "Power Connectivity with Internal LDO Controller"	Updated the following pin counts in diagram: VDD updated from 3 pins to 4 pins, VDDAL updated from 4 pins to 2 pins, and VDDAH updated from 3 pins to 2 pins. In note, “MOSFET output” updated to “MOSFET input and output.” In note, “Ferrites on VDDAL and VDDAL_PLL may be combined” replaced with “100K resistor for inrush current migration.”
Figure4-2, "Power Connectivity with External 1.1V Power Supply"	Updated the following pin counts in diagram: VDD updated from 3 pins to 4 pins.
Table5-1, "MDI/MDI-X Pin Mapping"	Row TXRXP/M_C (4, 5), column 100BASE-T updated from “D+/-” to “C+/-”. Row TXRXP/M_D (7, 8), column 100BASE-T updated from “C+/-” to “D+/-”.
Section5.13, Dynamic Channel Quality (DCQ) (TC1 and TC12)	All instances of “TC1” updated to “TC1 and TC12”.
Section5.13, Dynamic Channel Quality (DCQ) (TC1 and TC12)	Added “and Advanced diagnostics features for 1000BASE-T1 automotive Ethernet PHYs Version 1.7” to “These features are designed to be compliant with Sections 6.1.1, 6.1.2, and 6.1.3 of the OPEN Alliance TC1 - Advanced diagnostics features for 100BASE-T1 automotive Ethernet PHYs Version 1.0 specification.”

Section5.13.1, Mean Square Error (MSE) and Section5.13.2, Signal Quality Indicator (SQI)	Updated “The filtered error value is saved every 1.0 ms (125,000 symbols) to “The filtered error value is saved every 65,536 symbols (524,288 us)” and moved several lines above as its own paragraph.
Section5.16.4.1, RGMII ID Timing / TC6 Delay on Source (DoS) mode	Updated “Figure5-14 and Figure5-15 from the RGMII v2.0 Specification...” to “Figure5-14, Figure5-15 and Table5-6 from the RGMII v2.0 Specification...”.
Table5-15, "NAND Tree Test Pin Order"	Added LED5, LED4, and LED3 to table. Updated “LED1/PME_N1” to “LED1”. Updated “INT_N/ PME_N2” to “INT_N”.
Table6-9, "Variable I/O DC Electrical Characteristics VDDIO = 1.8/2.5/3.3V"	Removed “Effective Pull-Down Resistance” and “VO5 Type Buffer” information.
Section6.0, Operational Characteristics	Removed “On-Chip LDO Controller,” “Reference Circuits - LED Strap-In Pins” and “1588 GPIO Timing” sections from Operational Characteristics chapter.
Section7.0, Package Outline	Updated Package Marking Information.

Impacts to Data Sheet: See above details

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 30 Mar 2023

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

LAN8840 Gigabit Ethernet Transceiver with RGMII and IEEE 1588v2 Support

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Affected Catalog Part Numbers (CPN)

LAN8840/PSA
LAN8840-V/PSA
LAN8840T-V/PSA
LAN8840T/PSA