



## Product Change Notification / SYST-10YSFP517

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### Date:

11-Apr-2023

### Product Category:

32-bit Microcontrollers

### PCN Type:

Document Change

### Notification Subject:

Data Sheet - EEC1005 Enterprise Storage Backplane Management Processor

### Affected CPNs:

[SYST-10YSFP517\\_Affected\\_CPN\\_04112023.pdf](#)

[SYST-10YSFP517\\_Affected\\_CPN\\_04112023.csv](#)

### Notification Text:

SYST-10YSFP517

Microchip has released a new Datasheet for the EEC1005 Enterprise Storage Backplane Management Processor of devices. If you are using one of these devices please read the document located at [EEC1005 Enterprise Storage Backplane Management Processor](#).

**Notification Status:** Final

**Description of Change:**

Section/Figure/Entry	Correction
Throughout Document	Changed "slave" terminology to "target" where necessary
Section 3.0, "Configurations"	Two new UB2 Configuration settings added (0x16, 0x17). Add definition of "Min" pinout Configurations.
Section 10.0, "UB2 Enhancements"	The additional Configurations 0x16 and 0x17 listed and described.
Section 10.2, "LED Test Mode"	LED Test Mode blink pattern specified.
Section 7.0, "UBM Controller Commands"	Add table of all UBM commands.
Section 2.3, "BMC-Tunneled I2C HFC Emulation"	I2C addresses changed to 8-bit forms uniformly, to

	match Standard. Addressing clarified generally.
Section 3.0, "Configurations"	Three new UB2 Configuration settings added (0x13, 0x14, 0x15). Specific resistor values filled in.
Section 10.0, "UB2 Enhancements"	Three additional Configurations listed and identified by function.
Section 2.3, "BMC-Tunneled I2C HFC Emulation", Cover Page (Features)	Add section capturing addresses used, add to Features list.
Table4-1: Configuration FRU	Add declaration entries for: Clock Routing, PERST Support, PERST Management Override, PWRDIS Support
Section 7.0, "UBM Controller Commands"	Clarify that the command list is not comprehensive, and holds only some commands that require comment for EEC1005 application.
Section 7.6, "Capabilities (0x33)"	Fix errata in fields SLOT POWER CONTROL, PCIE RESET CONTROL, 2WIRE RESET
Section 10.1.1, "Background"	Update Intel VPP modes to new, simpler simultaneous support.
Various	Customer application references redacted. Misc changes to phrasing for accuracy.
Product Identification System Page, Cover Page (Features), Section 1.0, "General Description"	Adds UB2 enhanced version, and identifies original version as UB1. Adds UB1 vs. UB2 ordering information.
Section 10.0, "UB2 Enhancements"	New features in UB2 version listed and identified.
Section 3.0, "Configurations"	New UB2 Configuration settings added.
Section 11.2, "Strap pins"	New UB2 Strap Pin usages added.
Section 7.1, "Silicon Identity and Version (0x02)", Section 7.6, "Capabilities (0x33)"	New UB2 Changes to UBM command formats for Revision 1.4 standard.
Section TABLE 11-7:, "UBM Controller - 144 Pin ALT Package"	New Configuration Pinout table added
Section TABLE 11-3:, "UBM Controller - 144 Pin Package"	Fixed Pin swap of B9-F8 and B8-F9
Section TABLE 11-1:, " EEC1005 Strap Pins"	Added Strap pins table
Section TABLE 3-1:, "EEC1005 Configuration Select"	Added 144 pin UBM ALT configuration and ID numbers corrected
Section TABLE 4-1:, "Configuration FRU table"	Added Note on LED Pattern selection
Section TABLE 8-1:, "IBPI LED Blink Pattern"	Updated LED blink pattern table as per SFF8489 Spec for 2 LEDs

**Impacts to Data Sheet:** See above details.

**Reason for Change:** To Improve Productivity

**Change Implementation Status:** Complete

**Date Document Changes Effective:** 11 Apr 2023

**NOTE:** Please be advised that this is a change to the document only the product has not been changed.

**Markings to Distinguish Revised from Unrevised Devices:** N/A

## Attachments:

## EEC1005 Enterprise Storage Backplane Management Processor

Please contact your local [Microchip sales office](#) with questions or concerns regarding this notification.

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Affected Catalog Part Numbers (CPN)

EEC1005-I/SX1-UB1

EEC1005-I/WC-UB1