Revision 1.0.0
ADV Issue Date: 04/14/2023

CUSTOMER ADVISORY

ADV2306

Intel Agilex® 7 Pin Connection Guidelines Update

Description:

Intel® is notifying customers of updates to the Intel® Agilex® 7 Device family Pin Connection Guidelines (PCG). Please note that there is no change to the design of the device.

Here is the link to the updated Agilex® 7 Pin Connection Guidelines (PCG) document:
https://www.intel.com/content/www/us/en/docs/programmable/683112/current/device-family-pin-connection-guidelines.html

Below table lists the updates in the Agilex® 7 Device family Pin Connection Guidelines. These changes are also summarized in the revision history section within the PCG document.

• Added a footnote for the VCCH_SDM pin in Table: Power Supply Sharing Guidelines for Intel Agilex 7 Devices with F-Tile and R-Tile Transceivers. Refer to Table 36 on Page 68.
• Updated the HPS_COLD_nRESET signal description in Table: SDM Optional Signal Pins. , Refer to Table 13 on Page 29.
• Updated the connection guidelines of the VCCH pin. Refer to Table 11 on Page 16.
• Updated the connection guidelines of the GT[L,R]_RX_Q[0,1,2,3]_CH[0,1,2,3]P and FGT[L,R]_RX_Q[0,1,2,3]_CH[0,1,2,3]N pins. Refer to Table 19 on Page 40.

• Updated the connection guidelines of the VCCERT1_FHT_GXF[L,R] and VCCERT2_FHT_GXF[L,R] pins. Refer to Table 18 on Page 37.
• Updated Table: Power Supply Sharing Guidelines for Intel Agilex 7 Devices with P-Tile and E-Tile Transceivers and Table: Power Supply Sharing Guidelines for Intel Agilex 7 Devices with F-Tile and R-Tile Transceivers to combine the VCCFUSEWR_SDM with VCCIO_SDM and VCCIO_HPS rails. Refer to Table 35 on Page 64 and Table 36 on Page 68.
• Updated Table: Power Supply Sharing Guidelines for Intel Agilex 7 Devices with F-Tile and R-Tile Transceivers to combine the VCCERT_FGT_GXF with VCCERT1_FHT_GXF and VCCERT2_FHT_GXF rails. Refer to Table 36 on Page 68.
• Updated Figure: Example Power Supply Sharing Guidelines for Intel Agilex 7 Devices with P-Tile and E-Tile Transceivers and Figure: Example Power Supply Sharing Guidelines for Intel Agilex 7 Devices with F-Tile and R-Tile Transceivers to combine the VCCFUSEWR_SDM with VCCIO_SDM and VCCIO_HPS rails. Refer to Figure 1 on Page 67 and Figure 2 on Page 71.
• Updated Figure: Example Power Supply Sharing Guidelines for Intel Agilex 7 Devices with F-Tile and R-Tile Transceivers to combine the VCCERT_FGT_GXF with VCCERT1_FHT_GXF and VCCERT2_FHT_GXF rails. Refer to Figure 2 on Page 71.
• Updated the pin description of the VCCRCORE pin. Refer to Table 11 on Page 16.
• Updated the connection guidelines of the VCCHFUSE_GXR[L,R] pins Refer to Table 20 on Page 42.
• Updated the R-Tile Transceiver Pins section to include guidelines for the Intel Agilex™ 7 AGI041 device. Refer to Table 21 on Page 43.
• Updated the VCCFUSEWR_SDM notes in the following tables: — Table: Power Supply Sharing Guidelines for Intel Agilex 7 Devices with P-Tile and E-Tile

Transceivers — Table: Power Supply Sharing Guidelines for Intel Agilex 7 Devices with F-Tile and R-Tile Transceivers Refer to Table 35 on Page 64 and Table 36 on Page 68.
• Updated product family name to "Intel Agilex 7".
• Retitled the document from Intel Agilex Device Family Pin Connection Guidelines to Intel Agilex 7 Device Family Pin Connection Guidelines.

Recommended Action:

Customers are requested to review the change and determine the impact on their designs. Refer to the revision history of the PCG documents for complete list and history of updates.

For question or support, please contact your local Sales representative, or submit a question or request at the My Intel support page, log-in via:
https://www.intel.com/content/www/us/en/my-intel/fpga-sign-in.html

Products Affected:

The list of affected part numbers (OPNs) can be downloaded in Excel form:
https://cdrdv2.intel.com/v1/dl/getContent/776674?explicitVersion=true

Change Implementation:

Table 1:

Milestones	Availability
Availability of Intel® Agilex®7 PCG document Updates	Now

Contact:

For more information, please contact your local Sales representative, or submit a question or request at the My Intel support page, log-in via:
https://www.intel.com/content/www/us/en/my-intel/fpga-sign-in.html

Customer Notifications Subscription

If you would like to receive customer notifications by email, please follow the instructions in ADV 2209

Intel references J-STD-046 guidelines for PCN.
In accordance with J-STD-046, this change is deemed acceptable to the customer if no acknowledgement is received within 30 days from date of notification.

Revision History:

Date	Rev	Description
04/14/2023	1.0.0	Initial Release