

Dual N-Channel 12-V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^a	Q_g (Typ.)
12	0.040 at $V_{GS} = 4.5$ V	4.5	4.5 nC
	0.048 at $V_{GS} = 2.5$ V	4.5	
	0.063 at $V_{GS} = 1.8$ V	4.5	

FEATURES

- Halogen-free
- TrenchFET[®] Power MOSFET
- New Thermally Enhanced PowerPAK[®] SC-70 Package
- Small Footprint Area

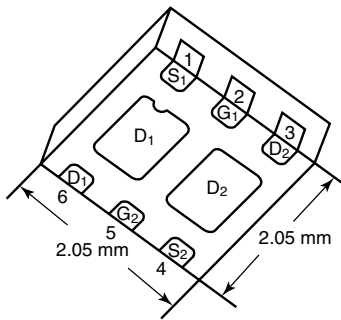


RoHS
COMPLIANT

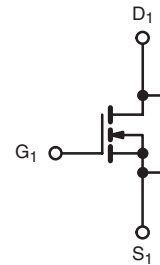
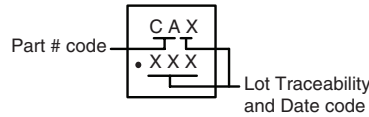
APPLICATIONS

- Load Switch for Portable Applications

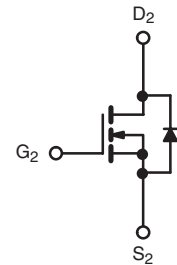
PowerPAK SC-70-6 Dual



Marking Code



N-Channel MOSFET



N-Channel MOSFET

Ordering Information: SiA912DJ-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	12	V
Gate-Source Voltage	V_{GS}	± 8	
Continuous Drain Current ($T_J = 150^\circ\text{C}$)	$T_C = 25^\circ\text{C}$	4.5 ^a	A
	$T_C = 70^\circ\text{C}$	4.5 ^a	
	$T_A = 25^\circ\text{C}$	4.5 ^{a, b, c}	
	$T_A = 70^\circ\text{C}$	4.5 ^{a, b, c}	
Pulsed Drain Current	I_{DM}	20	A
Continuous Source-Drain Diode Current	$T_C = 25^\circ\text{C}$	4.5 ^a	
	$T_A = 25^\circ\text{C}$	1.6 ^{b, c}	
Maximum Power Dissipation	$T_C = 25^\circ\text{C}$	6.5	W
	$T_C = 70^\circ\text{C}$	5	
	$T_A = 25^\circ\text{C}$	1.9 ^{b, c}	
	$T_A = 70^\circ\text{C}$	1.2 ^{b, c}	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, f}	R_{thJA}	52	65	$^\circ\text{C/W}$
Maximum Junction-to-Case (Drain)	R_{thJC}	12.5	16	

Notes:

a. Package limited

b. Surface Mounted on 1" x 1" FR4 board.

c. $t = 5$ s.

d. See Solder Profile (<http://www.vishay.com/ppg?73257>). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

f. Maximum under Steady State conditions is 110°C/W .

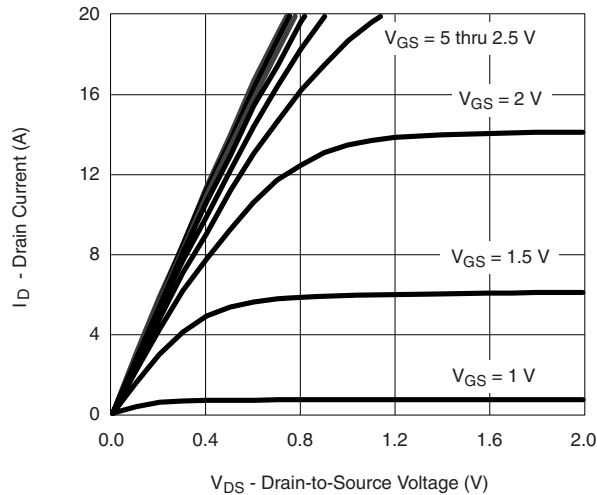
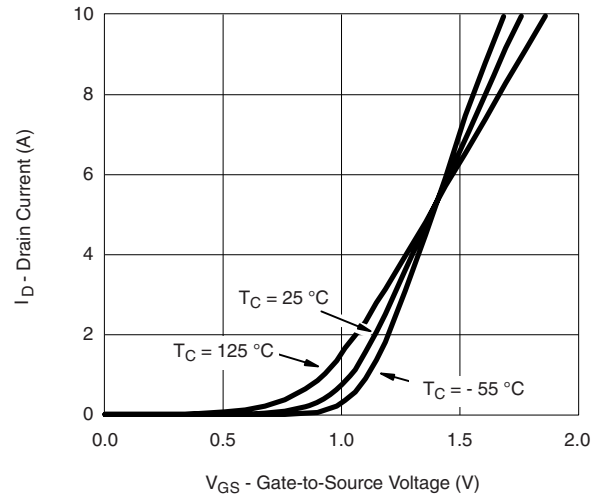
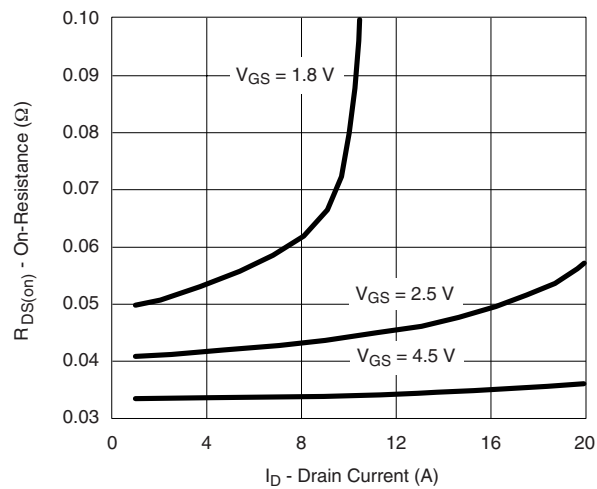
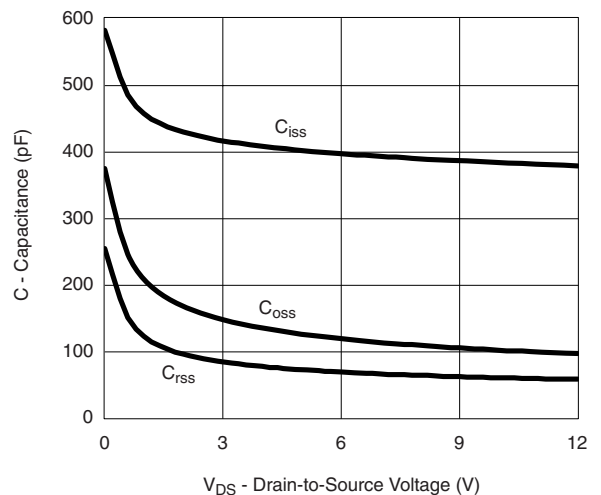
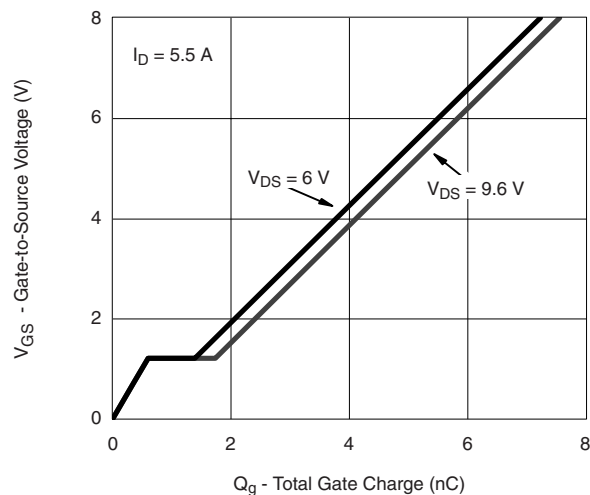
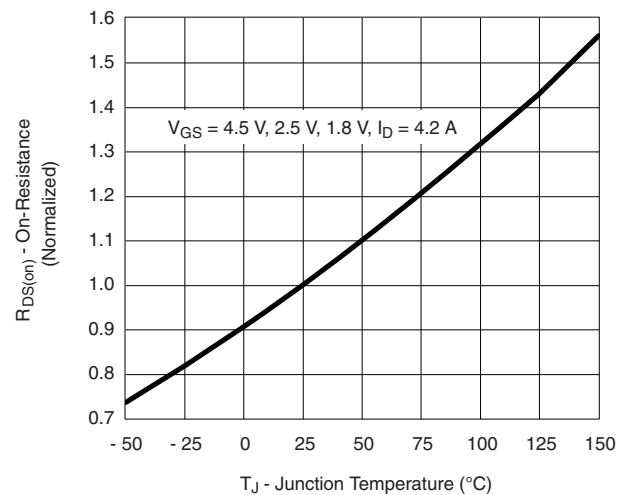
SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	12			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		12		mV/ $^{\circ}\text{C}$
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 2.8		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	0.4		1.0	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 8\text{ V}$			± 100	ns
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 12\text{ V}$, $V_{GS} = 0\text{ V}$			- 1	μA
		$V_{DS} = 12\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 55\text{ }^{\circ}\text{C}$			- 10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \leq 5\text{ V}$, $V_{GS} = 4.5\text{ V}$	- 20			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 4.5\text{ V}$, $I_D = 4.2\text{ A}$		0.033	0.040	Ω
		$V_{GS} = 2.5\text{ V}$, $I_D = 3.8\text{ A}$		0.039	0.048	
		$V_{GS} = 1.8\text{ V}$, $I_D = 1.6\text{ A}$		0.051	0.063	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 6\text{ V}$, $I_D = 4.2\text{ A}$		13		S
Dynamic ^b						
Input Capacitance	C_{iss}	$V_{DS} = 6\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$		400		pF
Output Capacitance	C_{oss}			120		
Reverse Transfer Capacitance	C_{rss}			70		
Total Gate Charge	Q_g	$V_{DS} = 6\text{ V}$, $V_{GS} = 8\text{ V}$, $I_D = 5.5\text{ A}$		7.5	11.5	nC
Gate-Source Charge	Q_{gs}	$V_{DS} = 6\text{ V}$, $V_{GS} = 4.5\text{ V}$, $I_D = 5.5\text{ A}$		4.5	6.8	
Gate-Drain Charge	Q_{gd}			0.6		
Gate Resistance	R_g			0.8		
Turn-on Delay Time	$t_{d(on)}$	$f = 1\text{ MHz}$		2.5		Ω
Rise Time	t_r					
Turn-Off Delay Time	$t_{d(off)}$					
Fall Time	t_f					
Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = 6\text{ V}$, $R_L = 1.4\text{ }\Omega$ $I_D \cong 4.4\text{ A}$, $V_{GEN} = 4.5\text{ V}$, $R_g = 1\text{ }\Omega$		5	10	ns
Rise Time	t_r			15	25	
Turn-Off Delay Time	$t_{d(off)}$			35	55	
Fall Time	t_f			15	25	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = 6\text{ V}$, $R_L = 1.6\text{ }\Omega$ $I_D \cong 4.4\text{ A}$, $V_{GEN} = 8\text{ V}$, $R_g = 1\text{ }\Omega$		5	10	
Rise Time	t_r			10	15	
Turn-Off Delay Time	$t_{d(off)}$			15	25	
Fall Time	t_f			10	15	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^{\circ}\text{C}$			4.5	A
Pulse Diode Forward Current	I_{SM}				20	
Body Diode Voltage	V_{SD}	$I_S = 4.4\text{ A}$, $V_{GS} = 0\text{ V}$		0.8	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 4.4\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $T_J = 25\text{ }^{\circ}\text{C}$		15	30	ns
Body Diode Reverse Recovery Charge	Q_{rr}			8	20	nC
Reverse Recovery Fall Time	t_a			8.5		ns
Reverse Recovery Rise Time	t_b			6.5		

Notes:

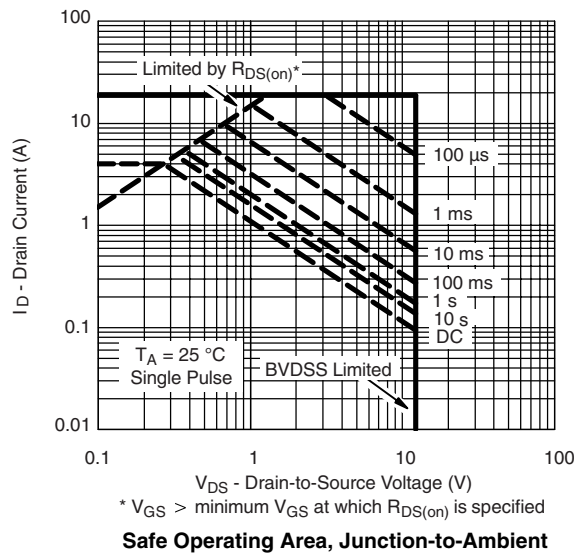
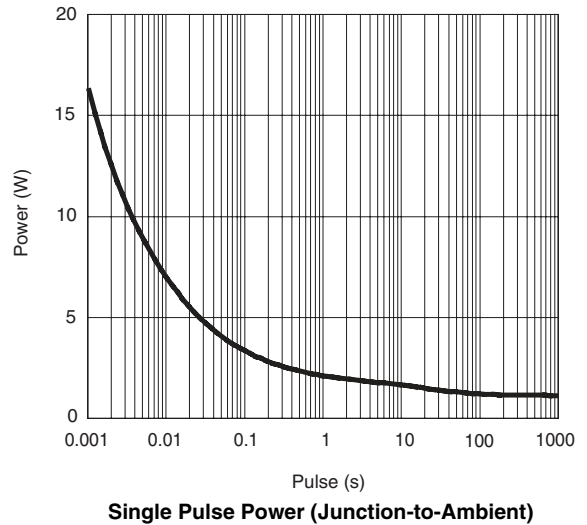
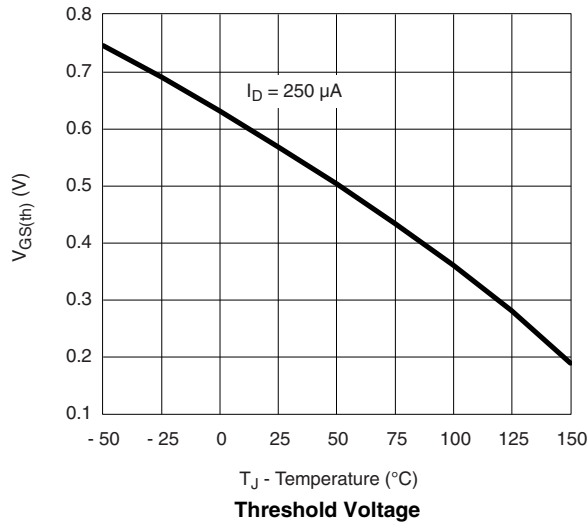
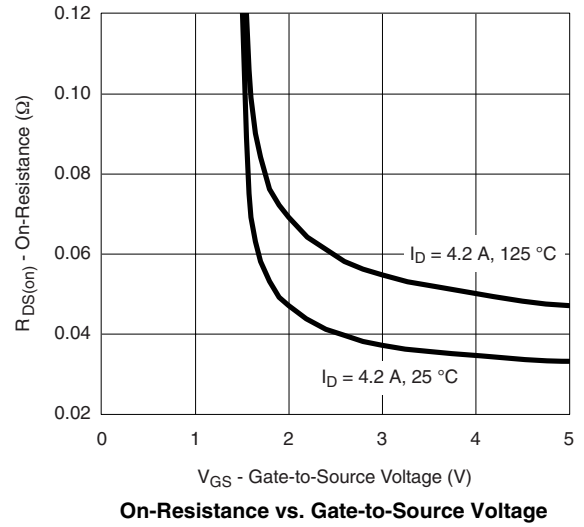
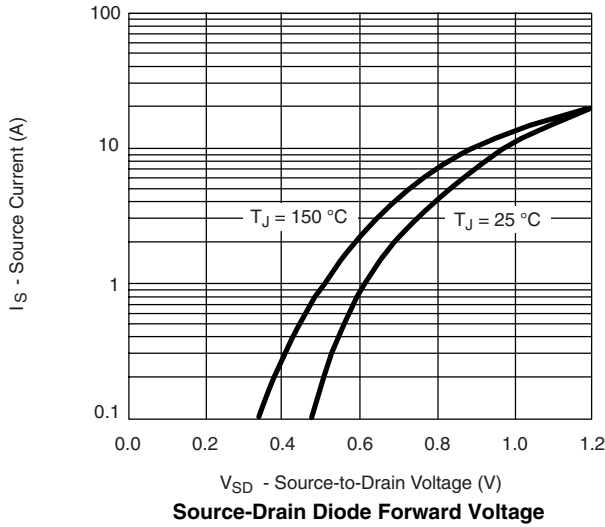
a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$

b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

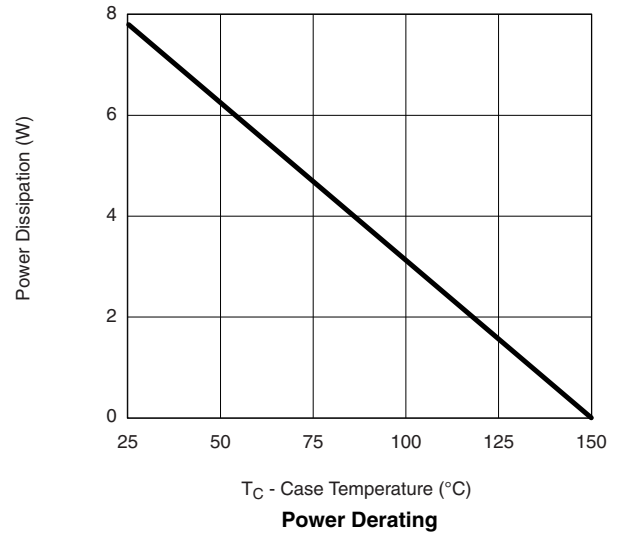
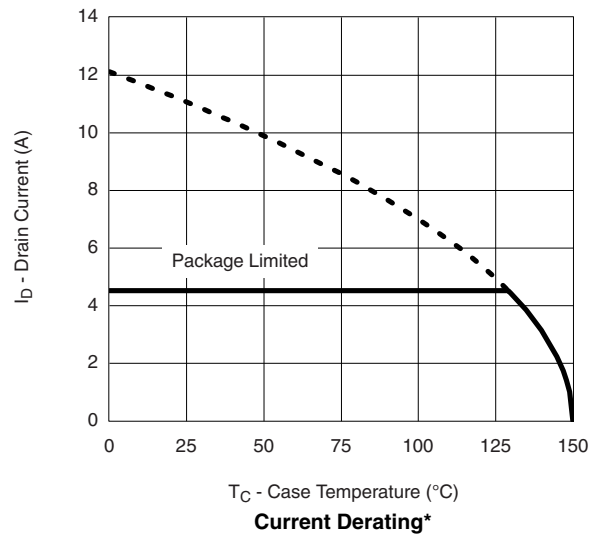
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted**Output Characteristics****Transfer Characteristics****On-Resistance vs. Drain Current and Gate Voltage****Capacitance****Gate Charge****On-Resistance vs. Junction Temperature**

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

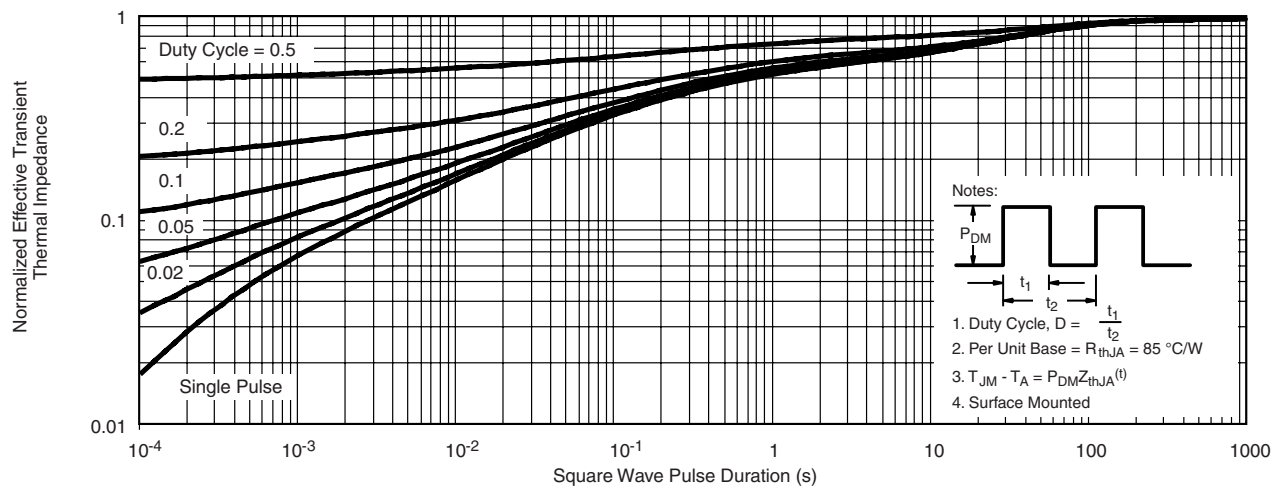
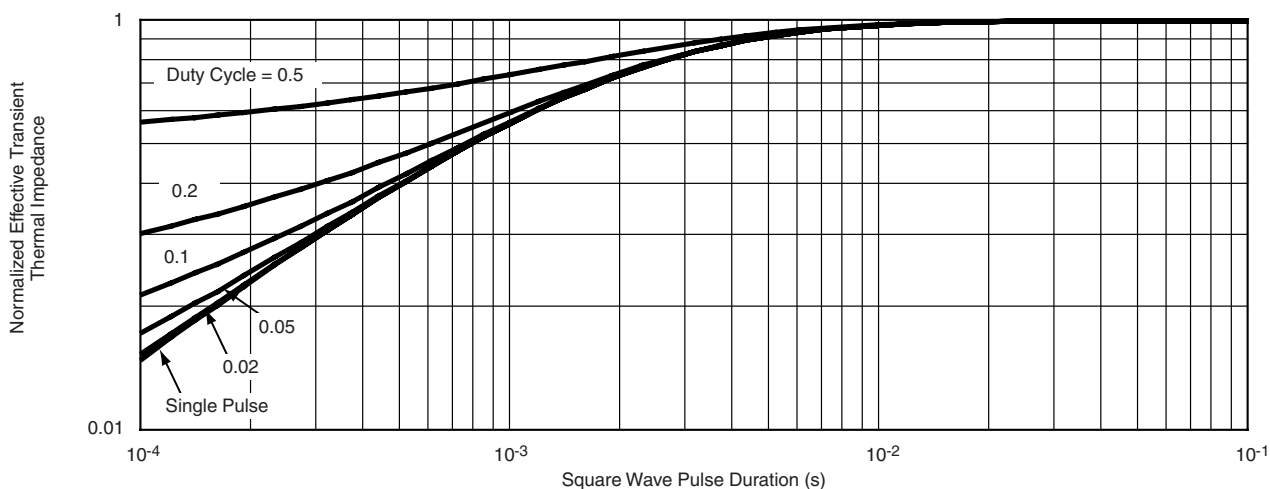




TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted**Normalized Thermal Transient Impedance, Junction-to-Ambient****Normalized Thermal Transient Impedance, Junction-to-Foot**

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