

MCT024L6W240320PML	240 x 320	MCU 16 BITS Interface	TFT Module
Specification			
Version: 1		Date: 16/09/2015	
Revision			
1	14/09/2015	First issue	

Display Features			
Display Size	2.4"		
Resolution	240 x 320		
Orientation	Portrait		
Appearance	RGB		
Logic Voltage	2.8V		
Interface	MCU 16 BITS		
Brightness	250 cd/m ²		
Touchscreen	---		
Module Size	47.20 x 60.26 x 2.45mm		
Operating Temperature	-20°C ~ +70°C		
Pinout	40 way FFC		
Pitch	0.5mm	Box Quantity	Weight / Display
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* - For full design functionality, please use this specification in conjunction with the ILI9341 specification.(Provided Separately)

Display Accessories	
Part Number	Description
MPBV6	40 Way FFC to cable and wires. Driven by any driver board that can be wired to a 1mm pitch SHDR-40V-S-B receptacle.

Optional Variants	
Appearances	Voltage

1. GENERAL SPECIFICATIONS

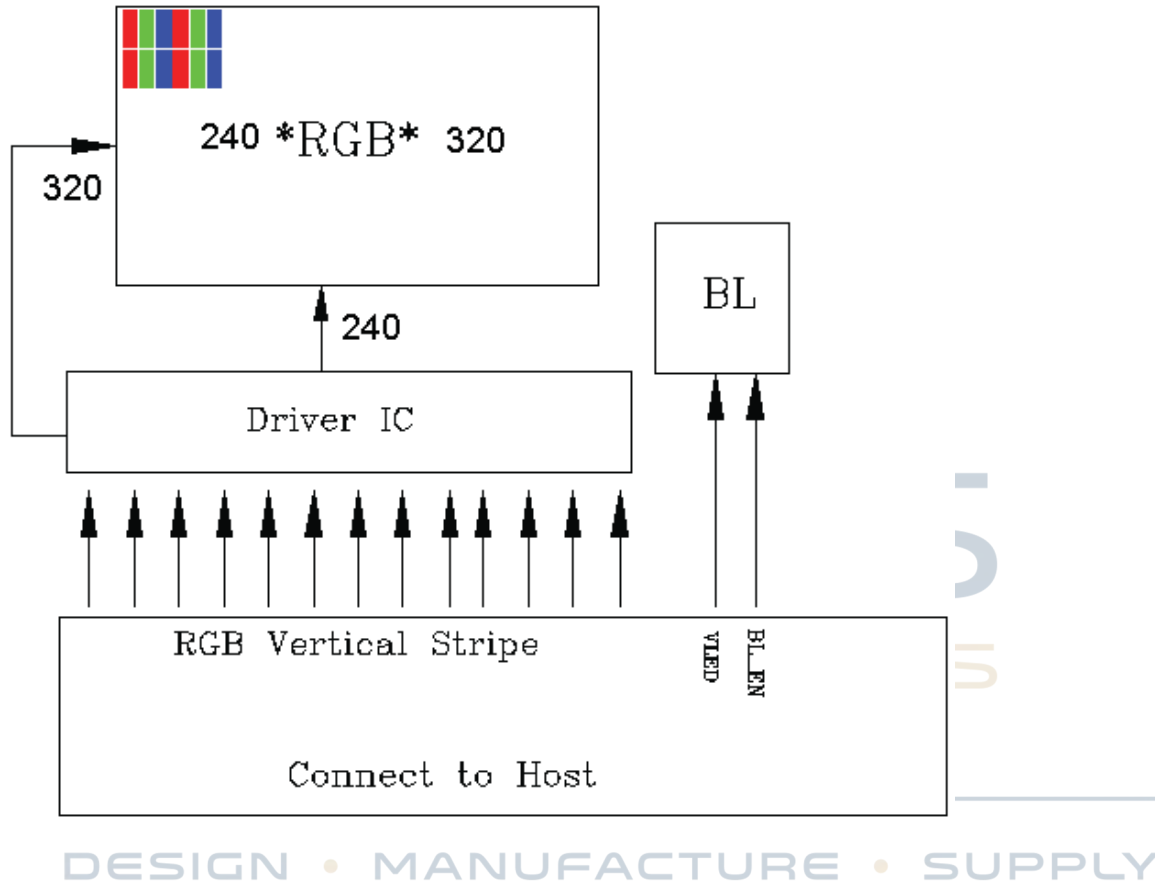
ITEM	SPECIFICATION	UNIT
OUTLINE DIMENSIONS	47.2 (W) X60.26 (H) X2.45 (D)	mm
DISPLAY SIZE	2.4	inch
DOT PITCH	0.153mmX0.153mm	mm
NUMBER OF DOTS	240* (RGB) *320	-
DRIVER IC	ILI9341	-
LCD TYPE	TFT(262K) TRANSMISSIVE	-
INTERFACE	MCU 16 BITS	
BACKLIGHT TYPE	LED White	-
VIEWING DIRECTION	6 O'clock	-

*See attached drawing for details.

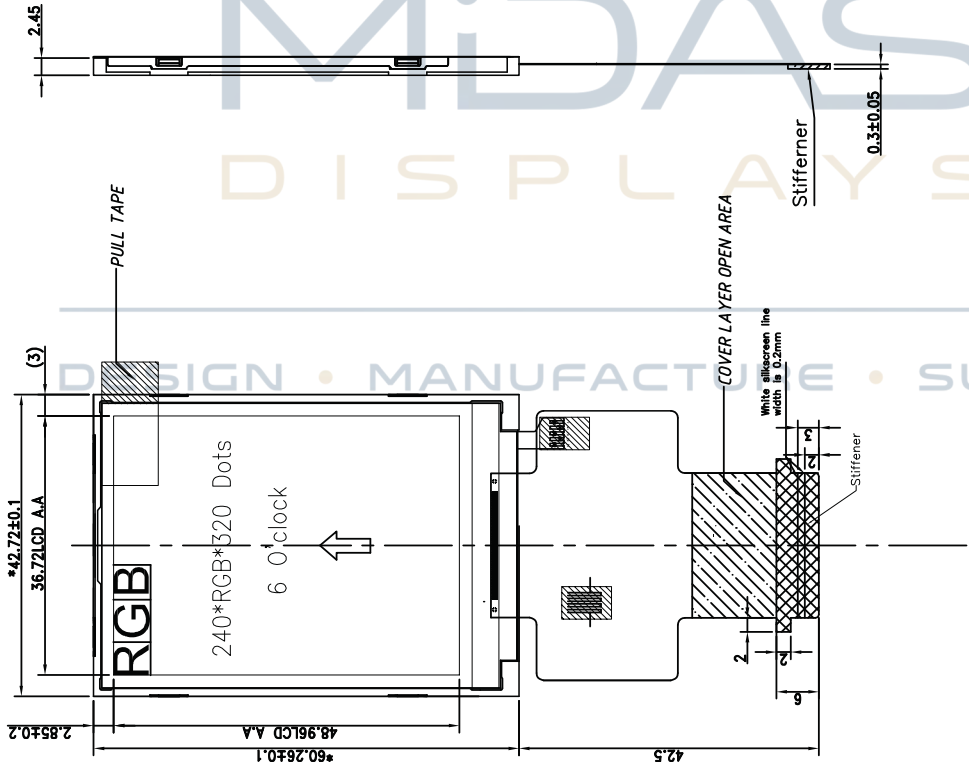
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2. BLOCK DIAGRAM

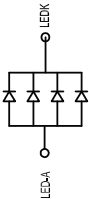
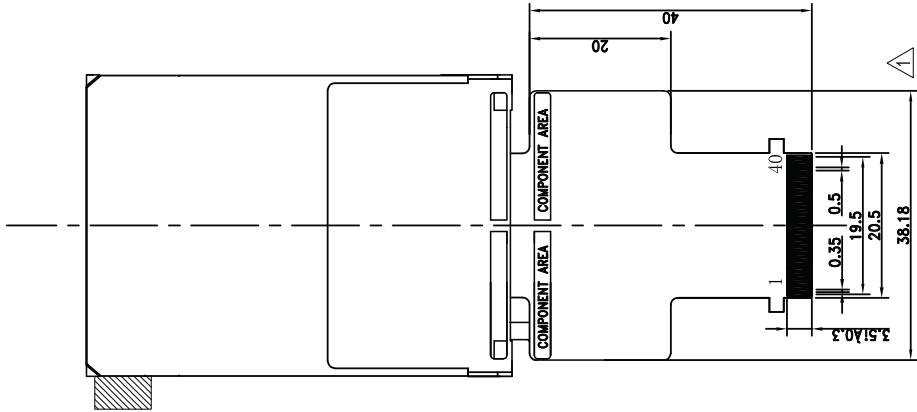


3. DIMENSIONAL OUTLINE



NOTES:

- 1. Display type: 2.4" TFT, 240(RGB)X320
- 2. Viewing angle: 6 O'clock
- 3. Display mode: 262K TFT/Transmissive/Normal White
- 4. Operating temp.: -20°C~+70°C
- 5. Storage temp.: -30°C~+80°C
- 6. IC: ILI9341
- 7. Logic power supply voltage: 2.8V
- 8. Backlight: 4 chip White LED , In Parallel, If=60mA
- 9. Luminance: 250cd/m2
- 10. All the raw material are Rohs compicant



B/L CIRCUIT DIAGRAM
4 PCS WHITE LED;IF =60mA,VF=3.2V

4. PIN DESCRIPTION:

NO.	PIN NAME	Type	Description																																																																																												
1	LEDK	P	Power supply for LED (Cathode)																																																																																												
2	LEDA	P	Power supply for LED (Anode)																																																																																												
3	GND	P	Ground(0V)																																																																																												
4~6	NC	-	No connection																																																																																												
7	SDA	I/O	SPI Serial Data Input/output																																																																																												
8	DOTCLK	I	Pixel clock signal																																																																																												
9	DE	I	Data enable																																																																																												
10	VSYNC	I	Vertical synchronizing signal																																																																																												
11	HSYNC	I	Horizontal synchronizing signal																																																																																												
12	VCC	P	Power voltage																																																																																												
13	RESET	I	Reset signal																																																																																												
14	GND	P	Ground(0V)																																																																																												
15~32	DB17~DB0	I/O	Data bus - Select the MCU interface mode																																																																																												
			IM3	IM2	IM1	IM0	MCU-Interface Mode	DB Pin in use		Register/Content	GRAM	0	0	0	0	80 MCU 8-bit bus interface I	D[7:0]	D[7:0]	0	0	0	1	80 MCU 16-bit bus interface I	D[7:0]	D[15:0]	0	0	1	0	80 MCU 9-bit bus interface I	D[7:0]	D[8:0]	0	0	1	1	80 MCU 18-bit bus interface I	D[7:0]	D[17:0]	0	1	0	1	3-wire 9-bit data serial interface I	SDA: In/OUT		0	1	1	0	4-wire 8-bit data serial interface I	SDA: In/OUT		1	0	0	0	80 MCU 16-bit bus interface II	D[8:1]	D[17:10], D[8:1]	1	0	0	1	80 MCU 8-bit bus interface II	D[17:10]	D[17:10]	1	0	1	0	80 MCU 18-bit bus interface II	D[8:1]	D[17:0]	1	0	1	1	80 MCU 9-bit bus interface II	D[17:10]	D[17:9]	1	1	0	1	3-wire 9-bit data serial interface II	SDI: In SDO: Out		1	1	1	0	4-wire 8-bit data serial interface II	SDI: In SDO: Out	
								IM3	IM2	IM1	IM0	MCU-Interface Mode	DB Pin in use																																																																																		
			Register/Content	GRAM																																																																																											
			0	0	0	0	80 MCU 8-bit bus interface I	D[7:0]	D[7:0]																																																																																						
			0	0	0	1	80 MCU 16-bit bus interface I	D[7:0]	D[15:0]																																																																																						
			0	0	1	0	80 MCU 9-bit bus interface I	D[7:0]	D[8:0]																																																																																						
			0	0	1	1	80 MCU 18-bit bus interface I	D[7:0]	D[17:0]																																																																																						
			0	1	0	1	3-wire 9-bit data serial interface I	SDA: In/OUT																																																																																							
			0	1	1	0	4-wire 8-bit data serial interface I	SDA: In/OUT																																																																																							
			1	0	0	0	80 MCU 16-bit bus interface II	D[8:1]	D[17:10], D[8:1]																																																																																						
			1	0	0	1	80 MCU 8-bit bus interface II	D[17:10]	D[17:10]																																																																																						
			1	0	1	0	80 MCU 18-bit bus interface II	D[8:1]	D[17:0]																																																																																						
			1	0	1	1	80 MCU 9-bit bus interface II	D[17:10]	D[17:9]																																																																																						
			1	1	0	1	3-wire 9-bit data serial interface II	SDI: In SDO: Out																																																																																							
			1	1	1	0	4-wire 8-bit data serial interface II	SDI: In SDO: Out																																																																																							
			MPU Parallel interface bus and serial interface select																																																																																												
			If use RGB Interface must select serial interface.																																																																																												
*: Fix this pin at VDDI or VSS.																																																																																															
33	RD	I	Read signal, active at low in MCU mode; In RGB and SPI mode, connect to GNG																																																																																												
34	WR	I	Write Signal, active at low in MCU mode; In RGB and SPI mode ,SPI Serial Clock																																																																																												
35	RS	I	In MCU mode, Register select signal, low is selected data register; High is selected command register. In RGB and SPI mode, connect to GND																																																																																												
36	CS	I	Chip selection pin/ Serial port data enable signal																																																																																												
37	XR(NC)	-	No connection																																																																																												
38	YD(NC)	-	No connection																																																																																												
39	XL(NC)	-	No connection																																																																																												
40	YU(NC)	-	No connection																																																																																												

Note: 1: input, 0: output, P: Power;

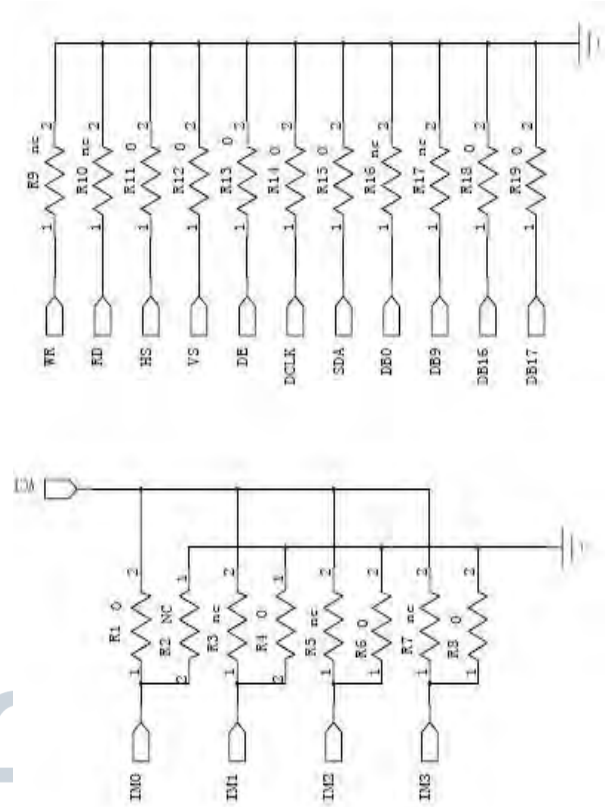
Note: 2: LCM have set to 80 MCU 16-bit bus interface I. Below is circuit on FPC for IM3~IM0.

[Link to example connector](#)

IM3	IM2	IM1	IM0	MCU-Interface Mode	DB pin in use		PIN of LCM to Gnd
					Register/content	GRAM	
0	0	0	0	80 MCU 8bit -bus	DB(7-0)	DB(7-0)	HS,VS,DE,DCLK,SDA,DB8-DB17
0	0	0	1	80 MCU 16bit -bus	DB(7-0)	DB(15-0)	HS,VS,DE,DCLK,SDA,DB16,DB17
0	0	1	0	80 MCU 9bit -bus	DB(7-0)	DB(8-0)	HS,VS,DE,DCLK,SDA,DB9-DB17
0	0	1	1	80 MCU 18bit -bus	DB(7-0)	DB(17-0)	HS,VS,DE,DCLK,SDA
0	1	0	1	3-wire 9-bit date serial	SDA in/out		HS,VS,DE,DCLK,RS,RD,DB0-DB17
0	1	1	0	4-wire 8-bit date serial	SDA in/out		HS,VS,DE,DCLK,RD,DB0-DB17
1	0	0	0	80 MCU 16bit -bus	DB(8-1)	DB(17-10) (8-1)	HS,VS,DE,DCLK,SDA,DB0,DB9
1	0	0	1	80 MCU 8bit -bus	DB(17-10)	DB(17-10)	HS,VS,DE,DCLK,SDA,DB0-DB9
1	0	1	0	80 MCU 18bit -bus	DB(17-10)	DB(17-0)	HS,VS,DE,DCLK,SDA
1	0	0	1	80 MCU 9bit -bus	DB(8-0)	DB(17-9)	HS,VS,DE,DCLK,SDA,DB0-DB8
R6=0	R5=0	R3=0	R1=0				
R8=1	R6=1	R4=1	R2=1				

NOTE:

Default interface of this part is "80 MCU 16-bit bus interface 1" ([IM3:IM0] = 0001), and "HS", "VS", "DE", "DCLK", "SDA", "DB16", "DB17", already are connected to GND via 0 ohm resistor on FPC. Refer to below circuit.



5. ELECTRICAL CHARACTERISTICS

5.1 Absolute Maximum Ratings

Item	Symbol	Values		Unit	Remark
		Min	Max		
Power Supply for Pump	VCC	-0.3	4.5	V	
Operating temperature range	To	-20	70	Degree C	
Storage temperature range	Ts	-30	80	Degree C	
Logic input voltage range	VI	-0.3	VCC+0.3	V	
Logic input voltage range	VO	-0.3	VCC+0.3	V	

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics

5.2 DC Characteristics

5.2.2 DC Characteristics for Digital Circuit

Item	Symbol	Values			Unit	Conditions
		Min	Typ	Max		
Low Level Input Voltage	Vil	GND	-	0.3xVCC	v	
High Level Input Voltage	Vih	0.7xVCC	-	VCC	uA	
High Level Output Voltage	Voh	VCC-0.4	-	VCC	ohm	
Low Level Output Voltage	Vol	GND	-	GND+0.4	uA	
Power Supply	VCC	2.5	2.8	3.3	V	
Input Leakage Current	Iil			±1.0	uA	
Pull High/Low Resistor	Rp	-	100K	-	ohm	

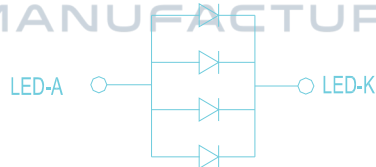
5.3 DC Backlight Unit

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Average Luminous Intensity	Iv		250		cd/m2	IF=60mA
Chromaticity Coordinates	X	0.234	0.284	0.334		IF=60mA
	Y	0.273	0.323	0.373		IF=60mA
Forward Voltage	VF		3.2	3.4	V	IF=60mA
Reverse Current	IR			50	μA	VR=5V, 1LED
Luminous Tolerance	IV-M	80			%	(MIN/MAX)×100
Power Dissipation	Pd	192			mW	
Peak Forward Current	Ifp	100			uA	
Reverse Voltage	VR	5			V	

B/L CIRCUIT DIAGRAM

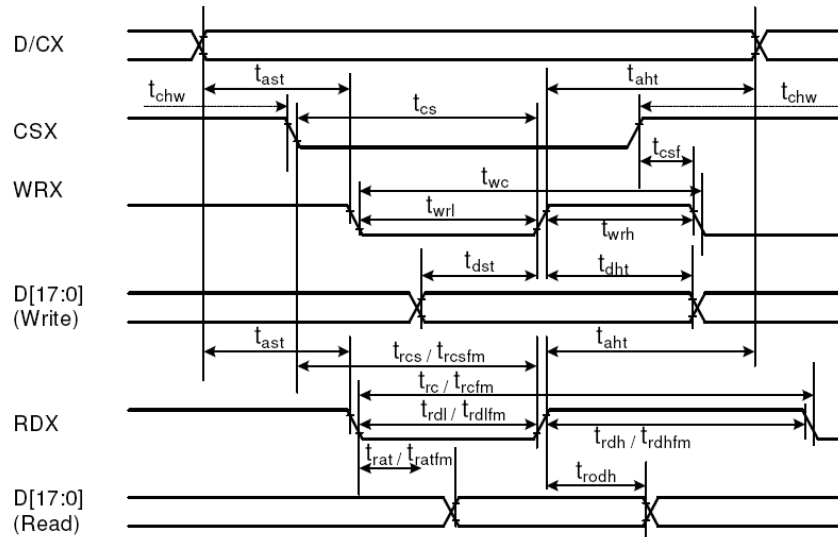
4 PCS WHITE LED; IF = 60mA, VF = 3.2V

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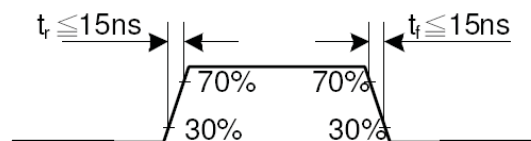
6. INPUT SIGNAL TIMING

6.1 Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080-I system)

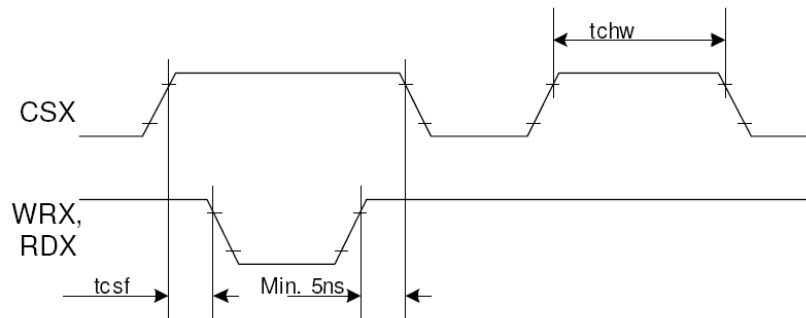


Signal	Symbol	Parameter	min	max	Unit	Description
DCX	t _{ast}	Address setup time	0	-	ns	
	t _{ah}	Address hold time (Write/Read)	0	-	ns	
CSX	t _{chw}	CSX "H" pulse width	0	-	ns	
	t _{cs}	Chip Select setup time (Write)	15	-	ns	
	t _{rcs}	Chip Select setup time (Read ID)	45	-	ns	
	t _{rcsfm}	Chip Select setup time (Read FM)	355	-	ns	
	t _{csf}	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	t _{wc}	Write cycle	66	-	ns	
	t _{wrh}	Write Control pulse H duration	15	-	ns	
	t _{wrl}	Write Control pulse L duration	15	-	ns	
RDX (FM)	t _{rcfm}	Read Cycle (FM)	450	-	ns	
	t _{rdhfm}	Read Control H duration (FM)	90	-	ns	
	t _{rdlfm}	Read Control L duration (FM)	355	-	ns	
RDX (ID)	t _{rc}	Read cycle (ID)	160	-	ns	
	t _{rdh}	Read Control pulse H duration	90	-	ns	
	t _{rdl}	Read Control pulse L duration	45	-	ns	
D[17:0], D[15:0], D[8:0], D[7:0]	t _{dst}	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	t _{dht}	Write data hold time	10	-	ns	
	t _{rat}	Read access time	-	40	ns	
	t _{ratfm}	Read access time	-	340	ns	
	t _{rod}	Read output disable time	20	80	ns	

Note: Ta = -30 to 70 °C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, VSS=0V

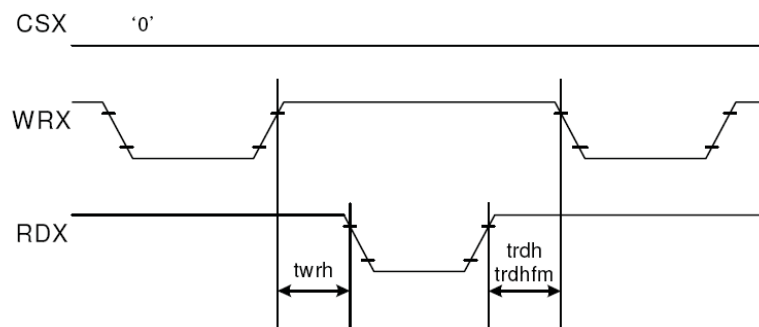


CSX timings :



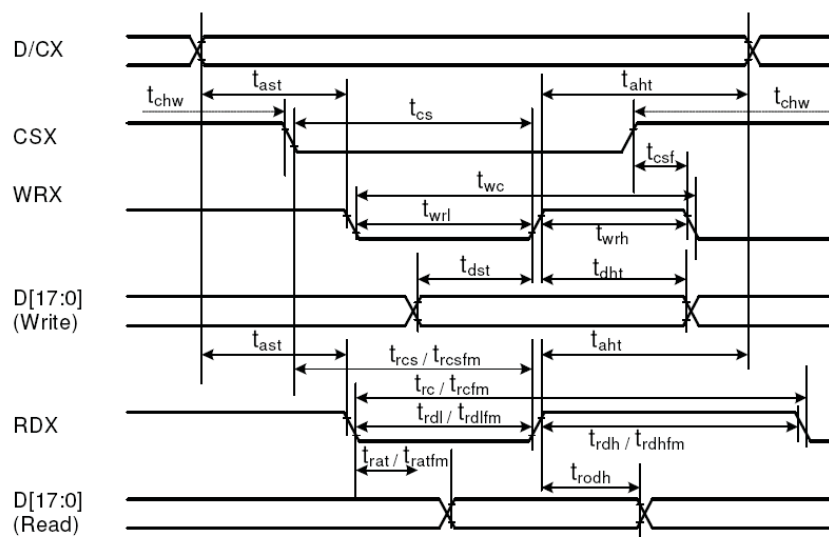
Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Write to read or read to write timings:



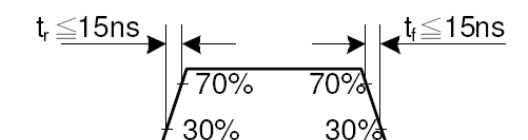
Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

6.2 Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080-II system)

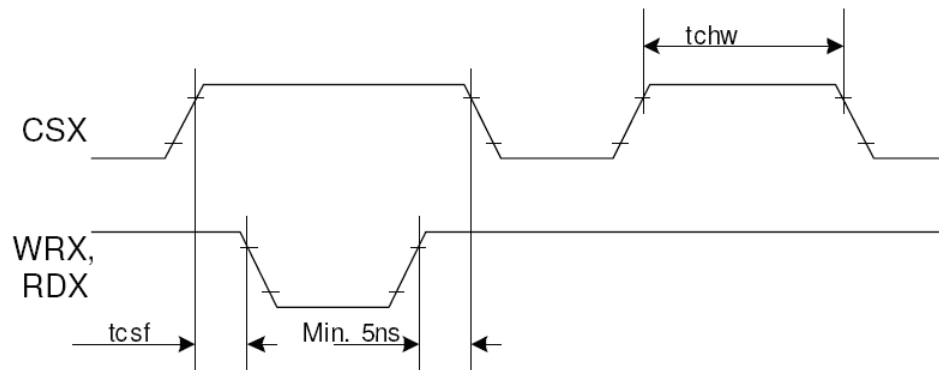


Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time (Write/Read)	0	-	ns	
CSX	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time (Write)	15	-	ns	
	trcs	Chip Select setup time (Read ID)	45	-	ns	
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX (FM)	trcfm	Read Cycle (FM)	450	-	ns	
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
D[17:0], D[17:10]&D[8:1], D[17:10], D[17:9]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

Note: $T_a = -30$ to 70 °C, $V_{DDI}=1.65V$ to $3.3V$, $V_{CI}=2.5V$ to $3.3V$, $V_{SS}=0V$.

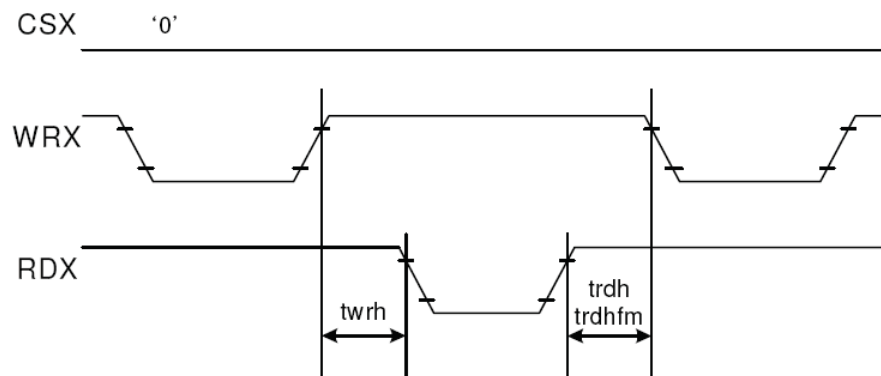


CSX timings :



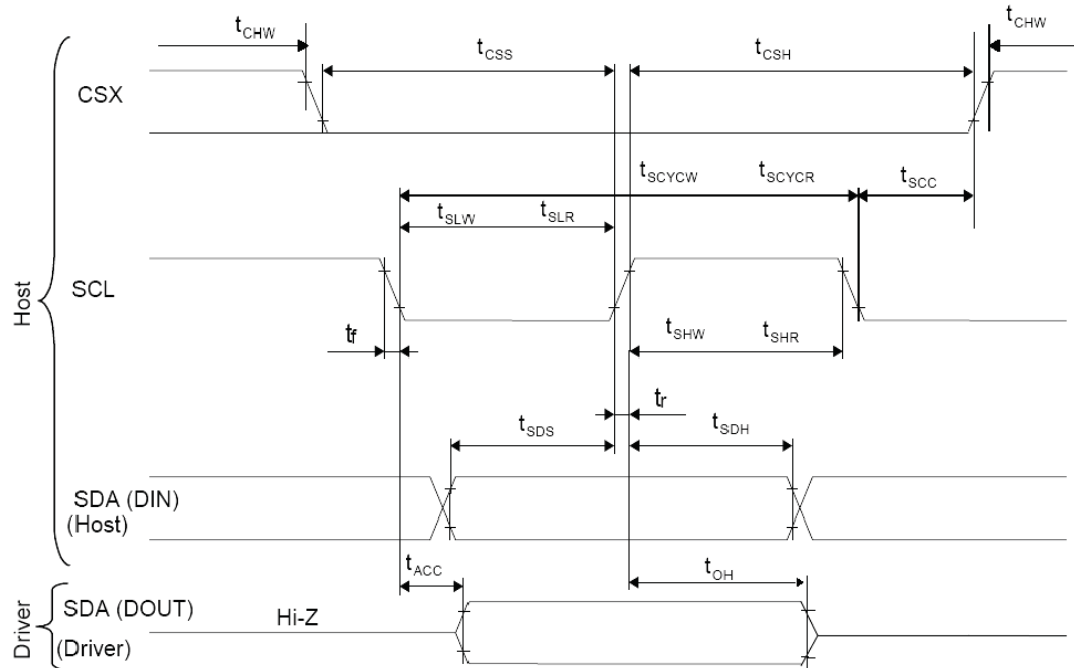
Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Write to read or read to write timings:



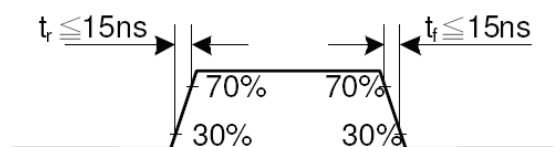
Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

6.3 Display Serial Interface Timing Characteristics (3-line SPI system)

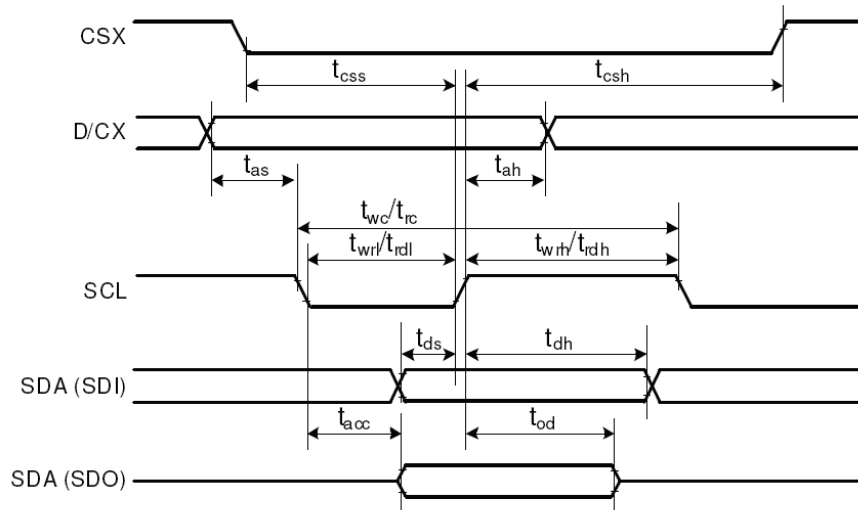


Signal	Symbol	Parameter	min	max	Unit	Description
SCL	tscycw	Serial Clock Cycle (Write)	100	-	ns	
	tshw	SCL "H" Pulse Width (Write)	40	-	ns	
	tslw	SCL "L" Pulse Width (Write)	40	-	ns	
	tscycr	Serial Clock Cycle (Read)	150	-	ns	
	tshr	SCL "H" Pulse Width (Read)	60	-	ns	
	tslr	SCL "L" Pulse Width (Read)	60	-	ns	
SDA / SDI (Input)	tsds	Data setup time (Write)	30	-	ns	
	tsdh	Data hold time (Write)	30	-	ns	
SDA / SDO (Output)	tacc	Access time (Read)	10	-	ns	
	toh	Output disable time (Read)	10	50	ns	
CSX	tsc	SCL-CSX	20	-	ns	
	tchw	CSX "H" Pulse Width	40	-	ns	
	tc	CSX-SCL Time	60	-	ns	
	tch		65	-	ns	

Note: $T_a = 25^\circ\text{C}$, $V_{DDI}=1.65\text{V to }3.3\text{V}$, $V_{CI}=2.5\text{V to }3.3\text{V}$, $AGND=VSS=0\text{V}$

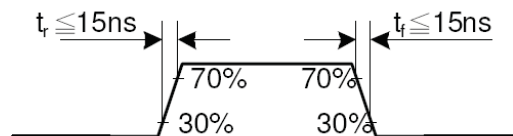


6.4 Display Serial Interface Timing Characteristics (4-line SPI system)

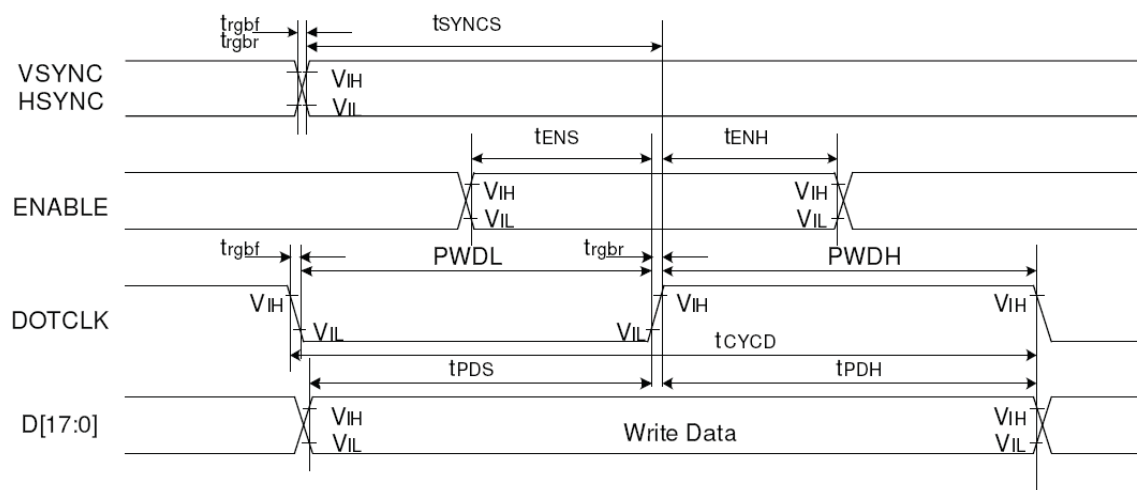


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	40	-	ns	
	tcsh	Chip select hold time (Read)	40	-	ns	
SCL	twc	Serial clock cycle (Write)	100	-	ns	
	twrh	SCL "H" pulse width (Write)	40	-	ns	
	twrl	SCL "L" pulse width (Write)	40	-	ns	
	trc	Serial clock cycle (Read)	150	-	ns	
	trdh	SCL "H" pulse width (Read)	60	-	ns	
	trdl	SCL "L" pulse width (Read)	60	-	ns	
D/CX	tas	D/CX setup time	10	-		
	tah	D/CX hold time (Write / Read)	10	-		
SDA / SDI (Input)	tds	Data setup time (Write)	30	-	ns	
	tdh	Data hold time (Write)	30	-	ns	
SDA / SDO (Output)	tacc	Access time (Read)	10	-	ns	For maximum CL=30pF
	tod	Output disable time (Read)	10	50	ns	For minimum CL=8pF

Note: $T_a = 25^\circ\text{C}$, $V_{DDI}=1.65\text{V to }3.3\text{V}$, $V_{CI}=2.5\text{V to }3.3\text{V}$, $AGND=VSS=0\text{V}$

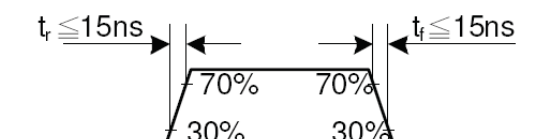


6.5 Parallel 18/16/6-bit RGB Interface Timing Characteristics



Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	18/16-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
DE	t_{ENS}	DE setup time	15	-	ns	
	t_{ENH}	DE hold time	15	-	ns	
D[17:0]	t_{POS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level pulse period	15	-	ns	
	PWDL	DOTCLK low-level pulse period	15	-	ns	
	t_{CYCD}	DOTCLK cycle time	100	-	ns	
	t_{trgb}, t_{trgbf}	DOTCLK, HSYNC, VSYNC rise/fall time	-	15	ns	
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	6-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
DE	t_{ENS}	DE setup time	15	-	ns	
	t_{ENH}	DE hold time	15	-	ns	
D[17:0]	t_{POS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level pulse period	15	-	ns	
	PWDL	DOTCLK low-level pulse period	15	-	ns	
	t_{CYCD}	DOTCLK cycle time	100	-	ns	
	t_{trgb}, t_{trgbf}	DOTCLK, HSYNC, VSYNC rise/fall time	-	15	ns	

Note: $T_a = -30$ to 70 °C, $V_{DDI}=1.65V$ to $3.3V$, $V_{CI}=2.5V$ to $3.3V$, $AGND=VSS=0V$



6.6 Controller Information

IC: ILI9341

7. OPTICAL CHARACTERISTICS

Item	Symbol	Condition	Specification			Unit	Remark
			Min.	Typ.	Max.		
Response time (By Quick)	Tr+Tf	$\theta = 0^\circ$	-	30	-	ms	Note 5
Contrast ratio	CR	$\theta = 0^\circ$	-	250	-		Note 2,6
Viewing angle	Top	$CR \geq 10$	-	45	-	deg.	Note 2,6,7
	Bottom	$CR \geq 10$	-	20	-		
	Left	$CR \geq 10$	-	45	-		
	Right	$CR \geq 10$	-	45	-		
CF Color chromaticity(CIE 1931)	Wx	$\theta = 0^\circ$	0.288	0.308	0.328		Note 3
	Wy		0.305	0.325	0.345		
	Rx		0.592	0.612	0.632		
	Ry		0.309	0.329	0.349		
	Gx		0.279	0.299	0.319		
	Gy		0.547	0.567	0.587		
	Bx		0.124	0.144	0.164		
	By		0.090	0.110	0.130		
NTSC				55%			Note 3
Cross talk	ct				2%		Note 10
Transmittance	Trans		4.5%	5.0%	-		Note 4

Note 1: Ambient temperature = 25°C.

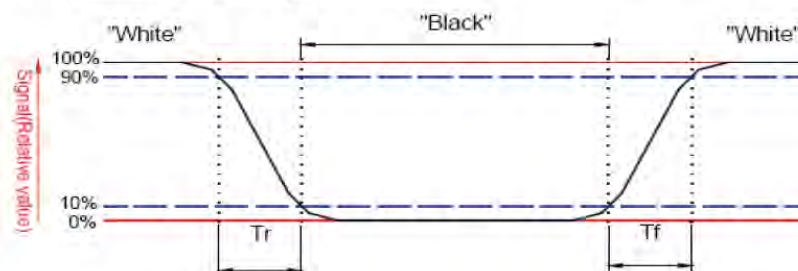
Note 2: To be measured with a viewing cone of 2° by Topcon luminance meter BM-5A.

Note 3: To be measured with Otsuta chromaticity meter LCF-2100M. CF only measure under C light simulation.

Note 4: CTC shipping status is cell without polarizer. Transmittance of Specification is cell with polarizer

Note 5: Definition of response time:

The output signals of TRD-100 are measured when the input signals are changed to "White" (falling time) and from "White" to "Black" (rising time), respectively. The interval is between the 10% and 90% of amplitudes. Refer to figure as below.

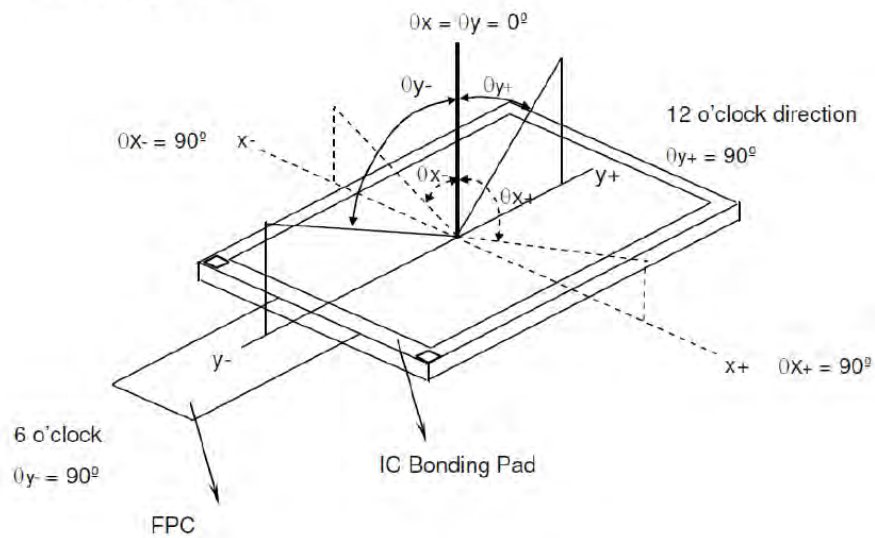


Note 6: Definition of contrast ratio:

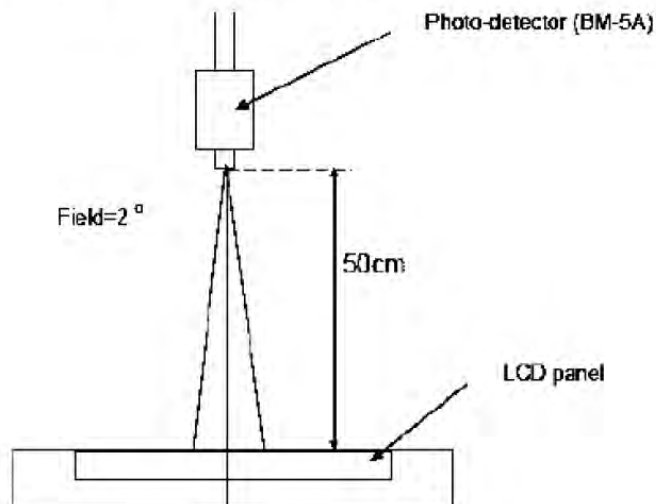
Contrast ratio is calculated by the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the "white" state}}{\text{Brightness on the "black" state}}$$

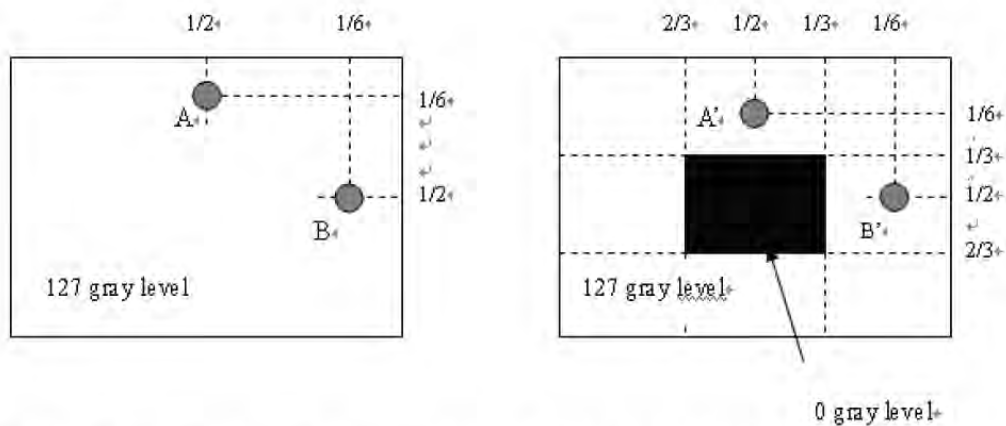
Note 7: Definition of viewing angle



Note 8: Optical characteristic measurement setup.



Note 9: Crosstalk.



$|LA - LA'| / LA \times 100\% = 2\% \text{ max.}$, LA and LA' are brightness at location A and A'
 $|LB - LB'| / LB \times 100\% = 2\% \text{ max.}$, LB and LB' are brightness at location B and B'

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