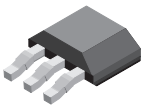
Highly Programmable Hall-Effect Switch

FEATURES AND BENEFITS

- Chopper stabilization for stable switchpoints throughout operating temperature range
- Externally programmable:
  - Operate point (through the VCC pin)
  - Output polarity
  - Output fall time for reduced EMI in automotive applications
- On-board voltage regulator for 3 to 24 V operation
- On-chip protection against:
  - Supply transients
  - Output short-circuits
  - Reverse battery condition

PACKAGES:

3-pin SIP
(suffix UA)



3-pin SIP
(suffix UA,
TS leadform)

3-pin SOT89
(suffix LT)

Not to scale

DESCRIPTION

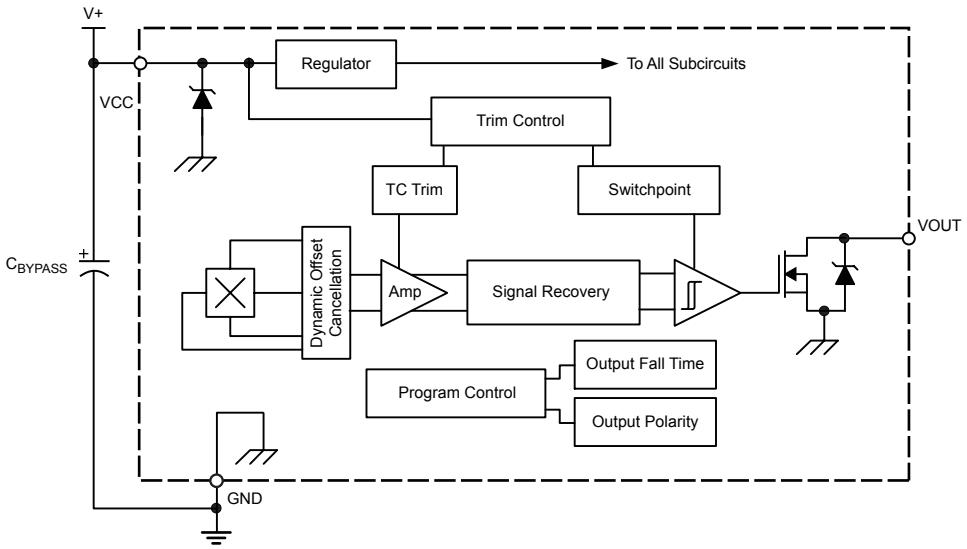
The A1128 is a field-programmable, unipolar Hall-effect switch designed for use in high-temperature applications. This device uses a chopper-stabilization technique to eliminate offset inherent in single-element devices.

The devices are externally programmable. A wide range of programmability is available on the magnetic operate point, B_{OP}, while the hysteresis remains fixed. This advanced feature allows optimization of the sensor IC switchpoint and can drastically reduce the effects of mechanical placement tolerances found in end-use production environments.

A proprietary dynamic offset cancellation technique, with an internal high-frequency clock, reduces the residual offset voltage, which is normally caused by device overmolding, temperature dependencies, and thermal stress. Having the Hall element and amplifier in a single chip minimizes many problems normally associated with low-level analog signals.

Two package styles provide a magnetically optimized package for most applications. Type LT is a miniature SOT89/TO-243AA surface mount package that is thermally enhanced with an exposed ground tab, and type UA is a three-lead ultramini SIP for through-hole mounting. The packages are lead (Pb) free, with 100% matte-tin-plated leadframes.

Functional Block Diagram



SELECTION GUIDE

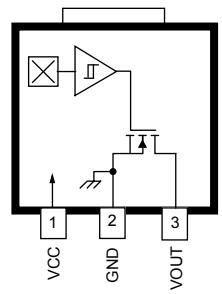
Part Number	Packing [1]	Package
A1128LLTTR-T [2]	7-in. reel, 1000 pieces/reel	3-pin SOT89/TO-243 surface mount
A1128LUA-T	Bulk, 500 pieces/bag	3-pin SIP through hole
A1128LUATS-T	13-in. reel, 4000 pieces/reel	3-pin SIP, TS leadform, surface mount

[1] Contact Allegro™ for additional packaging options.
[2] Last-Time Buy: This package variant has reached the end of its life cycle and will no longer be offered by Allegro. This product is considered obsolete and customer notification has been provided. All orders are accepted as final builds.
Date of status change: September 3, 2018. Recommended replacement: A1128LUATS-T.

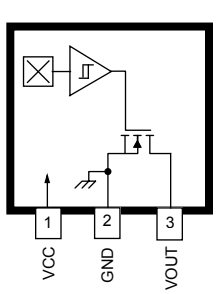
ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	V_{CC}		28	V
Reverse Supply Voltage	V_{RCC}		–18	V
Forward Output Voltage	V_{OUT}		26.5	V
Reverse Output Voltage	V_{ROUT}		–0.7	V
Output Sink Current	$I_{OUT(SINK)}$	VCC to VOUT	20	mA
Operating Ambient Temperature	T_A	L temperature range	–40 to 150	°C
Maximum Junction Temperature	T_J(max)		165	°C
Storage Temperature	T_{stg}		–65 to 170	°C

Pinout Diagrams



LT Package



UA Package

Terminal List Table

Number	Name	Function
1	VCC	Input power supply
2	GND	Ground
3	VOUT	Output signal

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OPERATING CHARACTERISTICS: Valid with T_A = –40°C to 150°C, C_{BYPASS} = 0.1 µF, V_{CC} = 12 V, unless otherwise noted

Characteristic	Symbol	Test Conditions		Min.	Typ.	Max.	Unit [1]
ELECTRICAL CHARACTERISTICS							
Supply Voltage	V_{CC}			3	12	24	V
Supply Current	I_{CC}	No load on VOUT		–	–	5.5	mA
Supply Zener Clamp Voltage	$V_{ZSUPPLY}$	T_A = 25°C, I_{CC} = I_{CC}(max) + 3 mA		28	–	–	V
Output Zener Clamp Voltage	$V_{ZOUTPUT}$	I_{OUT} = 3 mA		28	–	–	V
Reverse Battery Zener	V_{RCC}			–	–	–18	V
Reverse Battery Current	I_{RCC}	V_{CC} = –18 V		–5	–	–	mA
Chopping Frequency	f_C			–	400	–	kHz
POWER-ON CHARACTERISTICS							
Power-On Time	t_{PO}	T_A = 25°C; C_{LOAD} (PROBE) = 10 pF		–	–	30	µs
Power-On State [2]	POS	POL = 0; B < B_{RP}, t > t_{on}		–	High	–	–
		POL = 1; B < B_{RP} , t > t_{on}		–	Low	–	–
OUTPUT STAGE CHARACTERISTICS							
Output Saturation Voltage	$V_{OUT(sat)}$	I_{OUT} = 20 mA		–	175	400	mV
Output Leakage Current	I_{OFF}	V_{OUT} = 24 V; Switch state = Off		–	–	10	µA
Output Current Limit	$I_{OUT(lim)}$	Short-Circuit Protection, Output = On		30	–	90	mA
Output Rise Time [3][4]	t_r	V_{CC} = 12 V, R_{LOAD} = 820 Ω, C_{LOAD} = 10 pF		–	–	2	µs
		V_{CC} = 12 V, R_{LOAD} = 2 kΩ, C_{LOAD} = 4.7 nF		–	21	–	µs
Output Fall Time [4]	t_f	FALL = 0, V_{CC} = 12 V, R_{LOAD} = 820 Ω, C_{LOAD} = 10 pF		–	–	2	µs
		FALL = 1, V_{CC} = 12 V, R_{LOAD} = 2 kΩ, C_{LOAD} = 4.7 nF		–	6.5	–	µs
		FALL = 2, V_{CC} = 12 V, R_{LOAD} = 2 kΩ, C_{LOAD} = 4.7 nF		–	10	–	µs
		FALL = 3, V_{CC} = 12 V, R_{LOAD} = 2 kΩ, C_{LOAD} = 4.7 nF		–	12.5	–	µs
Output Polarity [2]	POL	POL = 0	B > B_{OP}	–	Low	–	–
			B < B_{RP}	–	High	–	–
		POL = 1	B > B_{OP}	–	High	–	–
			B < B_{RP}	–	Low	–	–

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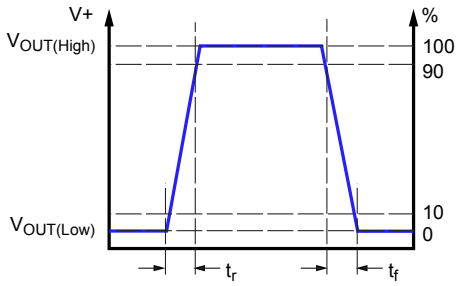

Rise Time and Fall Time Definitions

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OPERATING CHARACTERISTICS (continued): Valid with T_A = –40°C to 150°C, C_{BYPASS} = 0.1 µF, V_{CC} = 12 V, unless otherwise noted

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit [1]
MAGNETIC CHARACTERISTICS (valid V_{CC} = 3 to 24 V, $T_J \le T_J$(max), unless otherwise noted)						
Pre-Programming B_{OP} Target	B_{OPinit}	T_A = 25°C, BOPPOL = 0	–	–35	–	G
		T_A = 25°C, BOPPOL = 1	–	35	–	G
Switchpoint Thermal Drift [5]	ΔB_{OP}	LT package, B_{OP} = ±650 G	–0.14	–0.03	0.08	%/°C
		UA package, B_{OP} = ±650 G	–0.08	0.00	0.08	%/°C
Hysteresis	B_{hys}	$B_{OP} - B_{RP}$	5	15	30	G
PROGRAMMING CHARACTERISTICS						
Switchpoint Magnitude Selection Bits	Bit_{BOPSEL}		–	8	–	bit
Switchpoint Polarity Bits	Bit_{BOPPOL}		–	1	–	bit
Output Polarity Bits	Bit_{POL}		–	1	–	bit
Fall Time Bits	Bit_{FALL}		–	2	–	bit
Device Lock Bits	Bit_{LOCK}		–	1	–	bit
Programmable B_{OP} Range	B_{OP}	T_A = 25°C, BOPPOL = 1 (minimum at BOPSEL = 255, maximum at BOPSEL = 0)	–650	–	20	G
		T_A = 25°C, BOPPOL = 0 (minimum at BOPSEL = 0, maximum at BOPSEL = 255)	–20	–	650	G
B_{OP} Step Size	Res_{BOP}	Bit = LSB of BOPSEL	–	4	8	G

[1] 1 G (gauss) = 0.1 mT (millitesla).
[2] Output state when device configured as shown in figure 1.
[3] Output Rise Time is governed by external circuit tied to VOUT.
[4] Measured from 10% to 90% steady state output.
[5] Internal trimming utilized to minimize switchpoint drift across the operating temperature range.

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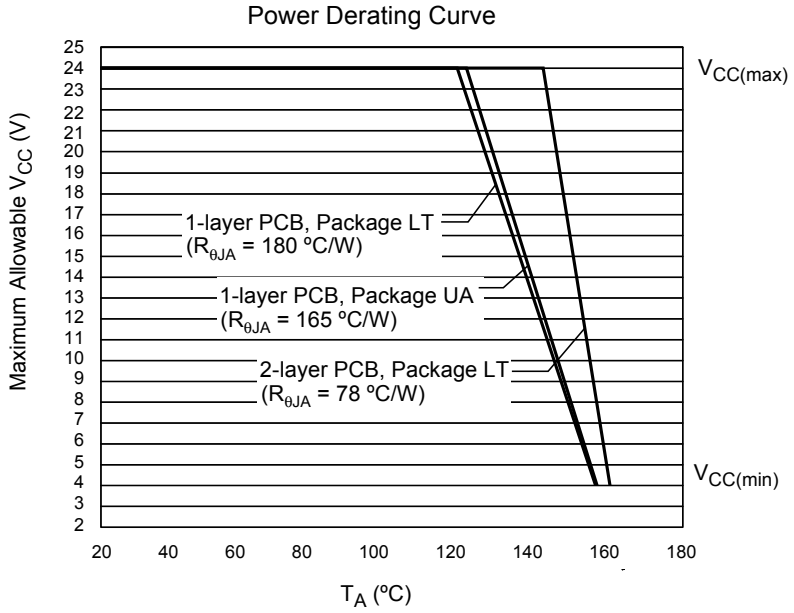
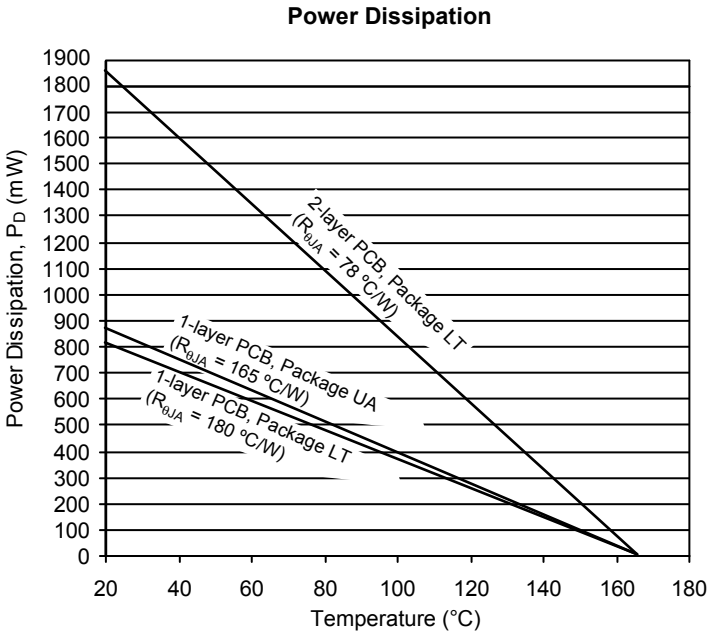
THERMAL CHARACTERISTICS: May require derating at maximum conditions; see Application Information

Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	Package UA, 1-layer PCB with copper limited to solder pads	165	°C/W
		Package LT, 1-layer PCB with copper limited to solder pads	180	°C/W
		Package LT, 2-layer PCB with 0.94 in^2 copper each side	78	°C/W

*Additional thermal information available on Allegro website.





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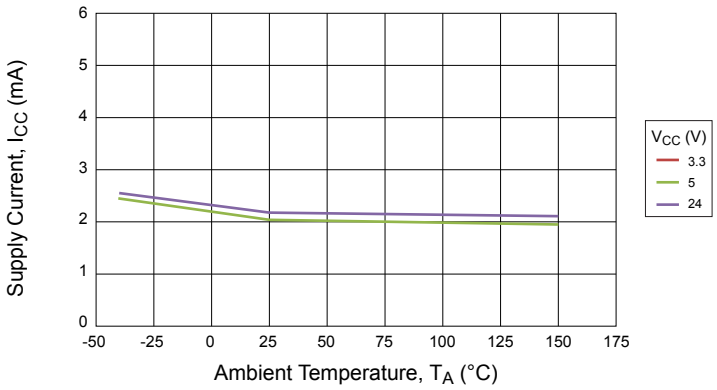
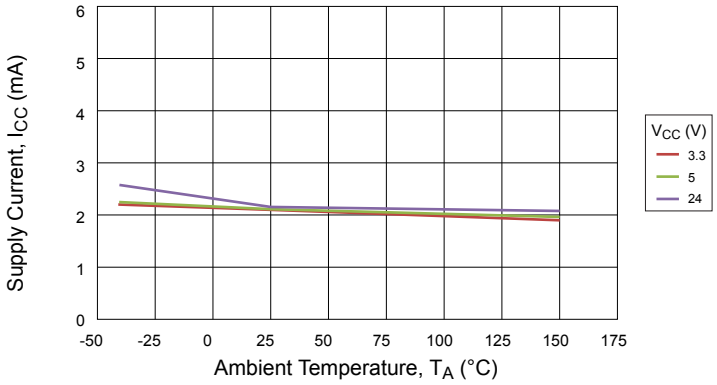
CHARACTERISTIC PERFORMANCE

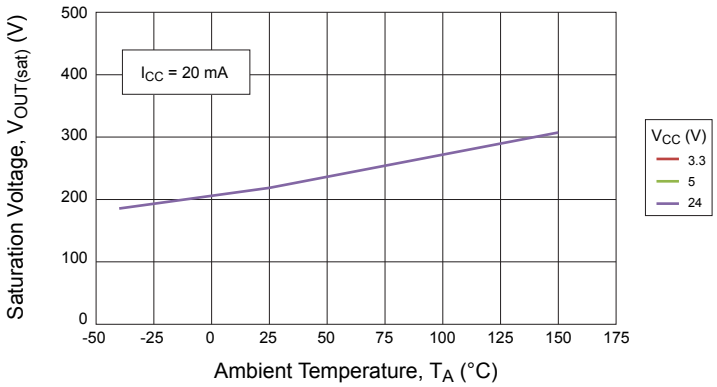
Supply Current (On) versus Ambient Temperature



Supply Current (Off) versus Ambient Temperature



Saturation Voltage versus Ambient Temperature



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APPLICATION INFORMATION

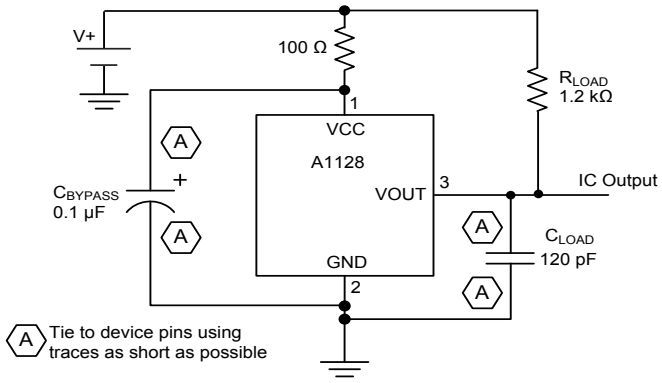

Figure 1. Typical Application Circuit

CHOPPER STABILIZATION TECHNIQUE

When using Hall-effect technology, a limiting factor for switch point accuracy is the small signal voltage developed across the Hall element. This voltage is disproportionally small relative to the offset that can be produced at the output of the Hall sensor IC. This makes it difficult to process the signal while maintaining an accurate, reliable output over the specified operating temperature and voltage ranges. Chopper stabilization is a unique approach used to minimize Hall offset on the chip. Allegro employs a technique to remove key sources of the output drift induced by thermal and mechanical stresses. This offset reduction technique is based on a signal modulation-demodulation process. The undesired offset signal is separated from the magnetic field-induced signal in the frequency domain, through modulation. The subsequent demodulation acts as a modulation process for the offset, causing the magnetic field-induced signal to recover its original spectrum at base band, while the DC offset becomes a high-frequency signal. The magnetic-sourced signal then can pass through a low-pass filter, while the modulated DC offset is suppressed. In addition to the removal of the thermal and stress related offset, this novel technique also reduces the amount of thermal noise in the Hall sensor IC while completely removing the modulated residue resulting from the chopper operation. The chopper stabilization technique uses a high frequency sampling clock. For demodulation process, a sample and hold technique is used. This high-frequency operation allows a greater sampling rate, which results in higher accuracy and faster signal-processing capability. This approach desensitizes the chip to the effects of thermal and mechanical stresses, and produces devices that have extremely stable quiescent Hall output voltages and precise recoverability after temperature cycling. This technique is made possible through the use of a BiCMOS process, which allows the use of low-offset, low-noise amplifiers in combination with high-density logic integration and sample-and-hold circuits.

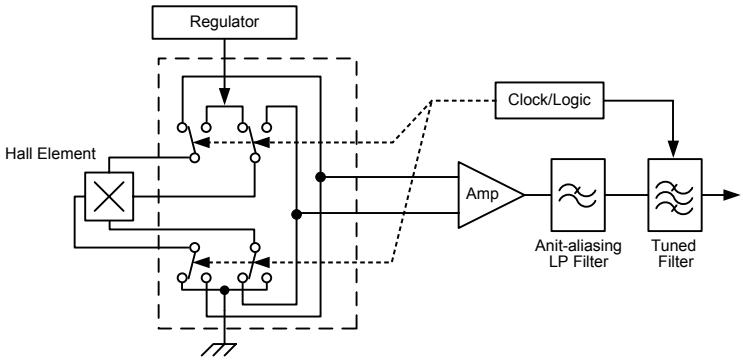

Figure 2. Concept of Chopper Stabilization Technique

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FUNCTIONAL DESCRIPTION

When the Output Polarity bit is not set (POL = 0), the A1128 output switches on after the magnetic field at the Hall sensor IC exceeds the operate point threshold, B_{OP}. When the magnetic field is reduced to below the release point threshold, B_{RP}, the device output switches off. The difference between the magnetic operate and release points is called the hysteresis of the device, B_{HYS}. In the alternative case, in which the Output Polarity bit is set (POL = 1), the A1128 output switches off when the magnetic field at the Hall sensor IC exceeds the operate point threshold, B_{OP}. When the magnetic field is reduced to below the release point threshold, B_{RP}, the device output switches on.

Note that for the Pre-Programming B_{OP} Target, B_{OPinit}, when BOPPOL = 0 although the operating range is 0 to B+, the initial B_{OPinit} is actually negative, and likewise, when BOPPOL = 1, although the operating range 0 to B– , the initial B_{OPinit} is actually positive.

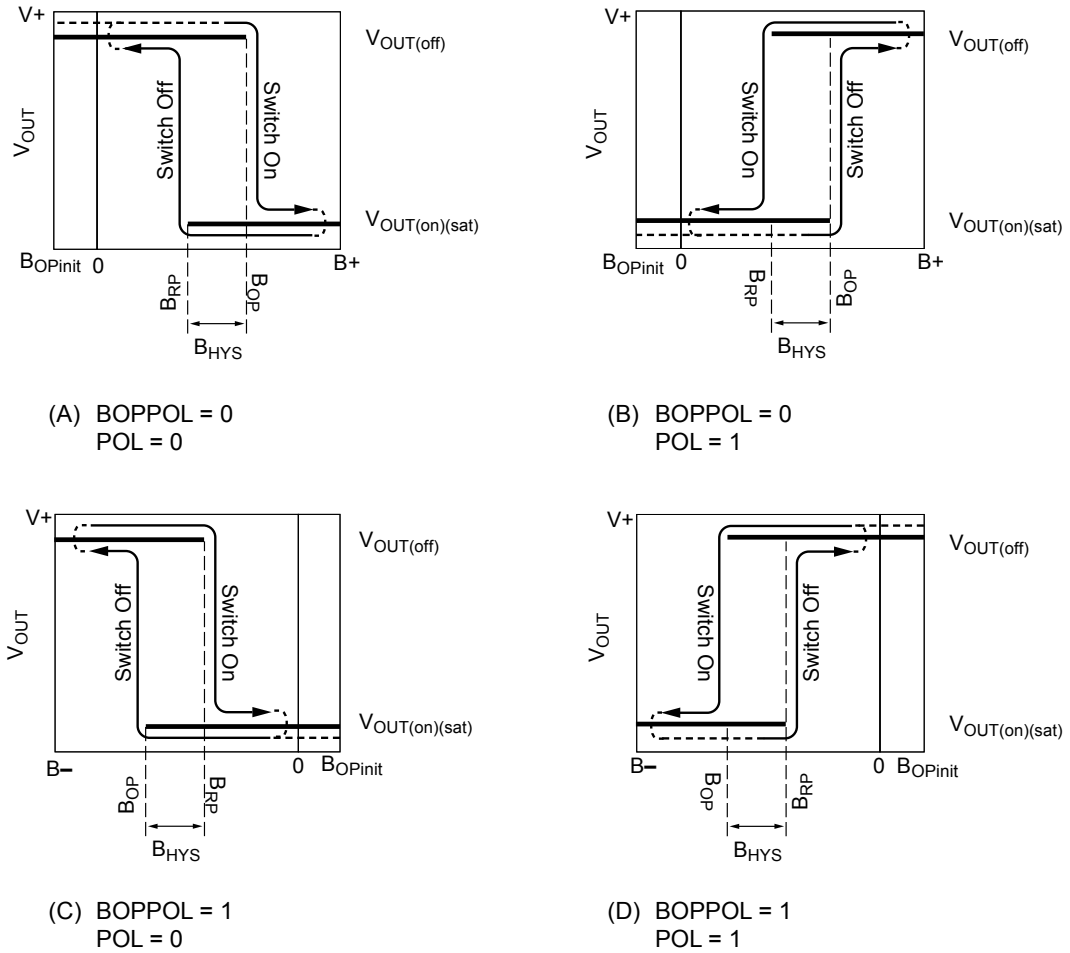

Figure 3. Hysteresis Diagrams. These plots demonstrate the behavior of the A1128 with the applied magnetic field impinging on the branded face of the device case (refer to Package Outline Drawings section). On the horizontal axis, the B+ direction indicates increasing south or decreasing north magnetic flux density, and the B– direction indicates increasing north or decreasing south magnetic flux density.

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PROGRAMMING GUIDELINES

OVERVIEW

Programming is accomplished by sending a series of input voltage pulses serially through the VCC (supply) pin of the device. A unique combination of different voltage level pulses controls the internal programming logic of the device to select a desired programmable parameter and change its value. There are three voltage levels that must be taken into account when programming. These levels are referred to as *high* (V_{PH}), *mid* (V_{PM}), and *low* (V_{PL}).

The A1128 features three programmable modes, Try mode, Blow mode, and Read mode:

- In Try mode, programmable parameter values are set and measured simultaneously. A parameter value is stored temporarily, and reset after cycling the supply voltage.
- In Blow mode, the value of a programmable parameter may be permanently set by blowing solid-state fuses internal to the device. Device locking is also accomplished in this mode.
- In Read mode, each bit may be verified as blown or not blown.

The programming sequence is designed to help prevent the device from being programmed accidentally; for example, as a result of noise on the supply line. Note that, for all programming modes, no parameter programming registers are accessible after the device-level LOCK bit is set. The only function that remains accessible is the overall Fuse Checking feature.

Although any programmable variable power supply can be used to generate the pulse waveforms, for design evaluations, Allegro highly recommends using the Allegro Sensor IC Evaluation Kit, available on the Allegro website On-line Store. The manual for that kit is available for download free of charge, and provides additional information on programming these devices. (Note: This kit is not recommended for production purposes.)

DEFINITION OF TERMS

Register The section of the programming logic that controls the choice of programmable modes and parameters.

Bit Field The internal fuses unique to each register, represented as a binary number. Changing the bit field settings of a particular register causes its programmable parameter to change, based on the internal programming logic.

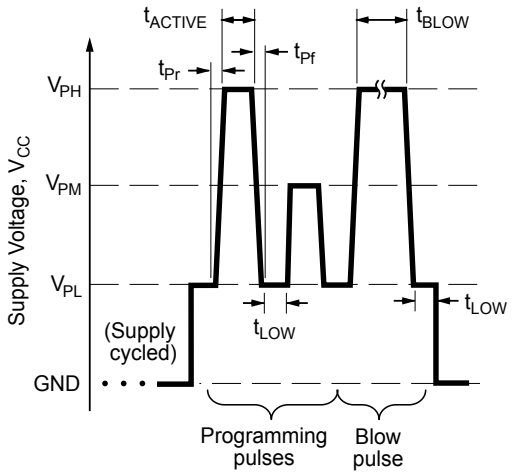

Figure 4. Programming pulse definitions (see table 1)

Table 1. Programming Pulse Requirements, Protocol at T_A = 25°C

Characteristics	Symbol	Notes	Min.	Typ.	Max.	Unit
Programming Voltage	V_{PL}	Measured at the VCC pin	4.5	5	5.5	V
	V_{PM}		12.5	–	14	V
	V_{PH}		21	–	27	V
Programming Current	I_{PP}	V_{CC} = 5 → 26 V, C_{BLOW} = 0.1 µF (min); minimum supply current required to ensure proper fuse blowing.	175	–	–	mA
Pulse Width	t_{LOW}	Duration of V_{PL} separating pulses at V_{PM} or V_{PH}	20	–	–	µs
	t_{ACTIVE}	Duration of pulses at V_{PM} or V_{PH} for key/code selection	20	–	–	µs
	t_{BLOW}	Duration of pulse at V_{PH} for fuse blowing	90	100	–	µs
Pulse Rise Time	t_{Pr}	V_{PL} to V_{PM} or V_{PL} to V_{PH}	5	–	100	µs
Pulse Fall Time	t_{Pf}	V_{PM} to V_{PL} or V_{PH} to V_{PL}	5	–	100	µs
Blow Pulse Slew Rate	SR_{BLOW}		0.375	–	–	V/µs

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Key A series of voltage pulses used to select a register or mode.

Code The number used to identify the combination of fuses activated in a bit field, expressed as the decimal equivalent of the binary value. The LSB of a bit field is denoted as code 1, or bit 0.

Addressing Increasing the bit field code of a selected register by serially applying a pulse train through the VCC pin of the device. Each parameter can be measured during the addressing process, but the internal fuses must be blown before the programming code (and parameter value) becomes permanent.

Fuse Blowing Applying a high voltage pulse of sufficient duration to permanently set an addressed bit by blowing a fuse internal to the device. Once a bit (fuse) has been blown, it cannot be reset.

Blow Pulse A high voltage pulse of sufficient duration to blow the addressed fuse.

Cycling the Supply Powering-down, and then powering-up the supply voltage. Cycling the supply is used to clear the programming settings in Try mode.

Programming Procedure

Programming involves selection of a register and mode, and then setting values for parameters in the register for evaluation or fuse blowing. Figure 8 provides an overview state diagram.

REGISTER SELECTION

Each programmable parameter can be accessed through a specific register. To select a register, from the Initial state, a sequence of voltage pulses consisting of one V_{PH} pulse, one V_{PM} pulse, and then a unique combination of V_{PH} and V_{PM} pulses, is applied serially to the VCC pin (with no V_{CC} supply interruptions). This sequence of pulses is called the *key*, and uniquely identifies each register. An example register selection key is shown in figure 5.

To simplify Try mode, the A1128 provides a set of four virtual registers, one for each combination of: B_{OP} selection (BOPSEL), B_{OP} polarity (BOPPOL), and a facility for transiting B_{OP} magnitude values in an increasing or decreasing sequence. These registers also allow wrapping back to the beginning of the register after transiting the register.

MODE SELECTION

The same physical registers are used for all programming modes. To distinguish Blow mode and Read mode, when selecting the registers an additional pulse sequence consisting of eleven V_{PM} pulses followed by one V_{PH} pulse is added to the key. The combined register and mode keys are shown in table 3.

TRY MODE

In Try mode, the bit field addressing is accomplished by applying a series of V_{PM} pulses to the VCC pin of the device, as shown in figure 6. Each pulse increases the total bit field value of the selected parameter, increasing by one on the falling edge of each additional V_{PM} pulse. When addressing a bit field in Try mode, the number of V_{PM} pulses is represented by a decimal number called a *code*. Addressing activates the corresponding fuse locations in the given bit field by increasing the binary value of an internal DAC, up to the maximum possible code. As the value of the bit field code increases, the value of the programmable parameter changes. Measurements can be taken after each V_{PM} pulse to determine if the desired result for the programmable parameter has been reached. Cycling the supply voltage resets all the locations in the bit field that have un-blown fuses to their initial states. This should also be done before selection of a different register in Try mode.

When addressing a parameter in Try mode, the bit field address (code) defaults to the value 1, on the falling edge of the final register selection key V_{PH} pulse (see figure 6). A complete example is shown figure 10. Note that, in the four B_{OP} selection virtual registers, after the maximum code is entered, the next VPM pulse wraps back to the beginning of the register, and selects code 0.

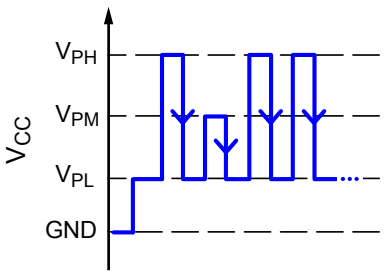

Figure 5. Example of Try mode register selection pulses, for the B_{OP} Negative Trim, Up-Counting register.

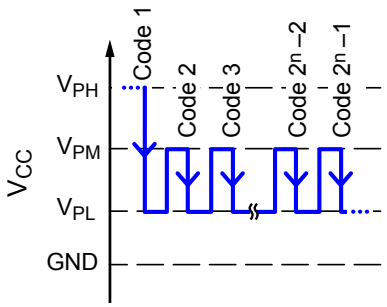

Figure 6. Try mode bit field addressing pulses.

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The four B_{OP} selecting virtual registers allow the programmer to adjust the B_{OP} parameter for use in north or south magnetic fields. In addition, values can be traversed from low to high, or from high to low. Figure 12 shows the relationship between the B_{OP} parameter and the different Try mode registers. Note: See the Output Polarity section for information about setting the POL bit before using Try mode.

The FALL and POL fields are in the same register (FALL is bits 1:0, and POL is bit 2). Therefore, in Try mode both can be programmed simultaneously by adding the codes for the two parameters, and send the sum as the code. For example, sending code 7 (111) sets FALL to 3 (x11) and sets POL (1xx).

BLOW MODE

After the required code is determined for a given parameter, its value can be set permanently by blowing individual fuses in the appropriate register bit field. Blowing is accomplished by selecting the register and mode selection key, followed by the appropriate bit field address, and ending the sequence with a Blow pulse. The Blow mode selection key is a sequence of eleven V_{PM} pulses followed by one V_{PH} pulse. The Blow pulse consists of a V_{PH} pulse of sufficient duration, t_{BLOW}, to permanently set an addressed bit by blowing a fuse internal to the device. The device power must be cycled after each individual fuse is blown.

Due to power requirements, a 0.1 µF blowing capacitor, C_{BLOW}, must be mounted between the VCC pin and the GND pin during programming, to ensure enough current is available to blow fuses. If programming in the application, C_{BYPASS} (see figure 1) can serve the same purpose.

The fuse for each bit in the bit field must be blown individually. The A1128 built-in circuitry allows only one fuse at a time to be blown. During Blow mode, the bit field can be considered a "one-hot" shift register. Table 2 illustrates how to relate the number of V_{PM} pulses to the binary and decimal value for Blow mode bit field addressing. It should be noted that the simple relationship between the number of V_{PM} pulses and the required code is:

$$2^n = \text{Code},$$

where n is the number of V_{PM} pulses, and the bit field has an initial state of decimal code 1 (binary 00000001). To correctly blow the required fuses, the code representing the required parameter value must be translated to a binary number. For example, as shown in figure 7, decimal code 5 is equivalent to the binary number 101. Therefore bit 2 must be addressed and blown, the device power supply cycled, and then bit 0 must be addressed and blown. The order of blowing bits, however, is not important. Blowing bit 0 first, and then bit 2 is acceptable. A complete example is shown in figure 11.

Note: After blowing, the programming is not reversible, even after cycling the supply power. Although a register bit field fuse cannot be reset after it is blown, additional bits within the same register can be blown at any time until the device is locked. For example, if bit 1 (binary 10) has been blown, it is still possible to blow bit 0. The end result would be binary 11 (decimal code 3).

LOCKING THE DEVICE

After the required code for each parameter is programmed, the device can be locked to prevent further programming of any parameters. To do so, perform the following steps:

1. Ensure that the C_{BLOW} capacitor is mounted.
2. Select the Output/Lock Bit register key.
3. Select Blow mode selection key.
4. Address bit 4 (10000) by sending four V_{PM} pulses.
5. Send one Blow pulse, at I_{PP} and SR_{BLOW}, and sustain it for t_{BLOW}.
6. Delay for a t_{LOW} interval, then power-down.
7. Optionally check all fuses.

Table 2. Blow Mode Bit Field Addressing

Quantity of V_{PM} Pulses	Binary Register Bit Field	Decimal Equivalent Code
0	0000 0001	1
1	0000 0010	2
2	0000 0100	4
3	0000 1000	8
4	0001 0000	16
5	0010 0000	32
6	0100 0000	64
7	1000 0000	128

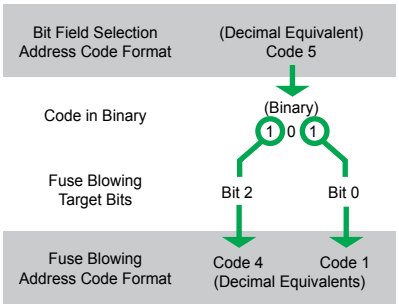

Figure 7. Example of code 5 broken into its binary components.

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Table 3. Programming Logic Table

Register Name [Selection Key]	Bit Field Address (Code)		Notes
	Binary (MSB→LSB)	Decimal Equivalent	
TRY MODE REGISTER SELECTIONS			
B_{OP} Positive, Trim Up-Counting [$2 \times V_{PH}$]	0000 0000	0	Increase B_{OP} (South field). Code 1 automatically selected when register entered, wraps back to code 0.
	1111 1111	255	B_{OP} selection is at maximum value.
B_{OP} Negative, Trim Up-Counting [$V_{PH} \rightarrow V_{PM} \rightarrow 2 \times V_{PH}$]	0000 0000	0	Increase B_{OP} (North field). Code 1 automatically selected when register entered, wraps back to code 0.
	1111 1111	255	B_{OP} selection is at maximum value.
B_{OP} Positive, Trim Down-Counting [$2 \times V_{PH} \rightarrow 4 \times V_{PM} \rightarrow V_{PH}$]	1111 1111	0	Decrease B_{OP} (South field). Code 1 automatically selected when register entered, wraps back to code 0. Code is automatically inverted (code 1 selects B_{OP} selection maximum value minus 1.)
	0000 0000	255	B_{OP} selection is at minimum value.
B_{OP} Negative, Trim Down-Counting [$V_{PH} \rightarrow V_{PM} \rightarrow 2 \times V_{PH} \rightarrow 4 \times V_{PM} \rightarrow V_{PH}$]	1111 1111	0	Decrease B_{OP} (North field). Code 1 automatically selected when register entered, wraps back to code 0. Code is automatically inverted (code 1 selects B_{OP} selection maximum value minus 1.)
	0000 0000	255	B_{OP} selection is at minimum value.
Output / Fuse Checking [$V_{PH} \rightarrow 3 \times V_{PM} \rightarrow V_{PH}$]	x01	1	Output Fall Time (FALL). Code 1 automatically selected. Minimum value.
	x11	3	Output Fall Time (FALL) selection is at maximum value.
	0xx	0	Output Polarity Bit (POL). Default, no fuse blowing required. POL = 0, see figures 3A and 3C.
	1xx	4	Output Polarity Bit (POL). Code 1 automatically selected. POL = 1, see figures 3B and 3D. Code references a single bit only.
	1000	8	Fuse Threshold Low Register. Code 1 automatically selected when register entered. Checks un-blown fuses. Code references a single bit only.
	1001	9	Fuse Threshold High Register. Checks blown fuses.
BLOW OR READ MODE REGISTER SELECTIONS			
B_{OP} Selection (BOPSEL) [$2 \times V_{PH} \rightarrow 11 \times V_{PM} \rightarrow V_{PH}$]	0000 0000	0	B_{OP} magnitude selection. Default, no fuse blowing required. Minimum value, corresponding to B_{OP}(min).
	1111 1111	255	B_{OP} magnitude selection. Maximum value, corresponding to B_{OP}(max).
B_{OP} Polarity (BOPPOL) [$V_{PH} \rightarrow V_{PM} \rightarrow V_{PH} \rightarrow 11 \times V_{PM} \rightarrow V_{PH}$]	0	0	South field polarity. Default, no fuse blowing required.
	1	1	North field polarity. Code 1 (bit 0) automatically selected.
Output / Lock Bit [$V_{PH} \rightarrow 3 \times V_{PM} \rightarrow V_{PH} \rightarrow 11 \times V_{PM} \rightarrow V_{PH}$]	00	0	Output Fall Time (FALL). Default, no fuse blowing required.
	11	3	Output Fall Time (FALL) selection is at maximum value. Code 1 (bit 0) automatically selected.
	000	0	Output Polarity Bit (POL). Default, no fuse blowing required. POL = 0, see figures 3A and 3C.
	100	4	Output Polarity Bit (POL). Code 1 (bit 0) automatically selected. Code refers to bit 2 only. POL = 1, see figures 3B and 3D.
	10000	16	Lock bit (LOCK). Locks access to all registers with exception of Fuse Threshold registers. Code 1 (bit 0) automatically selected in Blow mode. Code refers to bit 5 only.
	0 to 111 1111	–	Read mode bit values. Sequentially selects each bit in selected Blow mode register for reading bit status as blown or not blown. Code 1 (bit 0) automatically selected. Monitor VOUT after each pulse.

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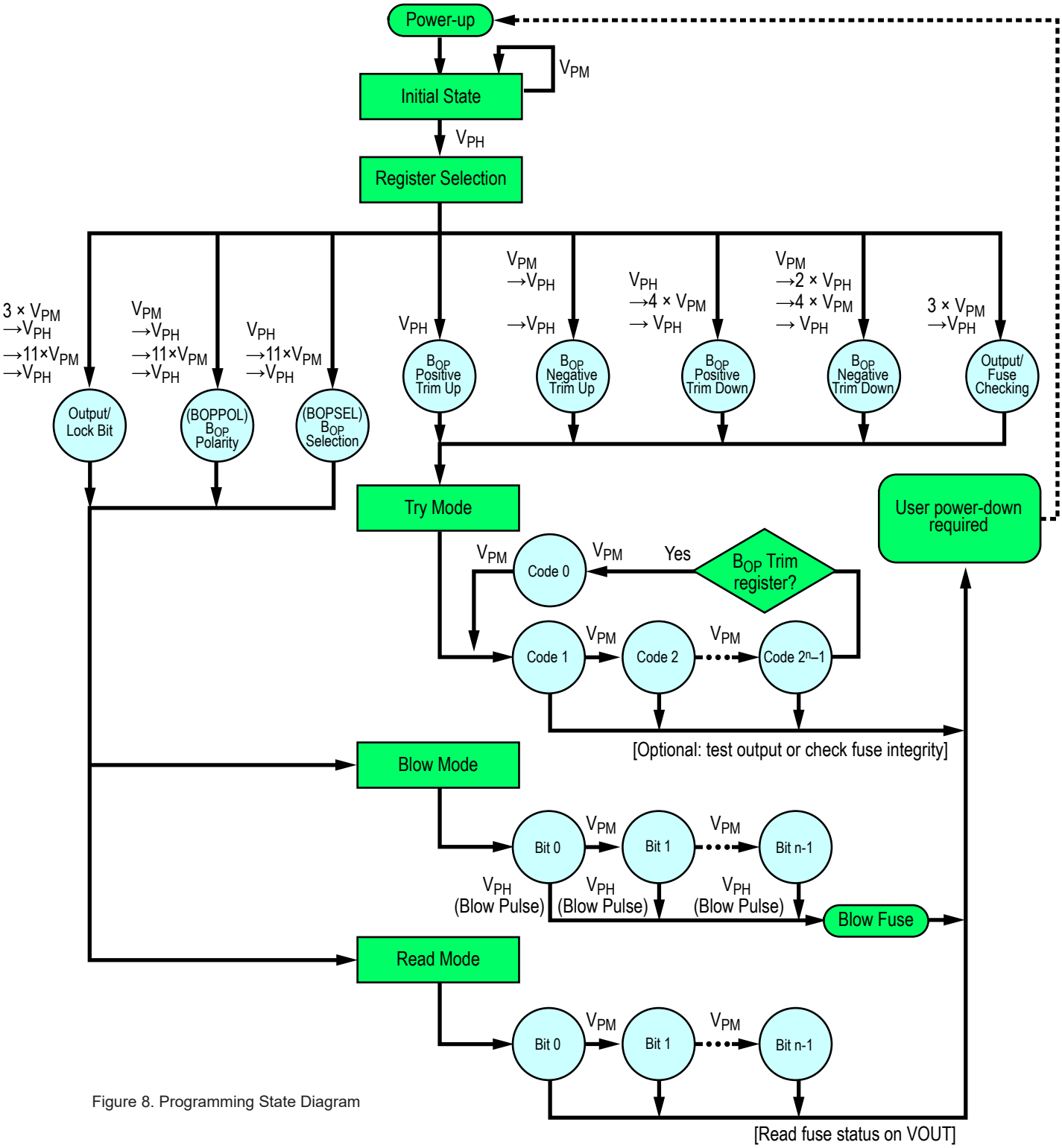

Figure 8. Programming State Diagram

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FUSE CHECKING

Incorporated in the A1128 is circuitry to simultaneously check the integrity of the fuse bits. The fuse checking feature is enabled by using the Fuse Checking registers, and while in Try mode, applying the codes shown in table 3. The register is only valid in Try mode and is available before or after the programming LOCK bit is set.

Selecting the Fuse Threshold High register checks that all blown fuses are properly blown. Selecting the Fuse Threshold Low register checks all un-blown fuses are properly intact. The supply current, I_{CC}, increases by 250 µA if a marginal fuse is detected. If all fuses are correctly blown or fully intact, there will be no change in supply current.

OUTPUT POLARITY

When selecting the B_{OP} registers in Try mode, the output polarity is determined by the value of the Output Polarity bit (POL). The default value is POL = 0 (fuse un-blown). For applications that require the output states defined by POL = 1 (see Operating Characteristics table), it is recommended to first permanently blow the POL bit by selecting the Output / Lock bit register, and code 4. The output is then defined by POL = 1 when selecting the B_{OP} Try mode registers. See table 3 for parameter details.

ADDITIONAL GUIDELINES

The additional guidelines in this section should be followed to ensure the proper behavior of these devices:

- The power supply used for programming must be capable of delivering at least V_{PH} and 175 mA.
- Be careful to observe the t_{LOW} delay time before powering down the device after blowing each bit.
- Set the LOCK bit (only after all other parameters have been programmed and validated) to prevent any further programming of the device.

READ MODE

The A1128 features a Read mode that allows the status of each programmable fuse to be read back individually. The status, blown or not blown, of the addressed fuse is determined by monitoring the state of the VOUT pin. A complete example is shown in figure 9.

Read mode uses the same register selection keys as Blow mode (see table 3), allowing direct addressing of the individual fuses in the BOPPOL and BOPSEL registers (do not inadvertently send a Blow pulse while in Read mode). After sending the register and mode selection keys, that is, after the falling edge of the final V_{PH} pulse in the key, the first bit (the LSB) is selected. Each additional V_{PM} pulse addresses the next bit in the selected register, up

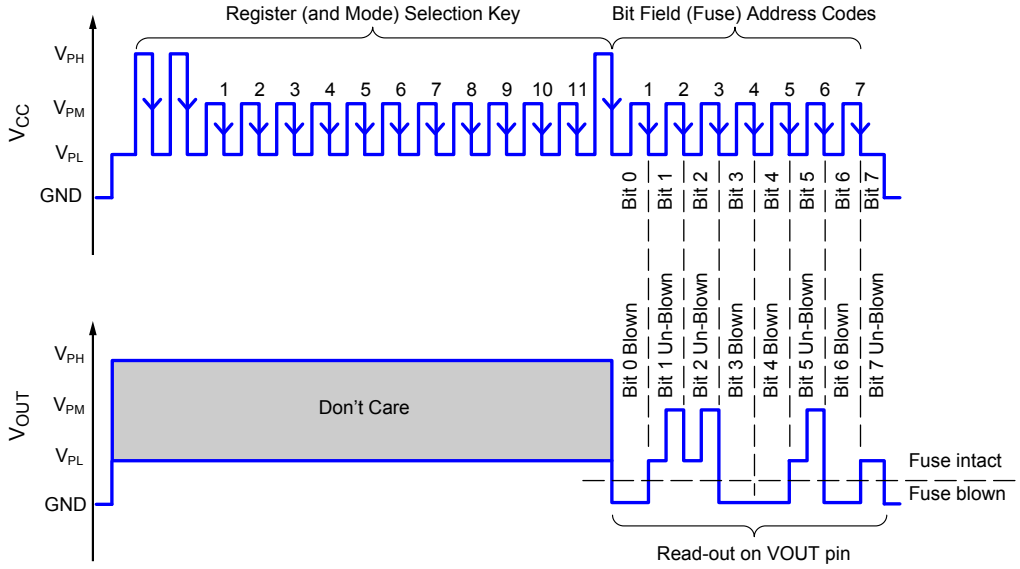

Figure 9. Read mode example. Pulse sequence for accessing the B_{OP} Selection register (BOPSEL) and reading back the status of each of the eight bit fields. In this example, the code (blown fuses) is $2^0 + 2^3 + 2^4 + 2^6 = 89$ (0101 1001). After each address pulse is sent, the voltage on the VOUT pin will be at GND for blown fuses and at V_{CC} (at V_{PL} or V_{PM}) for un-blown fuses.

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to the MSB. Read mode is available only before the LOCK bit has been set.

After the final V_{PH} key pulse, and after each V_{PM} address pulse, if V_{OUT} is low, the corresponding fuse can be considered blown (the status of the Output Polarity bit, POL, does not affect Read mode output values, allowing POL to be tested also). If the output state is high, the fuse can be considered un-blown. During Read mode VOUT must be pulled high using a pull-up resistor (see R_{LOAD} in the Typical Application Circuit diagram).

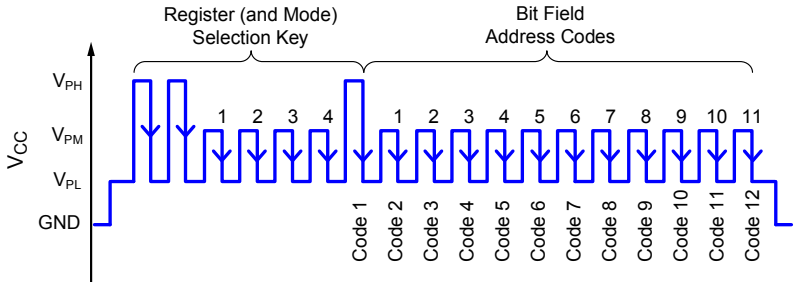

Figure 10. Example of Try mode programming pulses applied to the VCC pin. In this example, B_{OP} Positive Trim, Down-Counting register is addressed to code 12 by the eleven V_{PM} pulses (code 1 is selected automatically at the falling edge of the register-mode selection key).

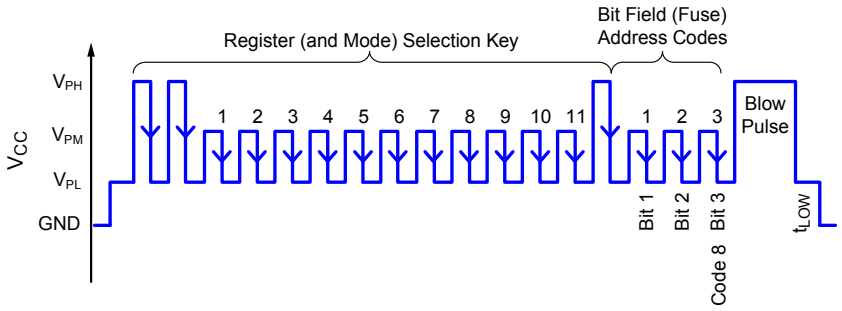

Figure 11. Example of Blow mode programming pulses applied to the VCC pin. In this example, the B_{OP} Magnitude Selection register (BOPSEL) is addressed to code 8 (bit 3, or 3 V_{PM} pulses) and its value is permanently blown.

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B_{OP} SELECTION

The A1128 allows accurate trimming of the magnetic operate point, B_{OP}, within the application. This programmable feature reduces effects due to mechanical placement tolerances and improves performance when used in proximity or vane sensing applications.

B_{OP} can be set to any value within the range allowed by the BOPSEL registers. This includes switchpoints of south or north polarity, and switchpoints at or near the zero crossing point for B. However, switching is recommended only within the Programmable B_{OP} Range, specified in the Operating Characteristics table.

Trimming of B_{OP} is typically done in two stages. In the first stage, B_{OP} is adjusted temporarily using the Try mode programming features, to find the fuse value that corresponds to the optimum B_{OP}. After a value is determined, then it can be permanently set using the Blow mode features.

As an aid to programming the A1128 has several options available in Try Mode for adjusting the B_{OP} parameter. As shown in figure 12, these allow trimming of B_{OP} for operation in north or south polarity magnetic fields. In addition the B_{OP} parameter can either trim-up, start at the B_{OP} minimum value and increase to the maximum value, or trim-down, starting at the B_{OP} maximum value and decreasing to the minimum value.

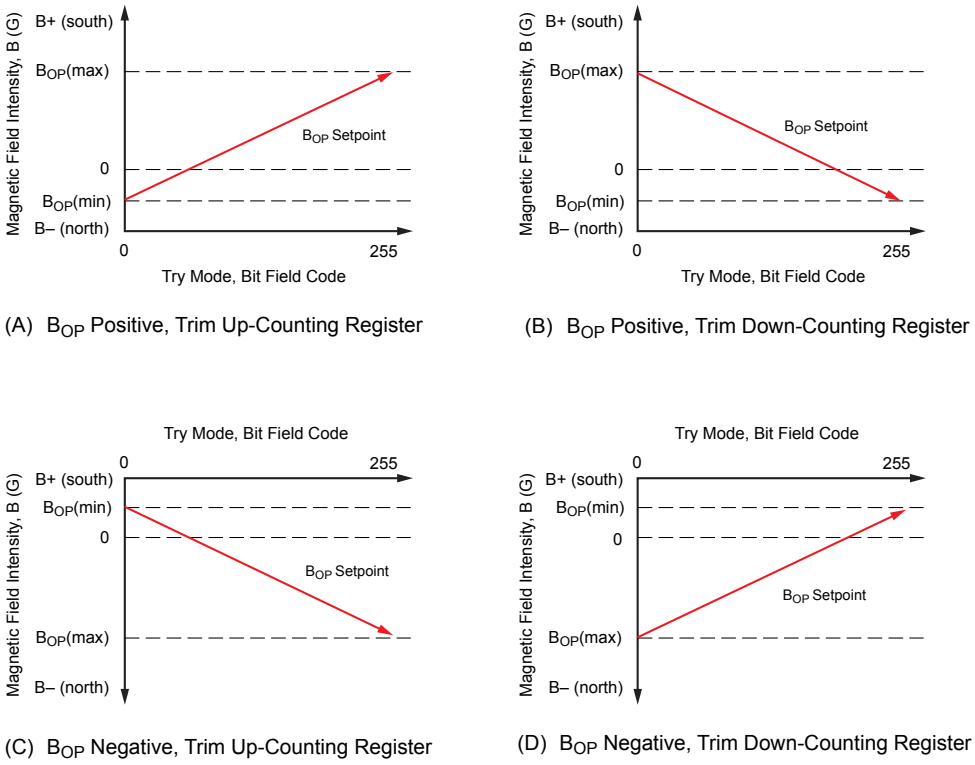

Figure 12. B_{OP} profiles for each of the four B_{OP} Selection virtual registers available in Try mode.

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POWER DERATING

The device must be operated below the maximum junction temperature of the device, $T_J(max)$. Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating T_J. (Thermal data is also available on the Allegro MicroSystems website.)

The Package Thermal Resistance, $R_{\theta JA}$, is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to the ambient air. Its primary component is the Effective Thermal Conductivity, K, of the printed circuit board, including adjacent devices and traces. Radiation from the die through the device case, $R_{\theta JC}$, is relatively small component of $R_{\theta JA}$. Ambient air temperature, T_A, and air motion are significant external factors, damped by overmolding.

The effect of varying power levels (Power Dissipation, P_D), can be estimated. The following formulas represent the fundamental relationships used to estimate T_J, at P_D.

$$P_D = V_{IN} \times I_{IN} \quad (1)$$

$$\Delta T = P_D \times R_{\theta JA} \quad (2)$$

$$T_J = T_A + \Delta T \quad (3)$$

For example, given common conditions such as: T_A= 25°C, V_{IN} = 12 V, I_{IN} = 4 mA, and $R_{\theta JA}$ = 140 °C/W, then:

$$P_D = V_{IN} \times I_{IN} = 12\ V \times 4\ mA = 48\ mW$$

$$\Delta T = P_D \times R_{\theta JA} = 48\ mW \times 140\ °C/W = 7°C$$

$$T_J = T_A + \Delta T = 25°C + 7°C = 32°C$$

A worst-case estimate, $P_D(max)$, represents the maximum allowable power level, without exceeding $T_J(max)$, at a selected $R_{\theta JA}$ and T_A.

Example: Reliability for V_{CC} at T_A=150°C, package UA, using a single-layer PCB.

Observe the worst-case ratings for the device, specifically: $R_{\theta JA}$=165 °C/W, $T_J(max)$ =165°C, $V_{CC}(max)$ =24 V, and $I_{CC}(max)$ = 5.5 mA.

Calculate the maximum allowable power level, $P_D(max)$. First, invert equation 3:

$$\Delta T_{max} = T_J(max) - T_A = 165°C - 150°C = 15°C$$

This provides the allowable increase to T_J resulting from internal power dissipation. Then, invert equation 2:

$$P_D(max) = \Delta T_{max} \div R_{\theta JA} = 15°C \div 165\ °C/W = 91\ mW$$

Finally, invert equation 1 with respect to voltage:

$$V_{CC}(est) = P_D(max) \div I_{CC}(max) = 91\ mW \div 5.5\ mA = 16.5\ V$$

The result indicates that, at T_A, the application and device can dissipate adequate amounts of heat at voltages $\leq V_{CC}(est)$.

Compare $V_{CC}(est)$ to $V_{CC}(max)$. If $V_{CC}(est) \leq V_{CC}(max)$, then reliable operation between $V_{CC}(est)$ and $V_{CC}(max)$ requires enhanced $R_{\theta JA}$. If $V_{CC}(est) \geq V_{CC}(max)$, then operation between $V_{CC}(est)$ and $V_{CC}(max)$ is reliable under these conditions.

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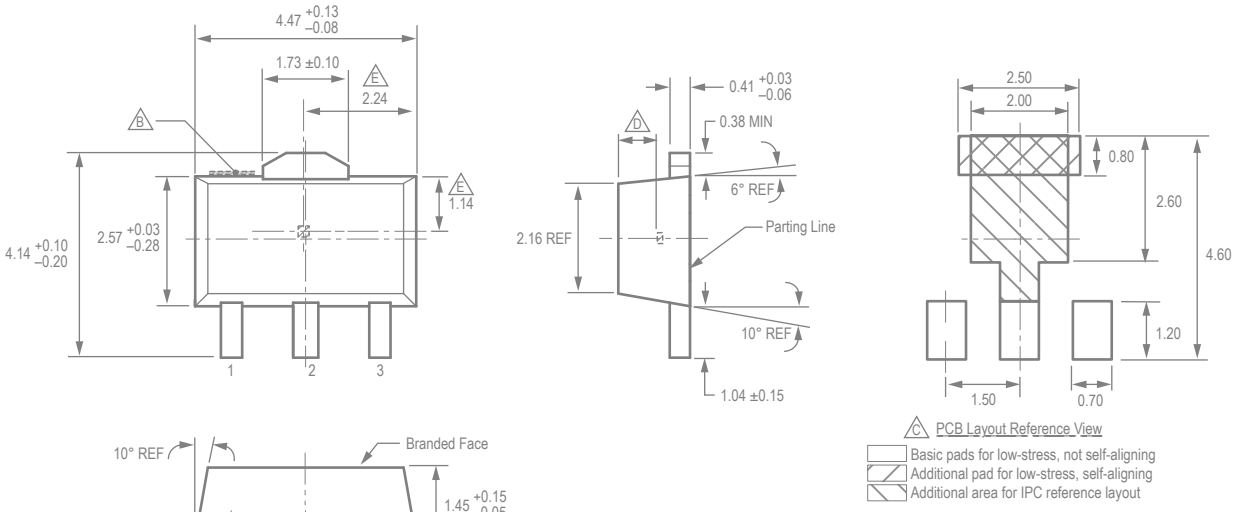
PACKAGE OUTLINE DRAWINGS

Package LT 3-Pin SOT-89



LAST-TIME BUY

Updated package drawing only. Allegro package assembly tooling has not changed.
For Reference Only; not for tooling use (reference DWG-9064)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Branding scale and appearance at supplier discretion

B Gate and tie bar burr area

C Reference land pattern layout;
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

D Active Area Depth, 0.77 mm

E Hall element; not to scale

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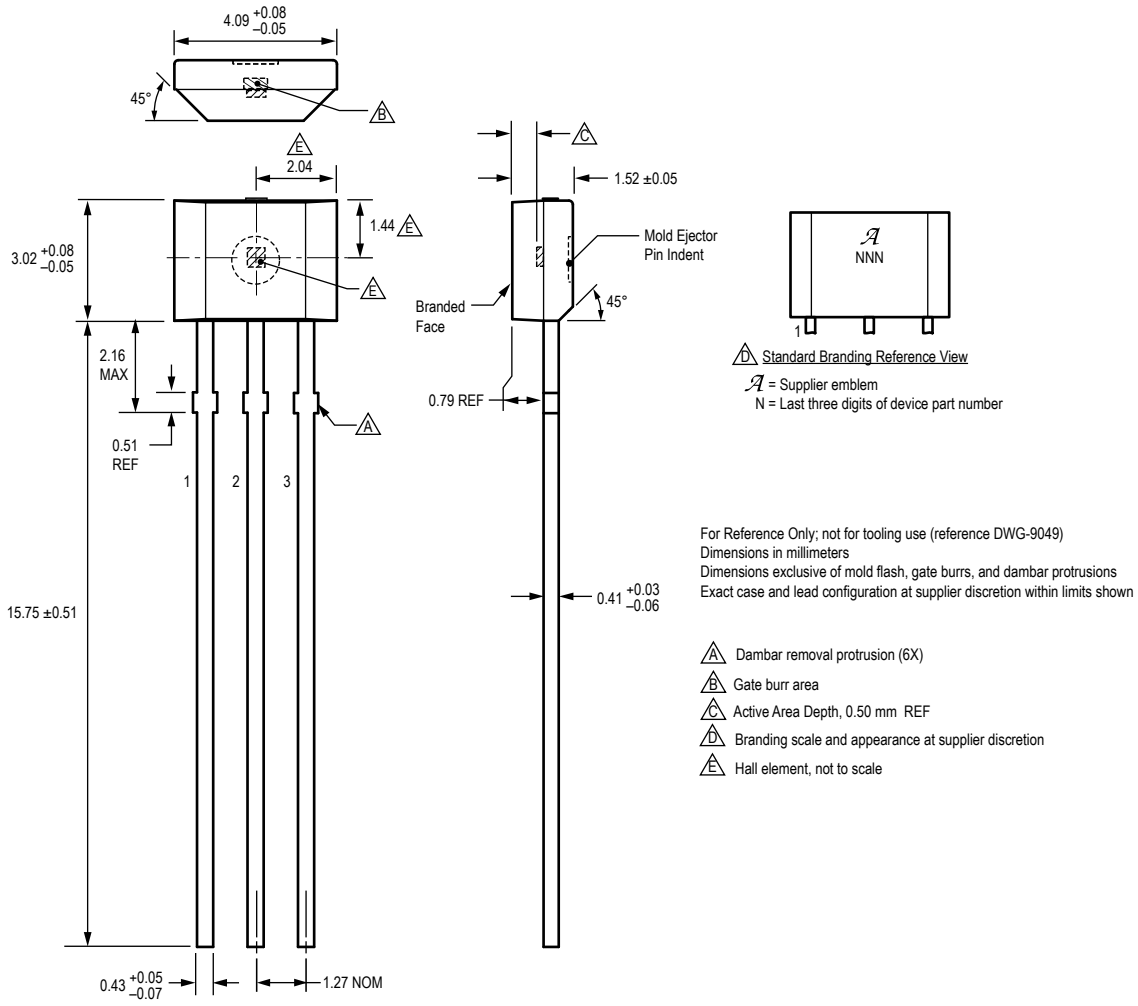
Package UA 3-Pin SIP



For Reference Only; not for tooling use (reference DWG-9049)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Dambar removal protrusion (6X)
B Gate burr area
C Active Area Depth, 0.50 mm REF
D Branding scale and appearance at supplier discretion
E Hall element, not to scale

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Package UA 3-Pin SIP, TS Leadform

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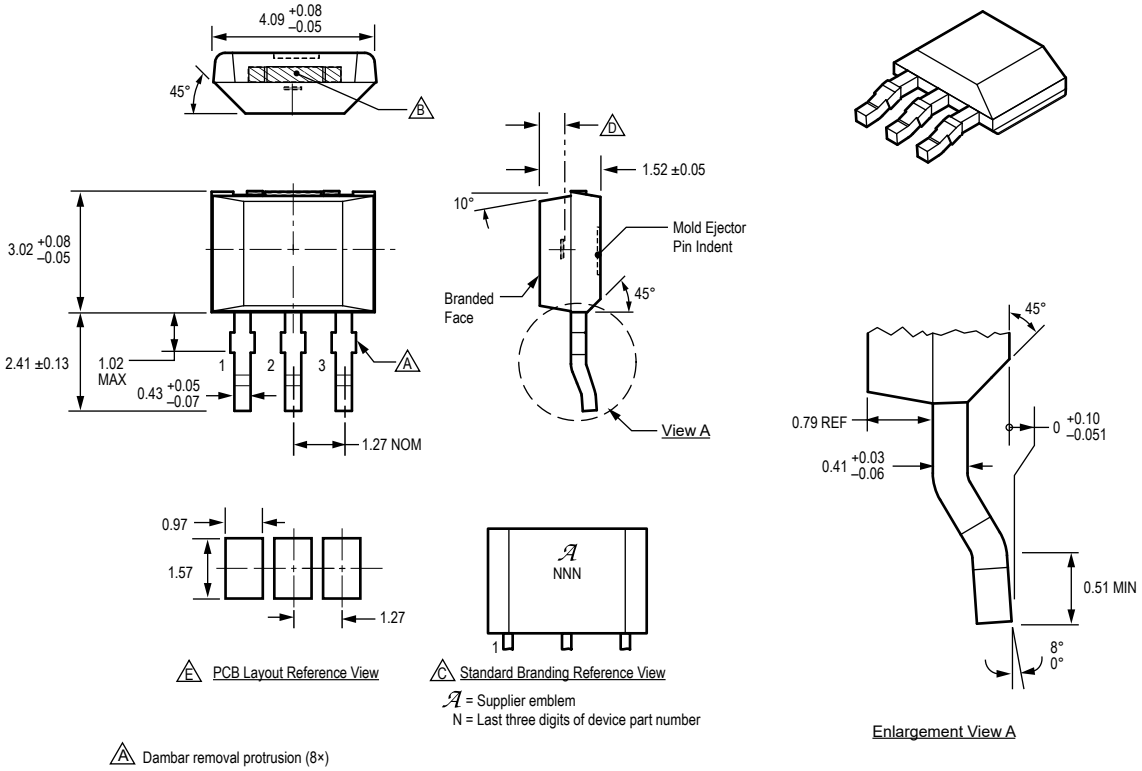
(For package, reference DWG-9065; for lead forming, reference DWG-9116)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



A Dambar removal protrusion (8×)

B Gate and tie bar burr area

C Branding scale and appearance at supplier discretion

D Active Area Depth, 0.50 mm ±0.08

E Reference land pattern layout;
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

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Revision History

Number	Date	Description
3	September 6, 2018	Minor editorial updates
4	December 7, 2018	Updated -LT package option status to Last-Time Buy; added UA package TS leadform option

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