TPS2398, TPS2399

-48 V Hot Swap Controller for Redundant Supply Systems

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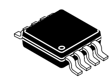
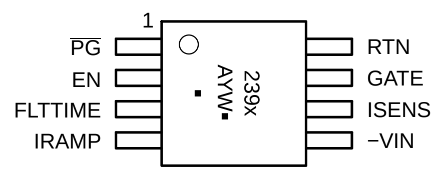


MSOP−8
Z SUFFIX
CASE 846AD

PIN CONNECTIONS AND MARKING DIAGRAM



(Top View)

239x	= Specific Device Code x = 8 or 9
A	= Assembly Location
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 15 of this data sheet.

The TPS2398 and TPS2399 integrated circuits are hot swap power managers optimized for use in nominal −48 V systems. They incorporate an improved circuit breaker response that provides rapid protection from short circuits, while still enabling plug−ins to tolerate large transients that can be generated by the sudden switchover to a higher voltage supply. They are designed for supply voltage ranges up to −80 V, and are rated to withstand spikes to −100 V. In conjunction with an external N−channel FET and sense resistor, they can be used to enable live insertion of plug−in cards and modules in powered systems. Both devices provide load current slew rate and peak magnitude limiting, easily programmed by sense resistor value and a single external capacitor.

Features

- Wide Input Supply: −36 V to −80 V
- Transient Rating to −100 V
- Improved Transient Response
- Enable Input (EN)
- Programmable Current Limit
- Programmable Current Slew Rate
- Fault Timer to Eliminate Nuisance Trips
- Open−Drain Power Good Output ($\overline{\text{PG}}$)
- MSOP−8 Package
- These are Pb−Free Devices

Typical Applications

- −48 V Distributed Power Systems
- Redundant Negative Voltage Supplies
- Central Office Switching Systems

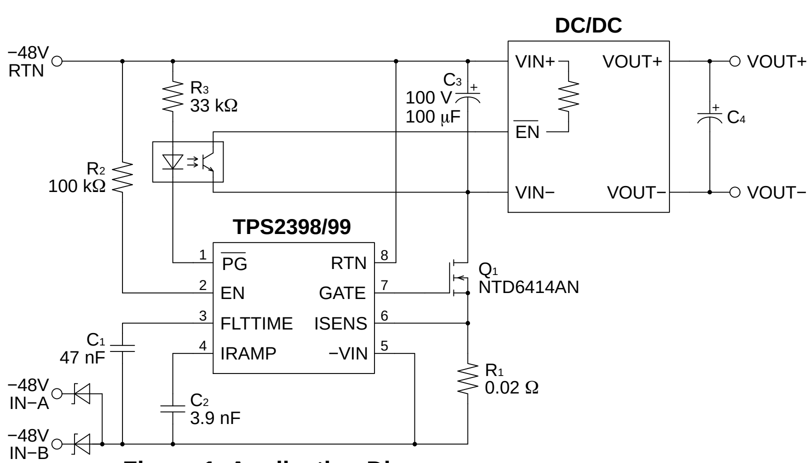


Figure 1. Application Diagram

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Publication Order Number:
TPS2398/D

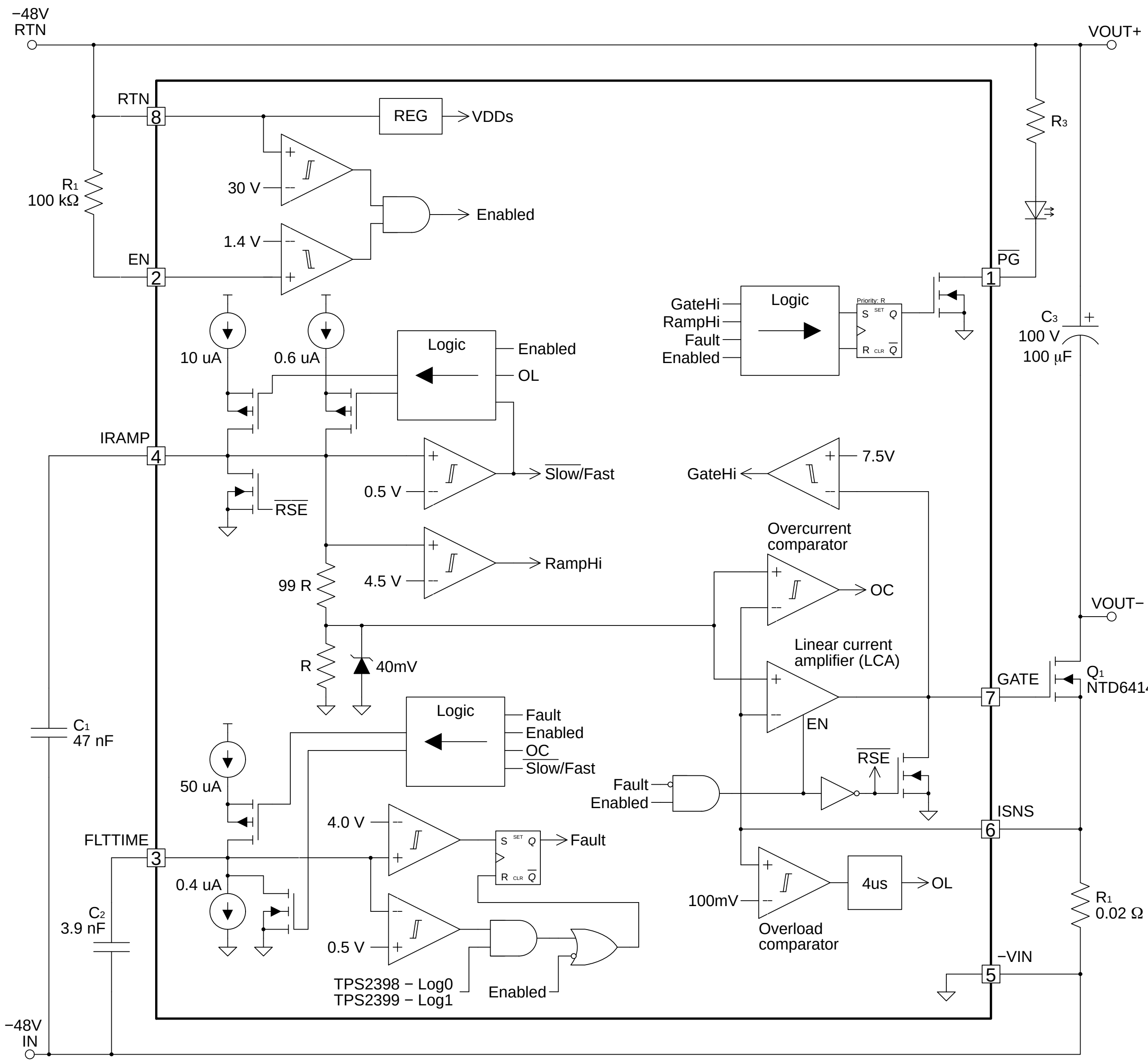


Figure 2. Internal Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

Pin Number	Pin Name	Description
2	EN	Enable input to turn on/off power to the load
1	PG	Open−drain, active−low indication of a load power good condition.
3	FLTTIME	Connection for user−programming of the fault timeout period.
7	GATE	Gate drive for external N−channel FET
4	IRAMP	Programming input for setting the inrush current slew rate.
6	ISENS	Current sense input.
8	RTN	Positive supply input for the TPS2398 and TPS2399.
5	−VIN	Negative supply input and reference pin for the TPS2398 and TPS2399.

Table 2. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input voltage range, all pins except RTN, EN, $\overline{PG}$ (Note 1)		−0.3 to 15	V
Input voltage range, RTN (Note 1)	RTN	−0.3 to 100	V
Input voltage range, EN (Notes 1, 2)	EN	−0.3 to 100	V
Output voltage range, $\overline{PG}$ (Notes 1, 3)	$\overline{PG}$	−0.3 to 100	V
Continuous output current, $\overline{PG}$	I_{PG}	10	mA
Continuous total power dissipation, $T_A < 25$	$P_{D(MAX)}$	420	mW
Operating junction temperature range	$T_{J(MAX)}$	−40 to 125	°C
Storage temperature range	T_{STG}	−55 to 150	°C
Lead temperature soldering 1.6 mm (1/16 inch) from case for 10 seconds	T_{SOL}	260	°C
Human Body Model (HBM) (Note 4)	ESD_{HBM}	2.0	kV
Charged Device Model (CDM) (Note 4)	ESD_{CDM}	1.5	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. With 100−kΩ minimum input series resistance, −0.3 V to 15 V with low impedance.
3. With 10−kΩ minimum input series resistance, −0.3 V to 80 V with low impedance.
4. All pins except RTN pin which is specified up to 1.0 kV.

Table 3. RECOMMENDED OPERATING CONDITIONS

Rating	Min	Nom	Max	Unit
Nominal input supply, −VIN to RTN	−80		−36	V
Operating ambient temperature	−40		85	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 4. DISSIPATION RATING TABLE

Package	$T_A < 25°C$	Derating Factor	$T_A < 85°C$
MSOP−8	420 mW	4.3 mW/°C	160 mW

Table 5. ELECTRICAL CHARACTERISTICS

$V_{I(−VIN)}$ = −48 V with respect to RTN, $V_{I(EN)}$ = 2.8 V, $V_{I(ISENS)}$ = 0 V, all outputs unloaded, device not in fault mode, T_J = 25°C; unless otherwise noted. The Min and Max specifications are guaranteed at −40°C ≤ T_J ≤ 85°C. (Notes 5, 6)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
INPUT SUPPLY						
Supply current, RTN	$V_{I(RTN)}$ = 48 V	I_{CC}		310	450	μA
	$V_{I(RTN)}$ = 80 V			310	450	μA
UVLO threshold, input voltage rising	To GATE pull−up, referenced to RTN	V_{UVLO_L}	−36	−30	−25	V
UVLO hysteresis		V_{HYS}	1.8	2.3	3.0	V
ENABLE INPUT (EN)						
Threshold voltage, input voltage rising	To GATE pull−up	V_{TH}	1.25	1.35	1.5	V
EN hysteresis		V_{HYS_EN}	20	40	90	mV
High−level input current	$V_{I(EN)}$ = 5 V	I_{IH}	−2	1	2	μA
LINEAR CURRENT AMPLIFIER (LCA)						
High−level output, GATE	$V_{I(ISENS)}$ = 0 V	V_{OH}	11	14	17	V
Output sink current	$V_{I(ISENS)}$ = 80 mV, $V_{O(GATE)}$ = 5 V, Fault mode	I_{SINK}	50	100		mA
Input current, ISENS	0 V < $V_{I(ISENS)}$ < 0.2 V	I_I	−1		1	μA

5. All voltages are with respect to the −VIN terminal unless otherwise stated.
6. Currents are positive into and negative out of the specified terminal.

Table 5. ELECTRICAL CHARACTERISTICS
$V_{I(-VIN)}$ = −48 V with respect to RTN, $V_{I(EN)}$ = 2.8 V, $V_{I(ISENS)}$ = 0 V, all outputs unloaded, device not in fault mode, T_J = 25°C; unless otherwise noted. The Min and Max specifications are guaranteed at −40°C ≤ T_J ≤ 85°C. (Notes 5, 6)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
LINEAR CURRENT AMPLIFIER (LCA)						
Reference clamp voltage	$V_{O(IRAMP)}$ = open	V_{REF_K}	33	40	46	mV
Input offset voltage	$V_{O(IRAMP)}$ = 2 V	V_{IO}	−7		6	mV
RAMP GENERATOR						
IRAMP source current, slow turn−on rate	$V_{O(IRAMP)}$ = 0.25 V	I_{SRC1}	−850	−600	−400	nA
IRAMP source current, normal rate	$V_{O(IRAMP)}$ = 1 V, 3 V	I_{SRC2}	−11	−10	−9	μA
Low−level output voltage	$V_{I(EN)}$ = 0 V	V_{OL}			5	mV
Voltage gain, relative to ISENS	$V_{O(IRAMP)}$ = 1 V, 3 V	A_V	9.5	10	10.5	mV/V
OVERLOAD COMPARATOR						
Current overload threshold, ISENS		V_{TH_OL}	80	100	120	mV
Glitch filter delay time	$V_{I(ISENS)}$ = 200 mV	t_{DLY}	2	4	7	μs
FAULT TIMER						
Low−level output voltage	$V_{I(EN)}$ = 0 V	V_{OL}			5	mV
Charging current, current limit mode	$V_{I(ISENS)}$ = 80 mV, $V_{O(FLTTIME)}$ = 2 V	I_{CHG}	−55	−50	−45	μA
Fault threshold voltage		V_{FLT}	3.75	4.0	4.25	V
Discharge current, retry mode (TPS2399)	$V_{I(ISENS)}$ = 80 mV, $V_{O(FLTTIME)}$ = 2 V, Fault Mode	I_{DSG}		0.38	0.75	μA
Output duty cycle (TPS2399)		D		0.8	1.5	%
Discharge current, timer reset mode	$V_{O(FLTTIME)}$ = 2 V	I_{RST}		1		mA
$\overline{PG}$ OUTPUT						
High−level output (leakage) current	$V_{I(EN)}$ = 0 V, $V_{O(\overline{PG})}$ = 65 V	I_{OH}			10	μA
Driver ON resistance	$I_{O(\overline{PG})}$ = 1 mA	$R_{DS(ON)}$		35	80	Ω

5. All voltages are with respect to the −VIN terminal unless otherwise stated.
6. Currents are positive into and negative out of the specified terminal.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

$V_{I(-VIN)} = -48$ V with respect to RTN, $V_{I(EN)} = 2.8$ V, $V_{I(ISENS)} = 0$ V, all outputs unloaded, device not in fault mode, $T_J = 25°C$

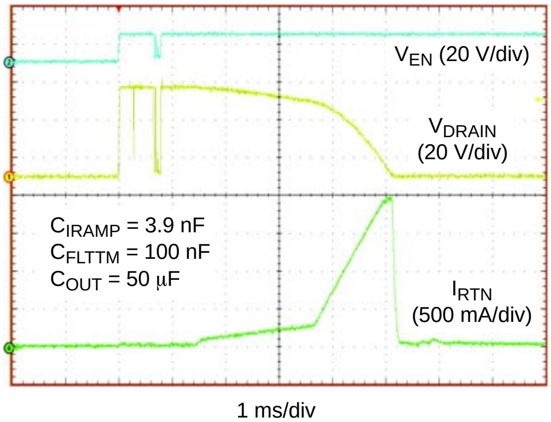


Figure 3. Live Insertion Event, $V_{IN} = -48$ V

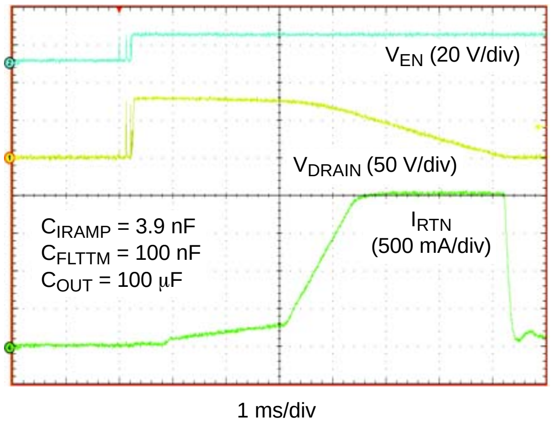


Figure 4. Live Insertion Event, $V_{IN} = -80$ V

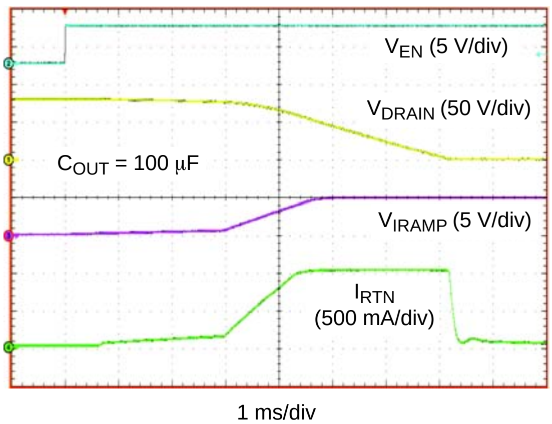


Figure 5. Start−up from Enable, $V_{IN} = -80$ V

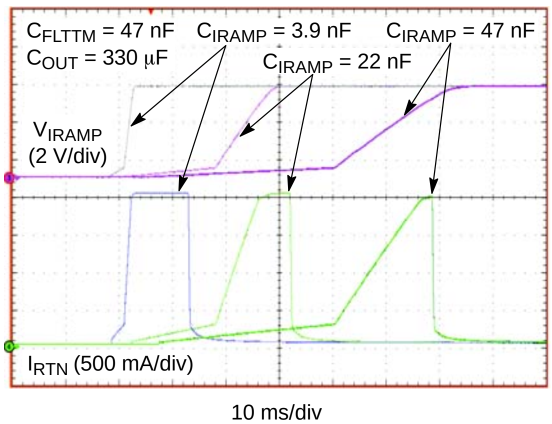


Figure 6. Output Current Ramp Profiles

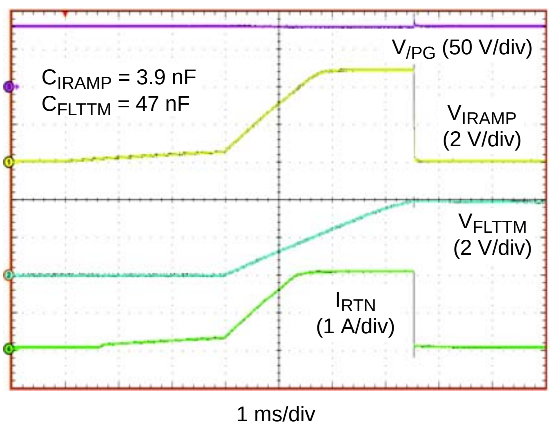


Figure 7. Turn−On into Short (TPS2399 only)

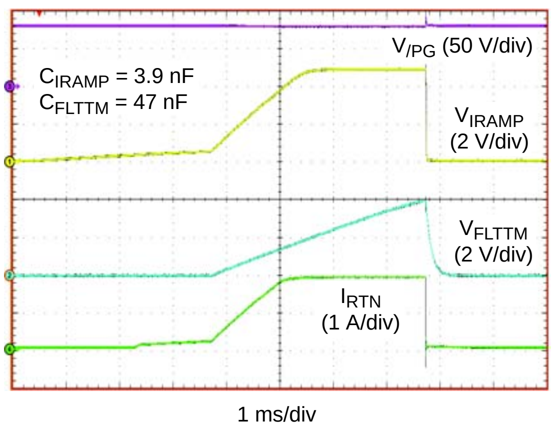


Figure 8. Turn−On into Short (TPS2398 only)

TYPICAL CHARACTERISTICS

$V_{I(-VIN)}$ = −48 V with respect to RTN, $V_{I(EN)}$ = 2.8 V, $V_{I(ISENS)}$ = 0 V, all outputs unloaded, device not in fault mode, T_J = 25°C

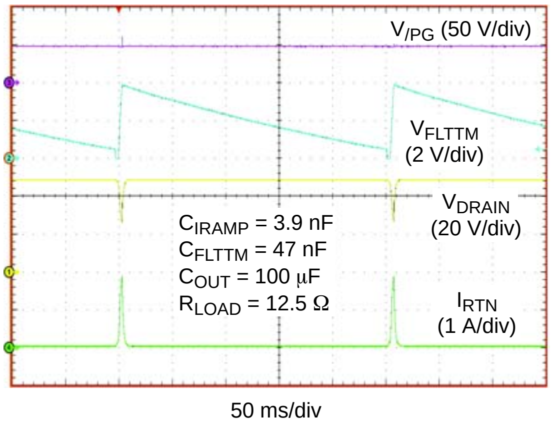


Figure 9. Fault−Retry Operation (TPS2399 only)

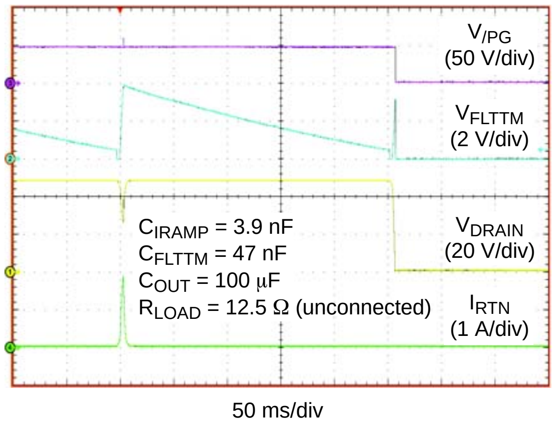


Figure 10. Recovery from a Fault (TPS2399 only)

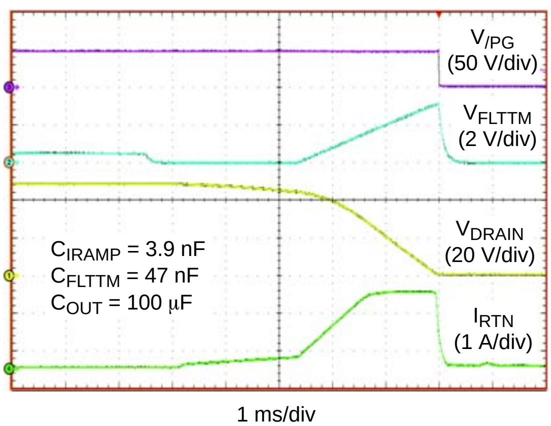


Figure 11. Recovery from a Fault − Expanded View (TPS2399 only)

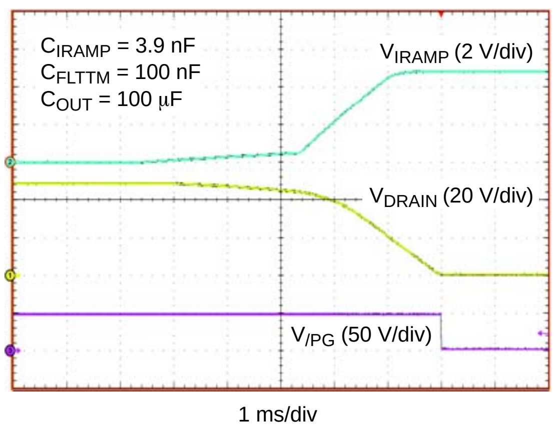


Figure 12. $\overline{\text{PG}}$ Ouput Timing − Voltage Qualified

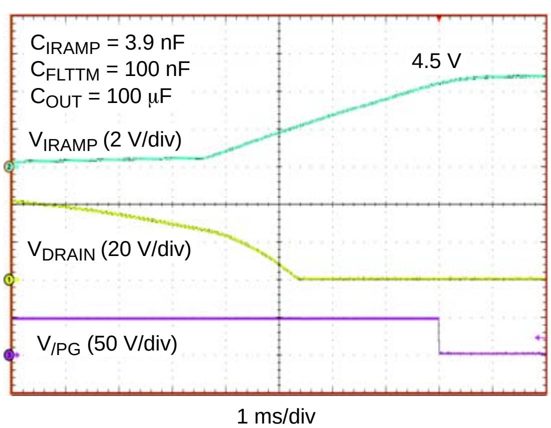


Figure 13. $\overline{\text{PG}}$ Ouput Timing − Current Qualified

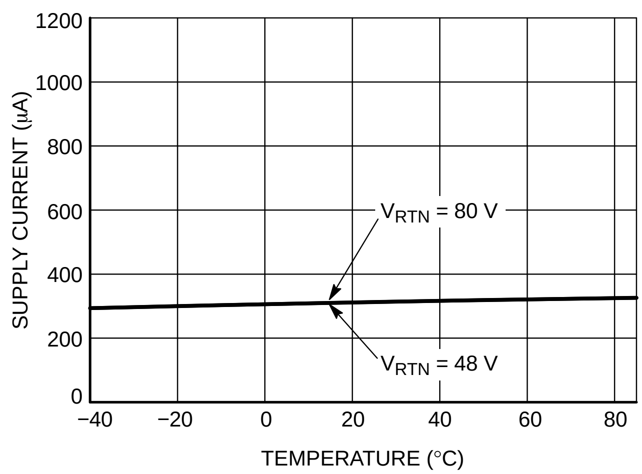


Figure 14. Supply Current

TYPICAL CHARACTERISTICS

$V_{I(-VIN)}$ = −48 V with respect to RTN, $V_{I(EN)}$ = 2.8 V, $V_{I(ISENS)}$ = 0 V, all outputs unloaded, device not in fault mode, T_J = 25°C

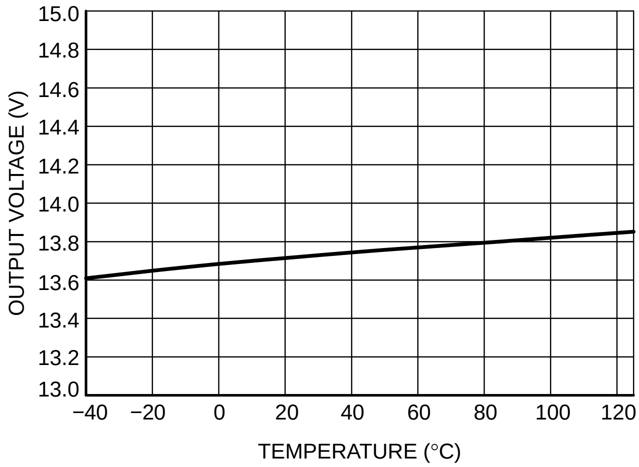


Figure 15. GATE High Output Voltage

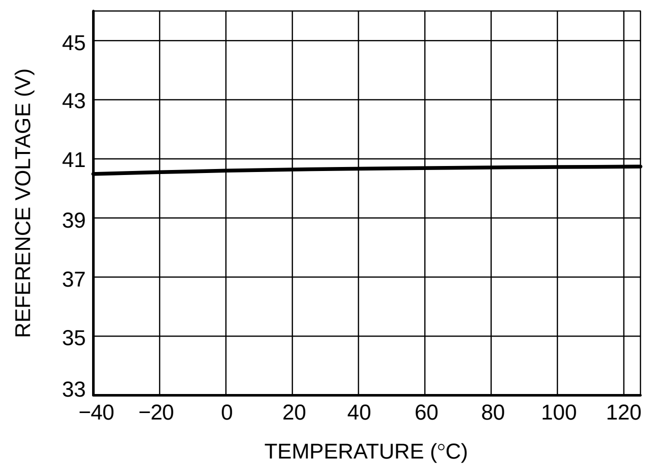


Figure 16. Reference Clamp Voltage

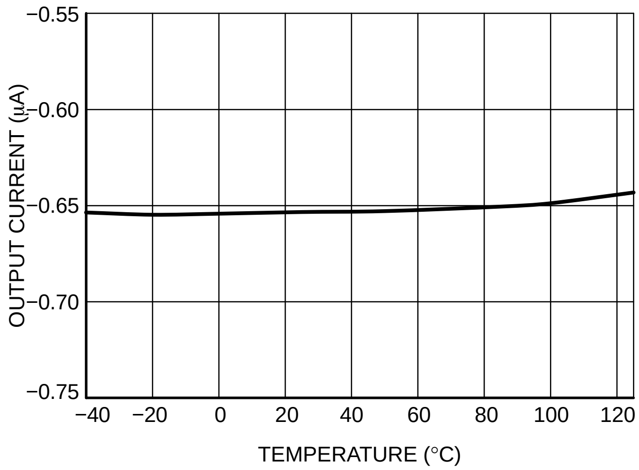


Figure 17. IRAMP Output Current − Slow Rate

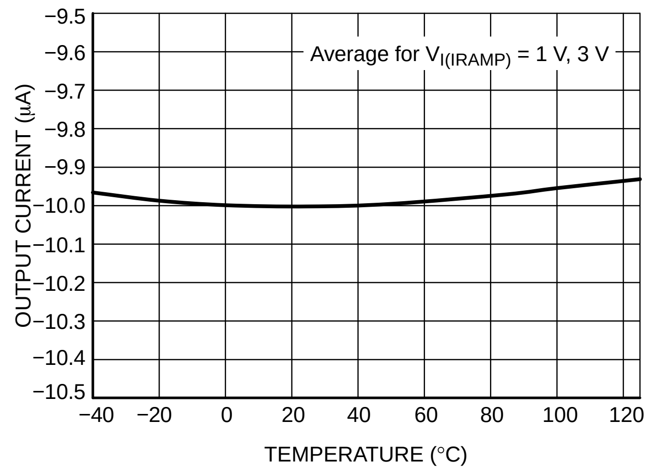


Figure 18. IRAMP Output Current − Fast Rate

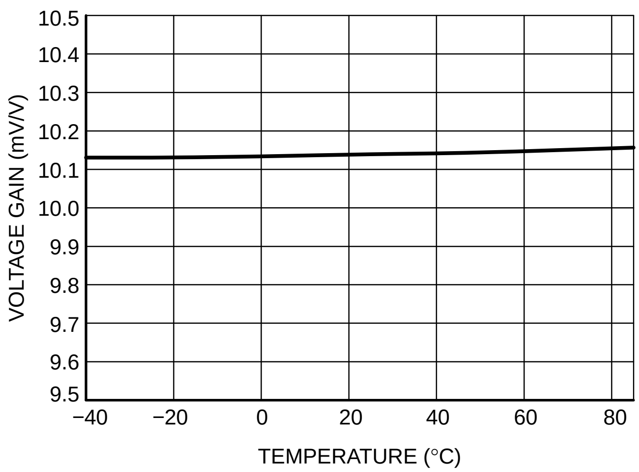


Figure 19. Voltage Gain, relative to ISNS

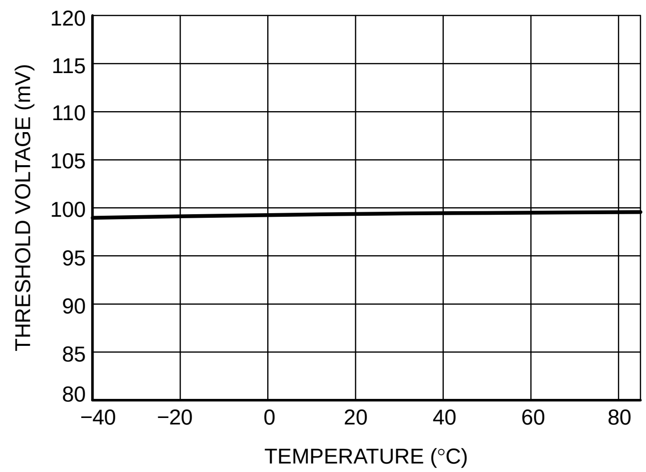


Figure 20. Current Overload Threshold, ISNS

TYPICAL CHARACTERISTICS

$V_{I(-VIN)}$ = −48 V with respect to RTN, $V_{I(EN)}$ = 2.8 V, $V_{I(ISENS)}$ = 0 V, all outputs unloaded, device not in fault mode, T_J = 25°C

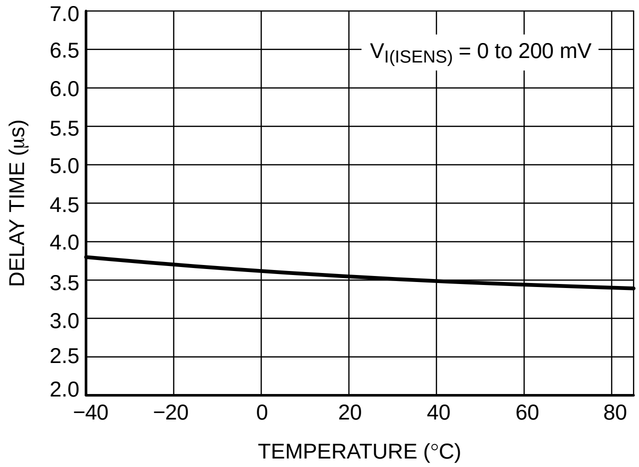


Figure 21. Glitch Filter Delay Time

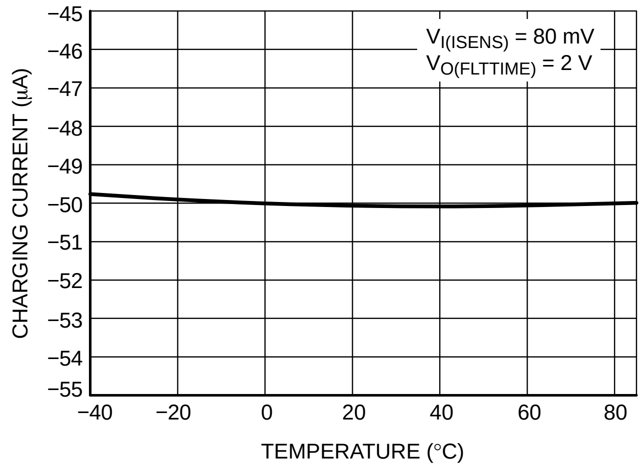


Figure 22. FLTTIME Charging Current

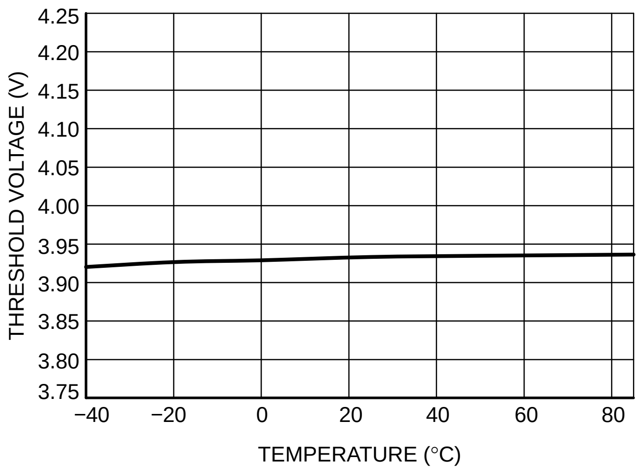


Figure 23. FLTTIME Threshold Voltage

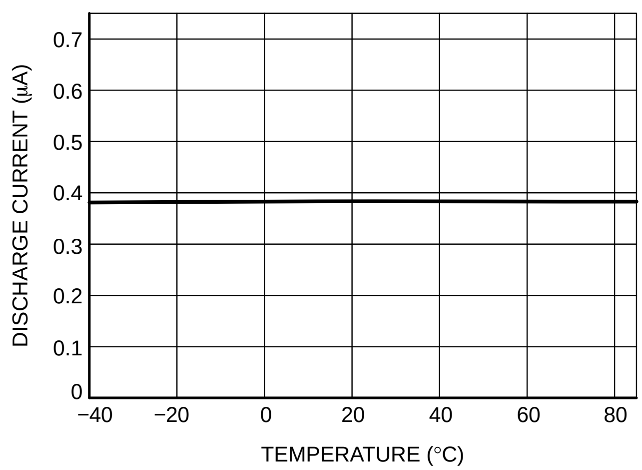


Figure 24. FLTTIME Discharge Current

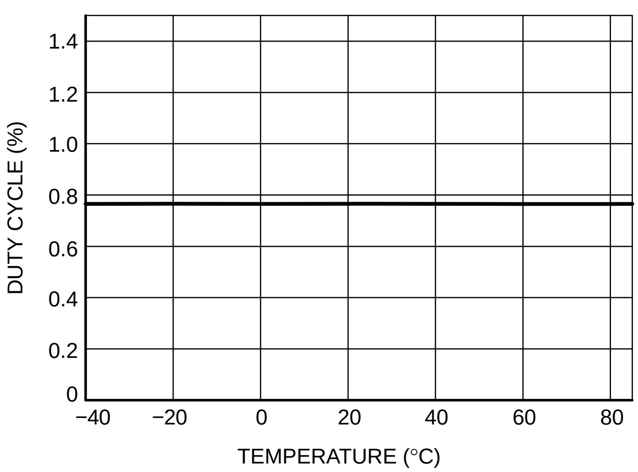


Figure 25. Fault−Retry Duty Cycle

DETAILED PIN DESCRIPTIONS

EN

Enable input to turn on/off power to the load. The EN pin is referenced to the −VIN potential of the circuit. When this input is pulled high (above the nominal 1.4 V threshold) the device enables the GATE output, and begins the ramp of current to the load. When this input is low, the linear current amplifier (LCA) is disabled, and a large pull−down device is applied to the FET gate, disabling power to the load.

FLTTIME

Connection for user−programming of the fault timeout period. An external capacitor connected from FLTTIME to −VIN establishes the timeout period to declare a fault condition. This timeout protects against indefinite current sourcing into a faulted load, and also provides a filter against nuisance trips from momentary current spikes or surges. The TPS2398 and TPS2399 define a fault condition as voltage at the ISENS pin at or greater than the 40 mV fault threshold. When a fault condition exists, the timer is active. The devices manage fault timing by charging the external capacitor to the 4 V fault threshold, then subsequently discharging it to reset the timer (TPS2398), or discharging it at approximately 1% the charge rate to establish the duty cycle for retrying the load (TPS2399). Whenever the internal fault latch is set (timer expired), the pass FET is rapidly turned off, and the /PG output is de−asserted.

GATE

Gate drive for external N−channel FET. When enabled, and the input supply is above the UVLO threshold, the gate drive is enabled and the device begins charging an external capacitor connected to the IRAMP pin. This pin voltage is used to develop the reference voltage at the non−inverting input of the internal LCA. The inverting input is connected to the current sense node, ISENS. The LCA acts to slew the pass FET gate to force the ISENS voltage to track the reference. The reference is internally clamped at 40 mV, so the maximum current that can be sourced to the load is determined by the sense resistor value as $I_{MAX} \leq 40\ mV / R_{SNS}$. Once the load voltage has ramped up to the input dc potential, and current demand drops off, the LCA drives the GATE output to about 14 V to fully enhance the pass FET, completing the low−impedance supply return path for the load.

IRAMP

Programming input for setting the inrush current slew rate. An external capacitor connected between this pin and −VIN establishes the load current slew rate whenever power to the load is enabled. The device charges the external capacitor to establish the reference input to the LCA. The closed−loop control of the LCA and pass FET acts to maintain the current sense voltage at ISENS at the reference potential. Since the sense voltage is developed as the drop across a resistor, the charging current ramp rate is set by the voltage ramp rate at the IRAMP pin. When the output is disabled via the EN input or due to a load fault, the capacitor is discharged and held low to initialize for the next turn−on.

ISENS

Current sense input. An external low value resistor connected between this pin and −VIN is used to feedback current magnitude information to the TPS2398/99. There are two internal device thresholds associated with the voltage at the ISENS pin. During charging of the load's input capacitance, or during other periods of excessive demand, the HSPM acts to limit this voltage to 40 mV. Whenever the LCA is in current regulation mode, the capacitor at FLTTIME pin is charged to activate the timer. If, when the LCA is driving to its supply rail, a fast−acting fault such as a short−circuit, causes the ISENS voltage to exceed 100 mV (the overload threshold), the GATE pin is pulled low rapidly, bypassing the fault timer.

$\overline{\text{PG}}$

Open−drain, active−low indication of load power good. A power good status is declared when the output is enabled, the GATE pin voltage has ramped to at least 7.5 V, and the voltage on the IRAMP pin exceeds approximately 4.5 V. This last condition assures that full programmed sourcing current is available prior to declaring power good, even with very slow current ramp rates. This additional protection prevents potential discharging of the module input bulk capacitance during load turn−on.

RTN

Positive supply input for the TPS2398/99. For negative voltage systems, the supply pin connects directly to the return node of the input power bus. Internal regulators lower down the input voltage to generate the various supply levels used by the TPS2398 and TPS2399.

−VIN

Negative supply input and reference pin for the TPS2398/99. This pin connects directly to the input supply negative rail. The input and output pins and all internal circuitry are referenced to this pin, so it is essentially the GND or VSS pin of the device.

APPLICATIONS INFORMATION

General

When a plug−in module or printed circuit card is inserted into a live chassis slot, discharged supply bulk capacitance on the board can draw huge transient currents from the system supplies. Without some form of inrush limiting, these currents can reach peak magnitudes ranging up to several hundred amps, particularly in high−voltage systems. Such large transients can damage connector pins, PCB etch, and plug−in and supply components. In addition, current spikes can cause voltage droops on the power distribution bus, causing other boards in the system to reset.

The TPS2398 and TPS2399 are hot swap power managers designed to limit these peaks to preset levels, as well as control the slew rate (di/dt) at which charging current ramps to the user−programmed limit. These devices use an external N−channel pass FET and sense element to provide closed−loop control of current sourced to the load. Input supply under−voltage lockout (UVLO) protection allows hot swap circuits to turn on automatically with the application of power, or to be controlled with a system command via the EN input. External capacitors control both the current ramp rate, and the time−out period for load voltage ramping. In addition, an internal overload comparator provides circuit breaker protection against shorts occurring during steady−state (post−turn−on) operation of the card.

The TPS2398 and TPS2399 operate directly from the input supply (nominal −48 VDC rail). The –VIN pin connects to the negative voltage rail, and the RTN pin connects to the supply return. Internal regulators convert input power to the supply levels required by the device circuitry. An input UVLO circuit holds the GATE output low until the supply voltage reaches a nominal 30 V level. A second comparator monitors the EN input; this pin must be pulled above the 1.4 V enable threshold to turn on power to the load.

Once enabled, and when the input supply is above the UVLO threshold, the GATE pull−down is removed, the linear control amplifier (LCA) is enabled, and a large discharge device in the RAMP CONTROL block is turned off. Subsequently, a small current source is now able to charge an external capacitor connected to the IRAMP pin. This results in a linear voltage ramp at IRAMP. The voltage ramp on the capacitor actually has two discrete slopes. As shown in Figure 2, charging current is supplied from either of two sources. Initially at turn−on, the 600 nA source is selected, to provide a slow turn−on rate. This slow turn−on helps ensure that the LCA is pulled out of saturation, and is slewing to the voltage at its non−inverting input before normal rate load charging is allowed. This mechanism helps reduce current steps at turn−on. Once the voltage at the IRAMP pin reaches approximately 0.5 V, an internal comparator de−asserts the SLOW signal, and the 10 μA source is selected for the remainder of the ramp period.

The voltage at IRAMP is divided down by a factor of 100, and applied to the non−inverting input of the LCA. Load current magnitude information at the ISENS pin is applied to the inverting input. This voltage is developed by connecting the current sense resistor between ISENS and −VIN. The LCA controls the gate of the external pass FET to force the ISENS voltage to track the divided down IRAMP voltage. Consequently, the load current slew rate tracks the linear voltage ramp at the IRAMP pin, producing a linear di/dt of the load current. The IRAMP capacitor is charged to about 5 V; however, the LCA input is clamped at 40 mV. Therefore, the current sourced to the load during turn−on is limited to a value given by $I_{MAX} \leq 40\text{ mV} / R_{SNS}$, where R_{SNS} is the value of the sense resistor.

The resultant load current, regulated by the controller, charges the module's input bulk capacitance in a safe fashion. Under normal conditions, this capacitance eventually charges up to the dc input potential. At this point, the load demand drops off, and the voltage at ISENS decreases. The LCA now drives the GATE output to its supply rail.

The device detects this condition as the GATE voltage rises through 7.5 V, latches this status and asserts the /PG output. If the full sourced current limit is not yet available to the load, as evidenced by the IRAMP voltage being less than 5 V, then the /PG assertion is delayed until that condition is also met.

The peak, steady−state GATE pin output, typically 14 V, ensures sufficient overdrive to fully enhance the external FET, while not exceeding the typical 20 V V_{GS} rating of common N−channel power FETs.

Fault timing is accomplished by connecting a capacitor between the FLTTIME and −VIN pins, allowing user−programming of the timeout period. Whenever the hot swap controller is in current control mode as described above, the LCA asserts an overcurrent indication – OC signal in the Figure 2. Overcurrent fault timing is inhibited during the slow turn−on portion of the IRAMP waveform. However, once the device transitions to the normal rate current ramp ($V_{IRAMP} \geq 0.5$ V), the external capacitor is charged by a 50 μA source, generating a voltage ramp at the FLTTIME pin. If the load voltage ramps successfully, the fault capacitor is discharged, and load initialization can begin. However, if the timing capacitor voltage attains the 4 V fault threshold, the LCA is disabled, the pass FET is rapidly turned off, and the fault is latched. Fault capacitor charging ceases, and the capacitor is then discharged. In addition, latching of a fault condition causes rapid discharge of the IRAMP capacitor. In this manner, the soft−start function is then reset and ready for the next output enable, if and when conditions permit.

Subsequent to a plug−in's start−up, and during the module's steady−state operation, load faults that force current limit operation also initiate fault timing cycles as described above. In this case, a fault timeout also clears the previously latched power good status.

The TPS2398 latches off in response to faults; once a fault timeout occurs, a large NMOS device is activated to rapidly discharge the external capacitor, resetting the timer for any subsequent device reset. The TPS2398 can only be reset by cycling power to the device, or by cycling the EN input.

In response to a latched fault condition, the TPS2399 enters a fault retry mode, wherein it periodically retries the load to test for continued existence of the fault. In this mode, the FLTTIME capacitor is discharged slowly by a about a 0.4 μA constant−current sink. When the voltage at the FLTTIME pin decays below 0.5 V, the LCA and RAMP CONTROL circuits are re−enabled, and a normal turn−on current ramp ensues. Again, during the load charging, the OC signal causes charging of the FLTTIME capacitor until the next delay period elapses. The sequential charging and discharging of the FLTTIME capacitor results in a typical 1% retry duty cycle. If the fault subsides, the timing capacitor is rapidly discharged, duty−cycle operation stops, and the /PG output is asserted.

Note that because of the timing inhibit during the initial slow ramp period, the duty cycle in practice is slightly greater than the nominal 1% value. However, sourced current during this period peaks at only about one−eighth the maximum limit. The duty cycle of the normal ramp and constant−current periods is approximately 1%.

The FAULT LOGIC within the TIMER BLOCK automatically manages capacitor charge and discharge actions, and the enabling of the GATE output.

Supply Transient Response

The TPS2398 and TPS2399 also feature a fast−acting overload comparator which acts to clamp large transients from catastrophic faults occurring once the pass FET is fully enhanced, such as short circuits. This function provides a back−up protection to the LCA by providing a hard gate discharge action when the LCA is saturated. If sense voltage excursions above 100 mV are detected, this comparator rapidly pulls down the GATE output, bypassing the fault timer, and terminating the short−circuit condition. Once the spike has been brought down below the overload threshold, the GATE output is released, allowing the circuit to turn on again in either current−ramp or current−limit mode. A 4 μs deglitch filter is applied to the OL signal to help reduce the occurrence of nuisance trips.

In redundant−supply systems, the sudden switchover to a supply of higher voltage potential is one more source of large current spikes. Due to the low impedance of filter capacitance under such high−frequency transients, these spikes are generally indistinguishable from true short−circuit faults to a hot swap controller. However, the TPS2398 and TPS2399 transient response addresses this issue by providing rapid circuit−breaker protection for load faults along with minimal interruption of power flow during supply switching events. The scope plots in Figure 26 illustrate how.

Figure 26 is a scope capture of the TPS2398/99 response in a diode−OR configuration to such an input transient event. (All waveforms are referenced to the −VIN pin.) In this example, the module is initially operating from a nominal −43 V supply (relative to the backplane supply return node). At the first major time division, another power supply, with an output of −48 V, is suddenly hot swapped into a secondary, or INB, input. This sudden voltage step is reflected in the −48V_RTN trace. On this board, the 5 V potential difference caused an 8 A spike, as shown by the I_{IN} trace (I_{IN} trace has been measured after the diode−OR). The GATE pin is rapidly pulled low, which quickly terminates the overload spike. However, it is quickly released, and seen to drive back to the pass FET ON−threshold, in this case, about 5 V. The resultant current−limit operation of the circuit is evidenced by the 2 A load on the B supply. Once supply current is flowing again, the filter capacitance is charged up to the new input supply level, seen here on the V_{DRAIN} trace. Once the capacitance is fully charged, the load demand rolls off to the operating 1 A level. As an added benefit, this event is transparent to the /PG signal, which remains asserted throughout the disturbance.

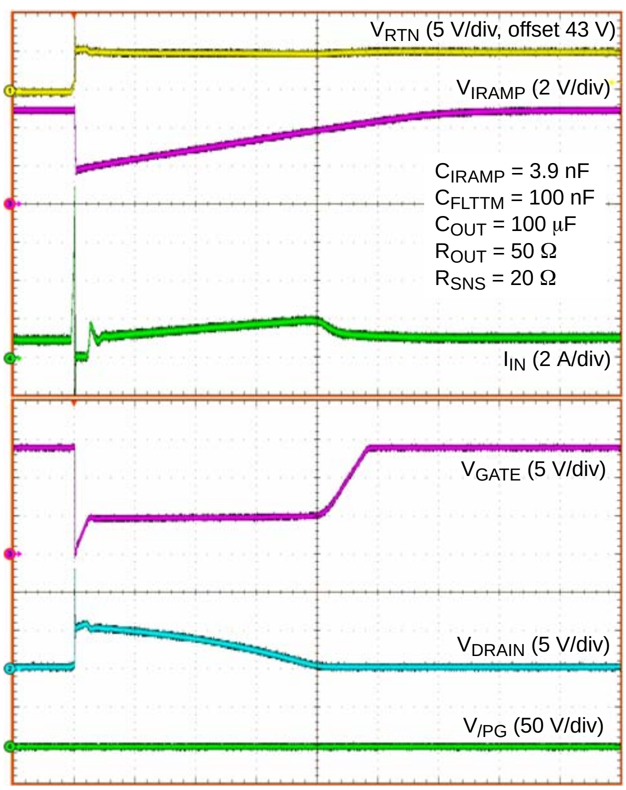


Figure 26. Input Transient Response

In order for downstream loads (bricks, etc.) to operate through the distribution bus transient, it is important to properly size the filtering capacitance to supply the needed energy during the OFF−time of the pass FET. In this example, once the RTN node jumps by 5 V higher than the original potential, about 6 V develops across the FET, indicating approximately a 1 V droop across the brick input. Therefore, due to the fast response of the TPS2398/99 devices, the 100 μF capacitor achieves excellent hold−up of the brick input voltage. Actual requirements depend heavily on the individual application. Whether the device turns back on in either current−ramp or current−limit mode depends in part on the size of the ramp capacitor (C_{IRAMP}) and the input capacitance of the pass FET. But in any case, the circuit turns back on in a controlled−current manner after rapidly clamping the potentially damaging spike.

Setting the Sense Resistor Value

Due to the current−limiting action of the internal LCA, the maximum allowable load current for an implementation is easily programmed by selecting the appropriate sense resistor value. The LCA acts to limit the sense voltage V_{ISENS} to its internal reference. Once the voltage at the IRAMP pin exceeds approximately 4 V, this limit is the clamp voltage, V_{REF_K}. Therefore, a maximum sense resistor value can be determined from Equation 1.

$$R_{SNS(MAX)} \leq \frac{V_{REF\_K(MIN)}}{I_{MAX}} \quad \text{(eq. 1)}$$

$$R_{SNS(MAX)} \leq \frac{33\ \text{mV}}{I_{MAX}}$$

Where:

- R_{SNS} is the sense resistor value,
- $V_{REF\_K(MIN)}$ is the minimum ref. clamp voltage, and
- I_{MAX} is the desired current limit.

When setting the sense resistor value, it is important to consider two factors, the minimum current that may be imposed by the TPS2398 or TPS2399, and the maximum load under normal operation of the module. For the first factor, the specification minimum clamp value is used, as seen in Equation 1. This method accounts for the tolerance in the sourced current limit below the typical level expected (40 mV / R_{SNS}). (The clamp measurement includes LCA input offset voltage; therefore, this offset does not have to be factored into the current limit again.) Second, if the load current varies over a range of values under normal operating conditions, then the maximum load level must be allowed for by the value of R_{SNS}. One example of this is when the load is a switching converter, or brick, which draws higher input current, for a given power output, when the distribution bus is at the low end of its operating range, with decreasing draw at higher supply voltages. To avoid current−limit operation under normal loading, some margin should be designed in between this maximum anticipated load and the minimum current limit level, or $I_{MAX} > I_{LOAD(MAX)}$, for Equation 1.

For example, using a 20 mΩ sense resistor for a nominal 1 A load application provides a minimum of 650 mA of overhead for load variance/margin. Typical bulk capacitor charging current during turn−on is 2 A (40 mV / 20 mΩ).

Setting the Inrush Slew Rate

The TPS2398 and TPS2399 devices enable user−programming of the maximum current slew rate during load start−up events. A capacitor tied to the IRAMP pin (C_2 in the typical application diagram) controls the di/dt rate. Once the sense resistor value has been established, a value for ramp capacitor C_{IRAMP}, in microfarads, can be determined from Equation 2.

$$C_{IRAMP} = \frac{11}{100 \cdot R_{SNS} \cdot \left(\frac{di}{dt}\right)_{MAX}} \quad \text{(eq. 2)}$$

Where:

- R_{SENSE} is in ohms, and
- $\left(\frac{di}{dt}\right)_{MAX}$ is the desired maximum slew rate, in amperes/second.

For example, if the desired slew rate for the typical application shown is 1500 mA/ms, the calculated value for C_{IRAMP} is about 3.7 nF. Selecting the next larger standard value of 3.9 nF (as shown in the diagram) provides some margin for capacitor and sense resistor tolerances.

As described earlier in this section, the TPS2398 and TPS2399 initiate ramp capacitor charging, and consequently, load current di/dt at a reduced rate. This reduced rate applies until the voltage on the IRAMP pin is about 0.5 V. The maximum di/dt rate, as set by Equation 2, is effective once the device has switched to the 10 μA charging source.

Setting the Fault Timing Capacitor

The fault timeout period is established by the value of the capacitor connected to the FLTTIME pin, C_{FLTTM}. The timeout period permits riding out spurious current glitches and surges that may occur during operation of the system, and prevents indefinite sourcing into faulted loads swapped into a live system. However, to ensure smooth voltage ramping under all conditions of load capacitance and input supply potential, the minimum timeout should be set to accommodate these system variables. To do this, a rough estimate of the maximum voltage ramp time for a completely discharged plug−in card provides a good basis for setting the minimum timer delay.

Due to the three−phase nature of the load current at turn−on, the load voltage ramp potentially has three distinct phases (compare Figures 3 and 4). This profile depends on the relative values of load capacitance, input dc potential, maximum current limit and other factors. The first two phases are characterized by the two different slopes of the current ramp; the third phase, if required for bulk capacitance charging, is the constant−current charging at I_{MAX}. Considering the two current ramp phases to be one period at an average di/dt simplifies calculation of the required timing capacitor.

For the TPS2398 and TPS2399, the typical duration of the soft−start ramp period, t_{SS}, is given by Equation 3.

$$t_{SS} = 1183 \cdot C_{IRAMP} \qquad \text{(eq. 3)}$$

Where:

- t_{SS} is the soft−start period in ms, and
- C_{IRAMP} is given in μF

During this current ramp period, the load voltage magnitude which is attained is estimated by Equation 4.

$$V_{LSS} = \frac{i_{AVG}}{2 \cdot C_{LOAD} \cdot C_{RAMP} \cdot 100 \cdot R_{SNS}} \cdot {t_{SS}}^2 \qquad \text{(eq. 4)}$$

Where:

- V_{LSS} is the load voltage reached during soft−start,
- i_{AVG} is 3.38 μA for the TPS2398 and TPS2399,
- C_{LOAD} is the amount of the load capacitance, and
- t_{SS} is the soft−start period, in seconds

The quantity i_{AVG} in Equation 4 is a weighted average of the two charge currents applied to C_{IRAMP} during turn−on, considering the typical output values.

If the result of Equation 4 is larger than the maximum input supply value, then the load can be expected to charge completely during the inrush slewing portion of the insertion event. However, if this voltage is less than the maximum supply input, $V_{IN(MAX)}$, the HSPM transitions to the constant−current charging of the load. The remaining amount of time required at I_{MAX} is determined from Equation 5.

$$t_{CC} = \frac{C_{LOAD} \cdot \left(V_{IN(MAX)} - V_{LSS}\right)}{\frac{V_{REF\_K(MIN)}}{R_{SNS}}} \qquad \text{(eq. 5)}$$

Where:

- t_{CC} is the constant−current voltage ramp time, in seconds, and
- $V_{REF\_K(MIN)}$ is the minimum clamp voltage, 33 mV.

With this information, the minimum recommended value timing capacitor C_{FLTTM} can be determined. The delay time needed will be either a time t_{SS2} or the sum of t_{SS2} and t_{CC}, according to the estimated time to charge the load. The quantity t_{SS2} is the duration of the normal rate current ramp period, and is given by Equation 6.

$$t_{SS2} = 0.35 \cdot C_{RAMP} \qquad \text{(eq. 6)}$$

Where:

- C_{RAMP} is given in microfarads

Since fault timing is generated by the constant−current charging of C_{FLTTM}, the capacitor value is determined from either Equation 7 or 8, as appropriate.

$$C_{FLTTM(MIN)} = \frac{55 \cdot t_{SS2}}{3.75} \qquad \text{(eq. 7)}$$

$$C_{FLTTM(MIN)} = \frac{55 \cdot \left(t_{SS2} + t_{CC}\right)}{3.75} \qquad \text{(eq. 8)}$$

Where:

- $C_{FLTTM(MIN)}$ is the recommended capacitor value, in microfarads,
- t_{SS2} is the result of Equation 6, in seconds, and
- t_{CC} is the result of Equation 5, in seconds.

Continuing the typical application example, using a 100 μF input capacitor (C_{LOAD}), Equations 3 and 4 estimate the load voltage ramping to approximately −46 V during the soft−start period. If the module should operate down to −72 V input supply, approximately another 1.58 ms of constant−current charging may be required. Therefore, Equations 6 and 8 are used to determine $C_{FLTTM(MIN)}$, and the result of 43 nF suggests the 47 nF standard value.

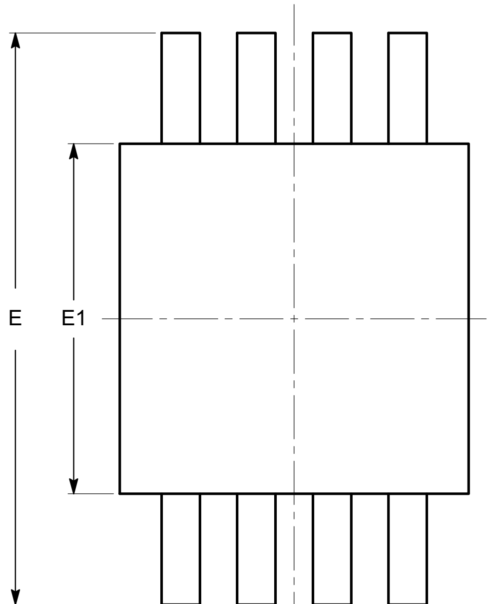
ORDERING INFORMATION

Device	Marking	Fault Operation	Package	Shipping†
TPS2398DMT7G	2398	Latch off	MSOP−8 (Pb−Free)	3000 / Tape & Reel
TPS2399DMT7G	2399	Periodically retry		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

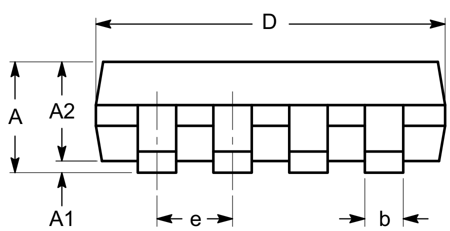
MSOP 8, 3x3
CASE 846AD−01
ISSUE O

DATE 19 DEC 2008

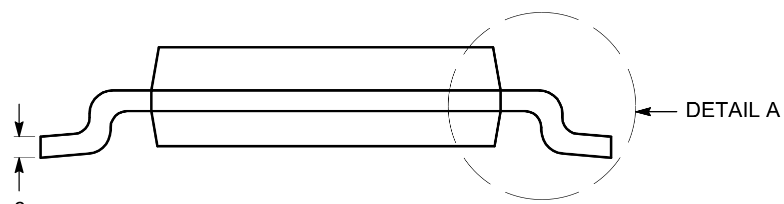


TOP VIEW

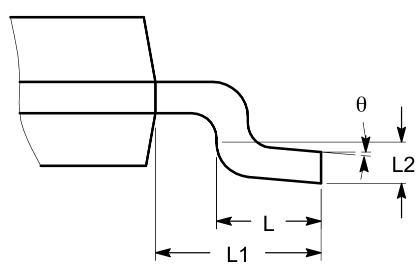
SYMBOL	MIN	NOM	MAX
A			1.10
A1	0.05	0.10	0.15
A2	0.75	0.85	0.95
b	0.22		0.38
c	0.13		0.23
D	2.90	3.00	3.10
E	4.80	4.90	5.00
E1	2.90	3.00	3.10
e		0.65 BSC	
L	0.40	0.60	0.80
L1		0.95 REF	
L2		0.25 BSC	
θ	0º		6º



SIDE VIEW



END VIEW



DETAIL A

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-187.

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