PIC32MX1XX/2XX 28/36/44-pin Family Silicon Errata and Data Sheet Clarification

The PIC32MX1XX/2XX 28/36/44-pin family devices that you have received conform functionally to the current Device Data Sheet (DS60001168**K**), except for the anomalies described in this document.

The errata described in this document will be addressed in future revisions of the PIC32MX1XX/2XX 28/36/44-pin silicon.

Note: The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1 through Table 4. The last column of each table represents the latest silicon revision for the devices listed. The silicon issues are summarized in Table 5.

Data Sheet clarifications and corrections start on page 12, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® X IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB X IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB X IDE project.
3. Configure the MPLAB X IDE project for the appropriate device and hardware debugger.
4. Select *Window > Dashboard*, and then click the **Refresh Debug Tool Status** icon ( ).
5. The part number and the Device and Revision ID values appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The Device and Revision ID values for the various silicon revisions are provided in Table 1 through Table 4.

TABLE 1: SILICON DEVREV VALUES FOR DEVICES WITH 16/32 KB FLASH

Part Number	Device ID(1)	Revision ID for Silicon Revision(1)	
		A0	A1
PIC32MX110F016B	0x4A07053	0x0	0x1
PIC32MX110F016C	0x4A09053		
PIC32MX110F016D	0x4A0B053		
PIC32MX210F016B	0x4A01053		
PIC32MX210F016C	0x4A03053		
PIC32MX210F016D	0x4A05053		
PIC32MX120F032B	0x4A06053		
PIC32MX120F032C	0x4A08053		
PIC32MX120F032D	0x4A0A053		
PIC32MX220F032B	0x4A00053		
PIC32MX220F032C	0x4A02053		
PIC32MX220F032D	0x4A04053		

Note 1: Refer to the **"Memory Organization"** and **"Special Features"** chapters in the current Device Data Sheet (DS60001168**J**) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON DEVREV VALUES FOR DEVICES WITH 64/128 KB FLASH

Part Number	Device ID(1)	Revision ID for Silicon Revision(1)		
		A0	A1	A3
PIC32MX130F064B	0x4D07053	0x0	0x1	0x3
PIC32MX130F064C	0x4D09053			
PIC32MX130F064D	0x4D0B053			
PIC32MX230F064B	0x4D01053			
PIC32MX230F064C	0x4D03053			
PIC32MX230F064D	0x4D05053			
PIC32MX150F128B	0x4D06053			—
PIC32MX150F128C	0x4D08053			
PIC32MX150F128D	0x4D0A053			
PIC32MX250F128B	0x4D00053			
PIC32MX250F128C	0x4D02053			
PIC32MX250F128D	0x4D04053			

Note 1: Refer to the **"Memory Organization"** and **"Special Features"** chapters in the current Device Data Sheet (DS60001168**J**) for detailed information on Device and Revision IDs for your specific device.

TABLE 3: SILICON DEVREV VALUES FOR DEVICES WITH 256 KB FLASH AND 64 KB RAM

Part Number	Device ID(1)	Revision ID for Silicon Revision(1)	
		A1	A2
PIC32MX170F256B	0x6610053	0x1	0x2
PIC32MX170F256D	0x661A053		
PIC32MX270F256B	0x6600053		
PIC32MX270F256D	0x660A053		
PIC32MX270F256DB	0x660C053		

Note 1: Refer to the **"Memory Organization"** and **"Special Features"** chapters in the current Device Data Sheet (DS60001168**J**) for detailed information on Device and Revision IDs for your specific device.

TABLE 4: SILICON DEVREV VALUES FOR DEVICES WITH 256 KB FLASH AND 16 KB RAM

Part Number	Device ID(1)	Revision ID for Silicon Revision(1)
		A0
PIC32MX130F256B	0x6703053	0x0
PIC32MX130F256D	0x6705053	
PIC32MX230F256B	0x6700053	
PIC32MX230F256D	0x6702053	

Note 1: Refer to the **"Memory Organization"** and **"Special Features"** chapters in the current Device Data Sheet (DS60001168**J**) for detailed information on Device and Revision IDs for your specific device.

TABLE 5: SILICON ISSUE SUMMARY

Module	Feature	Item	Issue Summary	Affected Device					
				Flash Memory (KB)	Data Memory (KB)	Silicon Revision			
						A0	A1	A2	A3
Voltage Regulator	BOR	1.	Device may not exit Brown-out Reset (BOR) state if a BOR event occurs.	16/32	4/8	X		—	—
				64	16	X		—	
				128	32	X		—	—
				256	16		—	—	—
				256	64	—			—
Oscillator	Clock Switch	2.	If a Fail-Safe Clock Monitor (FSCM) event occurs when Primary Oscillator (POSC) mode is used, firmware clock switch requests to switch from FRC mode will fail.	16/32	4/8	X	X	—	—
				64	16	X	X	—	X
				128	32	X	X	—	—
				256	16	X	—	—	—
				256	64	—	X	X	—
I^2C	Slave Mode	3.	The I^2C module does not respond to address 0x78 when the STRICT and A10M bits are cleared in the I2CxCON register.	16/32	4/8	X	X	—	—
				64	16	X	X	—	X
				128	32	X	X	—	—
				256	16	X	—	—	—
				256	64	—	X	X	—
USB	UIDLE Interrupt	4.	UIDLE interrupts cease if the UIDLE interrupt flag is cleared.	16/32	4/8	X	X	—	—
				64	16	X	X	—	X
				128	32	X	X	—	—
				256	16	X	—	—	—
				256	64	—	X	X	—
ADC	N/A	5	The DNL parameter of the ADC module is not within the published data sheet specifications when the ADC module is operating at maximum conversion rate.	16/32	4/8	X	X	—	—
				64	16	X	X	—	X
				128	32	X	X	—	—
				256	16	X	—	—	—
				256	64	—	X	X	—
ADC	CTMU Calibration	6.	Open selection for Channel 0 positive input is not functional.	16/32	4/8	X	X	—	—
				64	16			—	
				128	32			—	—
				256	16		—	—	—
				256	64	—			—

Legend: An ‘X’ indicates the issue is present in this revision of silicon;
shaded cells with an Em dash (‘—’) indicate that this silicon revision does not exist for this issue;
blank cells indicate an issue has been corrected in this revision of silicon.

TABLE 5: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item	Issue Summary	Affected Device					
				Flash Memory (KB)	Data Memory (KB)	Silicon Revision			
						A0	A1	A2	A3
ADC	Conversion Trigger from INT0 Interrupt	7.	The ADC module conversion triggers occur on the rising edge of the INT0 signal even when INT0 is configured to generate an interrupt on the falling edge.	16/32	4/8	X	X	—	—
				64	16	X	X	—	X
				128	32	X	X	—	—
				256	16	X	—	—	—
				256	64	—	X	X	—
Parallel Master Port (PMP)	Address Pins	8.	When the Parallel Master Port (PMP) module is enabled, address pins cannot be used as GPIO output pins.	16/32	4/8	X	X	—	—
				64	16	X	X	—	X
				128	32	X	X	—	—
				256	16	X	—	—	—
				256	64	—	X	X	—
I/O Ports	RA0 and RA1 Pins	9.	When I2C1 is enabled, all digital output-only functions and all analog functions on pins RA0 and RA1 do not function correctly.	16/32	4/8	X	X	—	—
				64	16	X	X	—	
				128	32	X	X	—	—
				256	16		—	—	—
				256	64	—			—
CPU	Data Write to a Peripheral	10.	A data write operation by the CPU to a peripheral may be repeated if an interrupt occurs during initial write operation.	16/32	4/8	X	X	—	—
				64	16	X	X	—	
				128	32	X	X	—	—
				256	16		—	—	—
				256	64	—			—
Oscillator	Clock Out	11.	A clock signal is present on the CLKO pin, regardless of the clock source and setting of the CLKO Enable Configuration bit, during a Power-on Reset (POR) condition.	16/32	4/8	X	X	—	—
				64	16	X	X	—	X
				128	32	X	X	—	—
				256	16	X	—	—	—
				256	64	—	X	X	—
Input Capture	Idle Mode and Sleep Mode	12.	All input capture modes selectable by ICM<2:0>, with the exception of Interrupt-only mode, will not work when the CPU enters Idle mode or Sleep mode.	16/32	4/8	X	X	—	—
				64	16	X	X	—	X
				128	32	X	X	—	—
				256	16	X	—	—	—
				256	64	—	X	X	—

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blank cells indicate an issue has been corrected in this revision of silicon.

TABLE 5: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item	Issue Summary	Affected Device					
				Flash Memory (KB)	Data Memory (KB)	Silicon Revision			
						A0	A1	A2	A3
Watchdog Timer (WDT)	Windowed Mode	13.	The Watchdog Timer may issue a reset even if the user tries to clear the module within the allowed window.	16/32	4/8	X	X	—	—
				64	16	X	X	—	X
				128	32	X	X	—	—
				256	16	X	—	—	—
				256	64	—	X	X	—
Non-5V Tolerant Pins	Pull-ups	14.	Internal pull-up resistors may not guarantee a logical '1' on non-5V tolerant pins when they are configured as digital inputs.	16/32	4/8	X	X	—	—
				64	16	X	X	—	
				128	32	X	X	—	—
				256	16		—	—	—
				256	64	—			—
5V Tolerant Pins	Pull-ups	15.	Internal pull-up resistors may not guarantee a logical '1' on 5V tolerant pins when they are configured as digital inputs.	16/32	4/8	X	X	—	—
				64	16	X	X	—	X
				128	32	X	X	—	—
				256	16	X	—	—	—
				256	64	—	X	X	—
I/O Ports	Open Drain	16.	The Open Drain selection (ODCx) on I/O port pins is not available when the pin is configured for anything other than a standard port output.	16/32	4/8	X	X	—	—
				64	16	X	X	—	
				128	32	X	X	—	—
				256	16		—	—	—
				256	64	—			—
I/O Ports	RB5 and RB6 Pins	17.	When the I2C2 module is enabled, all digital output-only functions and all analog functions on pins RB5 and RB6 do not function correctly.	16/32	4/8	X	X	—	—
				64	16	X	X	—	
				128	32	X	X	—	—
				256	16		—	—	—
				256	64	—			—
I/O Ports	Analog Inputs	18.	Certain functions are not available when using PGED3/PGEC3 or PGED4/PGEC4 while in Debug mode.	16/32	4/8	X	X	—	—
				64	16	X	X	—	X
				128	32	X	X	—	—
				256	16	X	—	—	—
				256	64	—	X	X	—

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blank cells indicate an issue has been corrected in this revision of silicon.

TABLE 5: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item	Issue Summary	Affected Device					
				Flash Memory (KB)	Data Memory (KB)	Silicon Revision			
						A0	A1	A2	A3
UART	Synchronization	19.	On a RX FIFO overflow, shift registers stop receiving data, which causes the UART to lose synchronization.	16/32	4/8	X	X	—	—
				64	16	X	X	—	X
				128	32	X	X	—	—
				256	16	X	—	—	—
				256	64	—	X	X	—
Timer1	Interrupts	20.	Timer1 will not generate interrupts with an external asynchronous clock input and prescaler other than 1:1.	16/32	4/8	X	X	—	—
				64	16	X	X	—	X
				128	32	X	X	—	—
				256	16	X	—	—	—
				256	64	—	X	X	—
Flash Memory	Write Protection	21.	The Program Write Protection (PWP) bits are not enabled unless the Boot Write Protect (BWP) bit is also enabled.	16/32	4/8	X	X	—	—
				64	16	X	X	—	X
				128	32	X	X	—	—
				256	16	X	—	—	—
				256	64	—	X	X	—
Flash Memory	Write Protection	22.	When enabled, the Boot Write Protect (BWP) bit also protects and overlaps the first page of user program space below 0x0400 in addition to the boot segment.	16/32	4/8	X	X	—	—
				64	16	X	X	—	
				128	32	X	X	—	—
				256	16		—	—	—
				256	64	—			—
Flash Memory	Write Protection	23.	The Program Write Protection (PWP) bit field is off by one page relative to the definition in the data sheet.	16/32	4/8	X	X	—	—
				64	16	X	X	—	
				128	32	X	X	—	—
				256	16		—	—	—
				256	64	—			—
Flash Memory	Write Protection	24.	Attempts to protect the entire Flash memory using the following values, will result in no pages being protected.	16/32	4/8	X	X	—	—
				64	16	X	X	—	
				128	32	X	X	—	—
				256	16		—	—	—
				256	64	—			—

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shaded cells with an Em dash (‘—’) indicate that this silicon revision does not exist for this issue;
blank cells indicate an issue has been corrected in this revision of silicon.

TABLE 5: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item	Issue Summary	Affected Device					
				Flash Memory (KB)	Data Memory (KB)	Silicon Revision			
						A0	A1	A2	A3
Power-Saving Modes	Idle	25.	On exit from Sleep mode, the SLEEP and IDLE status bits in the RCON register are being set.	16/32	4/8	X	X	—	—
				64	16	X	X	—	X
				128	32	X	X	—	—
				256	16	X	—	—	—
				256	64	—	X	X	—
CTMU	Temperature Measurement	26.	The CTMU internal temperature sensing diode does not function for VDD/AVDD operating voltages that are less than 2.5V.	16/32	4/8	X	X	—	—
				64	16	X	X	—	
				128	32	X	X	—	—
				256	16		—	—	—
				256	64	—	X	X	—
I^2C	Slave Addresses	27.	When the I^2C module is operating as a Slave, some reserved bus addresses may be Acknowledged (ACKed) when they should be not Acknowledged (NAKed).	16/32	4/8	X	X	—	—
				64	16	X	X	—	
				128	32	X	X	—	—
				256	16		—	—	—
				256	64	—	X	X	—
Bus Matrix	Flash Size	28.	The Flash Memory Size register (BMXPFMSZ) was not programmed with the correct value.	16/32	4/8	Date code pre-1750			
				64	16				
				128	32				
				256	16				
				256	64				

Legend: An 'X' indicates the issue is present in this revision of silicon;
shaded cells with an Em dash ('—') indicate that this silicon revision does not exist for this issue;
blank cells indicate an issue has been corrected in this revision of silicon.

Silicon Errata Issues

Note 1: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. The table provided in each issue indicates which issues exist for a particular revision of silicon based on Flash memory size.

2: The following applies to the Affected Silicon Revision tables in each silicon issue:

- An 'X' indicates the issue is present in this revision of silicon
- Shaded cells with an Em dash ('—') indicate that this silicon revision does not exist for this issue
- Blank cells indicate an issue has been corrected or does not exist in this revision of silicon

1. Module: Voltage Regulator

Device may not exit the Brown-out Reset (BOR) state if a BOR event occurs.

Work arounds

Work around 1:

VDD must remain within the published specification (see parameter DC10 of the device data sheet).

Work around 2:

Reset the device by providing the Power-on Reset (POR) condition.

Affected Silicon Revisions

Device Flash Memory (KB)	Data Memory (KB)	Device Silicon Revision					
		A0	A1	A2	A3		
16/32	4/8	X		—	—		
64	16	X		—			
128	32	X		—	—		
256	16		—	—	—		
256	64	—			—		

2. Module: Oscillator

If the Primary Oscillator (POSC) mode is implemented and a Fail-Safe Clock Monitor (FSCM) event occurs (failure of the external primary clock), the internal clock source will switch to the FRC oscillator. Subsequent firmware clock switch requests from the FRC oscillator to other clock sources will fail and the device will continue to execute on the FRC oscillator. On repair of the external clock source and a power-on state, the device will resume operation with the primary oscillator clock source.

Work around

None.

Affected Silicon Revisions

Device Flash Memory (KB)	Data Memory (KB)	Device Silicon Revision					
		A0	A1	A2	A3		
16/32	4/8	X	X	—	—		
64	16	X	X	—	X		
128	32	X	X	—	—		
256	16	X	—	—	—		
256	64	—	X	X	—		

3. Module: I²C

The slave address, 0x78, is one of a group of reserved addresses. It is used as the upper byte of a 10-bit address when 10-bit addressing is enabled. The I²C module control register allows the programmer to enable both 10-bit addressing and strict enforcement of reserved addressing, with the A10M and STRICT bits, respectively. When both bits are cleared, the device should respond to the reserved address 0x78, but it does not.

Work around

None.

Affected Silicon Revisions

Device Flash Memory (KB)	Data Memory (KB)	Device Silicon Revision					
		A0	A1	A2	A3		
16/32	4/8	X	X	—	—		
64	16	X	X	—	X		
128	32	X	X	—	—		
256	16	X	—	—	—		
256	64	—	X	X	—		

4. Module: USB

If the bus has been idle for more than 3 ms, the UIDLE interrupt flag is set. If software clears the interrupt flag and the bus remains idle, the UIDLE interrupt flag will not be set again.

Work around

Software can leave the UIDLE bit set until it has received some indication of bus resumption (i.e., Resume, Reset, SOF, or Error).

Note:	Resume and Reset are the only interrupts that should be following UIDLE assertion. If the UIDLE bit is set, it should be okay to suspend the USB module (as long as this code is protected by the GUARD and/or ACTPEND logic). This will require software to clear the UIDLE interrupt enable bit to exit the USB ISR (if using interrupt driven code).

Affected Silicon Revisions

Device Flash Memory (KB)	Data Memory (KB)	Device Silicon Revision					
		A0	A1	A2	A3		
16/32	4/8	X	X	—	—		
64	16	X	X	—	X		
128	32	X	X	—	—		
256	16	X	—	—	—		
256	64	—	X	X	—		

5. Module: ADC

If the ADC module is configured to operate at a maximum conversion rate of 1.1 Msps, missing codes are possible every 2^5 codes and the DNL parameter will not be within the published specification.

Work around

Configure the ADC module to operate for a maximum conversion rate of 500 ksps.

Affected Silicon Revisions

Device Flash Memory (KB)	Data Memory (KB)	Device Silicon Revision					
		A0	A1	A2	A3		
16/32	4/8	X	X	—	—		
64	16	X	X	—	X		
128	32	X	X	—	—		
256	16	X	—	—	—		
256	64	—	X	X	—		

6. Module: ADC

If the ADC module is used in conjunction with the CTMU module in Absolute Capacitive/Time Measurement mode, Channel 0 positive input must remain open (CH0SA<3:0> = 1111 or CH0SB<3:0> = 1111) during the calibration step. However, open selection for Channel 0 positive input is not functional and connects this input to AVSS.

Work around

Connect the ADC module to any unused pin and perform the CTMU calibration step. This connection will add a small amount of additional capacitance, but will have minimal impact on overall measurements.

Affected Silicon Revisions

Device Flash Memory (KB)	Data Memory (KB)	Device Silicon Revision					
		A0	A1	A2	A3		
16/32	4/8	X	X	—	—		
64	16			—			
128	32			—	—		
256	16		—	—	—		
256	64	—			—		

7. Module: ADC

When the ADC module is configured to start conversion on an external interrupt (SSRC<2:0> = 001), the start of conversion always occurs on a rising edge detected at the INT0 pin, even when the INT0 pin has been configured to generate an interrupt on a falling edge (INT0EP = 0).

Work around

Generate ADC conversion triggers on the rising edge of the INT0 signal.

Alternately, use external circuitry to invert the signal appearing at the INT0 pin, so that a falling edge of the input signal is detected as a rising edge by the INT0 pin.

Affected Silicon Revisions

Device Flash Memory (KB)	Data Memory (KB)	Device Silicon Revision					
		A0	A1	A2	A3		
16/32	4/8	X	X	—	—		
64	16	X	X	—	X		
128	32	X	X	—	—		
256	16	X	—	—	—		
256	64	—	X	X	—		

8. Module: Parallel Master Port (PMP)

If the PMP module is enabled, any pin with a PMP addressing capability (PMAx) cannot be used as a general purpose output pin, even when the corresponding PTEN<10:0> bit in the PMAEN register is cleared. All other functionality on these pins, including GPIO input functionality is not affected.

Work around

To use a GPIO pin as an output when this pin is shared with PMP addressing functionality and PMP is enabled, do the following:

1. Enable PMP addressing by setting the corresponding PTEN<10:0> bit in the PMAEN register.
2. Instead of using corresponding LATx registers to output GPIO data, use the PMADDR register.

Affected Silicon Revisions

Device Flash Memory (KB)	Data Memory (KB)	Device Silicon Revision					
		A0	A1	A2	A3		
16/32	4/8	X	X	—	—		
64	16	X	X	—	X		
128	32	X	X	—	—		
256	16	X	—	—	—		
256	64	—	X	X	—		

9. Module: I/O Ports

When I2C1 is enabled, all digital output-only functions and all analog functions on pin RA0 and RA1 do not function correctly.

Digital output VOH/IOH does not meet the specification in the data sheet and analog signal input loading increases with an increase in applied voltage on any enabled analog function on RA0/RA1. If I2C1 is enabled, any analog or digital output-only function enabled on RA0/RA1 will also cause a corresponding 40 mA/pin increase in IDD.

Work around

Disable slew rate control of the I2C1 module by setting the DISSLW bit (I2C1CON<9>) = 1.

Affected Silicon Revisions

Device Flash Memory (KB)	Data Memory (KB)	Device Silicon Revision					
		A0	A1	A2	A3		
16/32	4/8	X	X	—	—		
64	16	X	X	—			
128	32	X	X	—	—		
256	16		—	—	—		
256	64	—			—		

10. Module: CPU

During normal operation, if a CPU write operation is interrupted by an incoming interrupt, it should be aborted (not completed) and resumed after the interrupt is serviced. However, some of these write operations may not be aborted, resulting in a double write to peripherals by the CPU (the first write during the interrupt and the second write after the interrupt is serviced).

Work around

Most peripherals are not affected by this issue, as a double write will not have a negative impact. However, the following communication peripherals will double-send data if their respective transmit buffers are written twice: SPI, I^2C, UART, and PMP. To avoid double transmission of data, utilize DMA to transfer data to these peripherals or disable interrupts while writing to these peripherals.

Affected Silicon Revisions

Device Flash Memory (KB)	Data Memory (KB)	Device Silicon Revision					
		A0	A1	A2	A3		
16/32	4/8	X	X	—	—		
64	16	X	X	—			
128	32	X	X	—	—		
256	16		—	—	—		
256	64	—			—		

11. Module: Oscillator

A clock signal is present on the CLKO pin, regardless of the clock source and setting of the CLKO Enable Configuration bit, OSCIOFNC (DEVCFG1<10>), during a Power-on Reset (POR) condition.

Work around

Do not connect the CLKO pin to a device that would be adversely affected by rapid pin toggling or a frequency other than that defined by the oscillator configuration. Do not use the CLKO pin as an input if the device connected to the CLKO pin would be adversely affected by the pin driving a signal out.

Affected Silicon Revisions

Device Flash Memory (KB)	Data Memory (KB)	Device Silicon Revision					
		A0	A1	A2	A3		
16/32	4/8	X	X	—	—		
64	16	X	X	—	X		
128	32	X	X	—	—		
256	16	X	—	—	—		
256	64	—	X	X	—		

12. Module: Input Capture

All input capture modes selectable by ICM<2:0>, with the exception of Interrupt-only mode, will not work when the CPU enters Idle or Sleep mode.

Work around

Configure the Input Capture module for Interrupt-only mode (ICM<2:0> = 111) when the CPU is in Sleep or Idle mode.

Affected Silicon Revisions

Device Flash Memory (KB)	Data Memory (KB)	Device Silicon Revision					
		A0	A1	A2	A3		
16/32	4/8	X	X	—	—		
64	16	X	X	—	X		
128	32	X	X	—	—		
256	16	X	—	—	—		
256	64	—	X	X	—		

13. Module: Watchdog Timer (WDT)

When the Watchdog Timer module is used in Windowed mode, the module may issue a reset even if the user tries to clear the module within the allowed window.

Work around

None.

Affected Silicon Revisions

Device Flash Memory (KB)	Data Memory (KB)	Device Silicon Revision					
		A0	A1	A2	A3		
16/32	4/8	X	X	—	—		
64	16	X	X	—	X		
128	32	X	X	—	—		
256	16	X	—	—	—		
256	64	—	X	X	—		

14. Module: Non-5V Tolerant Pins

When internal pull-ups are enabled on non-5V tolerant pins, the level as measured on the pin and available to external device inputs may not exceed the minimum value of V_{IH}, and therefore qualify as a logic “high”. However, with respect to the PIC32 device, as long as $V_{DD} \geq 3V$ and the load does not exceed -50 µA, the internal pull-ups are guaranteed to be recognized as a logic “high” internally to the device.

Work around

It is recommend to only use external pull-ups:

- To guarantee a logic “high” for external logic input circuits outside of the PIC32 device
- For PIC32 device inputs, if the external load exceeds -50 µA or $V_{DD} < 3V$

Affected Silicon Revisions

Device Flash Memory (KB)	Data Memory (KB)	Device Silicon Revision					
		A0	A1	A2	A3		
16/32	4/8	X	X	—	—		
64	16	X	X	—			
128	32	X	X	—	—		
256	16		—	—	—		
256	64	—			—		

15. Module: 5V Tolerant Pins

When internal pull-ups are enabled on 5V tolerant pins, the level as measured on the pin and available to external device inputs may not exceed the minimum value of V_{IH}, and therefore qualify as a logic “high”. However, with respect to the PIC32 device, as long as $V_{DD} \geq 3V$ and the load does not exceed -50 µA, the internal pull-ups are guaranteed to be recognized as a logic “high” internally to the device.

Work around

It is recommend to only use external pull-ups:

- To guarantee a logic “high” for external logic input circuits outside of the PIC32 device
- For PIC32 device inputs, if the external load exceeds -50 µA or $V_{DD} < 3V$

Affected Silicon Revisions

Device Flash Memory (KB)	Data Memory (KB)	Device Silicon Revision					
		A0	A1	A2	A3		
16/32	4/8	X	X	—	—		
64	16	X	X	—	X		
128	32	X	X	—	—		
256	16	X	—	—	—		
256	64	—	X	X	—		

16. Module: I/O Ports

The Open Drain selection (ODCx) on I/O port pins is not available when the pin is configured for anything other than a standard port output. In addition, the Open Drain feature is not available for dedicated or remappable Peripheral Pin Select (PPS) output features.

Work around

None.

Affected Silicon Revisions

Device Flash Memory (KB)	Data Memory (KB)	Device Silicon Revision					
		A0	A1	A2	A3		
16/32	4/8	X	X	—	—		
64	16	X	X	—			
128	32	X	X	—	—		
256	16		—	—	—		
256	64	—			—		

17. Module: I/O Ports

When the I2C2 module is enabled, all digital output-only functions and all analog functions on pins RB5 and RB6 do not function correctly.

Digital output (V_{OH}/I_{OH}) does not meet the specifications in the data sheet, and analog signal input loading increases with an increase in applied voltage on any enabled analog function on the RB5 and RB6 pins. If the I2C2 is enabled, any analog or digital output-only function enabled on the RB5 and RB6 pins will also cause a corresponding ~40 mA/pin increase in I_{DD}.

Work around

Disable the I2C2 module slew rate by setting the DISSLW bit in the I2C2CON register = 1.

Affected Silicon Revisions

Device Flash Memory (KB)	Data Memory (KB)	Device Silicon Revision					
		A0	A1	A2	A3		
16/32	4/8	X	X	—	—		
64	16	X	X	—			
128	32	X	X	—	—		
256	16		—	—	—		
256	64	—			—		

18. Module: I/O Ports

Certain functions are not available when using PGED3/PGEC3 or PGED4/PGEC4 while in Debug mode.

When using the PGED3/PGEC3 pins while debugging, these functions are not available:

- $V_{REF}+/CV_{REF}+$/AN0/C3INC
- $V_{REF}-/CV_{REF}-$/AN1.

On 44-pin devices, when using the PGED4/PGEC4 pins while debugging, these functions are not available:

- AN6
- AN7

Work around

Use either the PGED1/PGEC1 pin pair or the PGED2/PGEC2 pin pair for debugging.

Affected Silicon Revisions

Device Flash Memory (KB)	Data Memory (KB)	Device Silicon Revision					
		A0	A1	A2	A3		
16/32	4/8	X	X	—	—		
64	16	X	X	—	X		
128	32	X	X	—	—		
256	16	X	—	—	—		
256	64	—	X	X	—		

19. Module: UART

During a RX FIFO overflow condition, the shift register stops receiving data. This causes the UART to lose synchronization with the serial data stream. The only way to recover from this is to turn the UART OFF and ON until it synchronizes. This could require several OFF/ON sequences.

Work arounds

Work around 1:

Avoid the RX overrun condition by ensuring that the UARTx module has a high enough interrupt priority such that other peripheral interrupt processing latencies do not exceed the time to overrun the UART RX buffer based on the application baud rate. Alternately or in addition to, set the URXISEL bits in the UxSTA register to generate an earlier RX interrupt based on RX FIFO fill status to buy more time for interrupt latency processing requirements.

Work around 2:

If avoiding RX FIFO overruns is not possible, implement a ACK/NAK software handshake protocol to repeat lost packet transfers after restoring UART synchronization.

Affected Silicon Revisions

Device Flash Memory (KB)	Data Memory (KB)	Device Silicon Revision					
		A0	A1	A2	A3		
16/32	4/8	X	X	—	—		
64	16	X	X	—	X		
128	32	X	X	—	—		
256	16	X	—	—	—		
256	64	—	X	X	—		

20. Module: Timer1

Timer1 will not generate interrupts with an external asynchronous clock input and prescaler other than 1:1.

Work around

With external clock asynchronous mode, use 1:1 prescaler mode with a software timer overflow variable to keep track of desired equivalent > 1:1 prescaler setting. Alternately, use external synchronous clock mode if this is an option for the application.

Affected Silicon Revisions

Device Flash Memory (KB)	Data Memory (KB)	Device Silicon Revision					
		A0	A1	A2	A3		
16/32	4/8	X	X	—	—		
64	16	X	X	—	X		
128	32	X	X	—	—		
256	16	X	—	—	—		
256	64	—	X	X	—		

21. Module: Flash Memory

The Program Write Protection (PWP) bits (DEVCFG0<18:10>) are not enabled unless the Boot Write Protect (BWP) bit (DEVCFG0<24> is also enabled (i.e., = 0).

Work around

None.

Please refer to silicon issues 22, 23, and 24 for related information.

Affected Silicon Revisions

Device Flash Memory (KB)	Data Memory (KB)	Device Silicon Revision					
		A0	A1	A2	A3		
16/32	4/8	X	X	—	—		
64	16	X	X	—	X		
128	32	X	X	—	—		
256	16	X	—	—	—		
256	64	—	X	X	—		

22. Module: Flash Memory

When enabled, the Boot Write Protect (BWP) bit inadvertently also protects and overlaps the first page of PWP user program space below 0x0400, (i.e., PWP<8:0> = 0x1FE), in addition to the boot segment, regardless of the state of the Program Write Protection (PWP) bits (DEVCFG0<18:10>). If Boot Write Protect is enabled by setting the BWP bit (DEVCFG0<24>) = 0, users will not be able to Page Erase or program the first page of the PWP user program space. Only user run-time Page Erase/Program operations are affected, which does not include a Bulk erase of the entire Flash.

Work around

None.

Please refer to silicon issues 21., 23., and 24. for related information

Affected Silicon Revisions

Device Flash Memory (KB)	Data Memory (KB)	Device Silicon Revision					
		A0	A1	A2	A3		
16/32	4/8	X	X	—	—		
64	16	X	X	—			
128	32	X	X	—	—		
256	16		—	—	—		
256	64	—			—		

23. Module: Flash Memory

The Program Write Protection (PWP) bit field is off by one page relative to the data sheet definition. In silicon, PWP<8:0> = (n + 1), where 'n' is the DEVCFG0<18:10> value as defined in the data sheet.

TABLE 6: PWP BITS (DEVCFG0<18:10>)

Value	Expected	Actual
111111111	Disabled	Disabled
111111110	Memory below 0x400 is write-protected	Disabled
111111101	Memory below 0x800 is write-protected	Memory below 0x400 is write-protected
• • •		
011111111	Memory below 0x40000 is write-protected	Memory below 0x3FC00 is write-protected

Work around

Set the PWP<8:0> bits (DEVCFG0<18:10>) = {DEVCFG0<PWP> - 1} to correct for the first page protection offset. Please refer to silicon issues 21., 22., and 24. for related information.

Affected Silicon Revisions

Device Flash Memory (KB)	Data Memory (KB)	Device Silicon Revision					
		A0	A1	A2	A3		
16/32	4/8	X	X	—	—		
64	16	X	X	—			
128	32	X	X	—	—		
256	16		—	—	—		
256	64	—			—		

24. Module: Flash Memory

Attempts to protect the entire Flash memory using the following values, will result in no pages being protected.

Program Write Protection bits (DEVCFG0<PWP>):

111101111 = Memory below 0x4000 (16K) address is write-protected.

111011111 = Memory below 0x8000 (32K) address is write-protected.

110111111 = Memory below 0x10000 (64K) address is write-protected.

101111111 = Memory below 0x20000 (128K) address is write-protected.

Work around

To protect the entire Flash including the last page, use the following values:

DEVCFG0<PWP>:

111110000 = Memory below 0x4000 (16K) address is write-protected.

111100000 = Memory below 0x8000 (32K) address is write-protected.

111000000 = Memory below 0x10000 (64K) address is write-protected.

10000000 = Memory below 0x20000 (128K) address is write-protected.

Please refer to silicon issues 21., 22., and 23. for related information.

Affected Silicon Revisions

Device Flash Memory (KB)	Data Memory (KB)	Device Silicon Revision					
		A0	A1	A2	A3		
16/32	4/8	X	X	—	—		
64	16	X	X	—			
128	32	X	X	—	—		
256	16		—	—	—		
256	64	—			—		

25. Module: Power-Saving Modes

On exit from Sleep mode, both the SLEEP and IDLE status bits in the RCON register are set.

Work around

Add the following code to the user application at the point it wakes from Sleep mode:

```
rcon_var1 = RCON;
// ... enter Sleep mode
if (rcon_var1 & 0x4) Nop();
// If IDLE bit already set previously
// before sleep do nothing
else RCONbits.IDLE = 0x0;
// If IDLE bit is not set previously
// and is after Sleep mode then clear
```

Affected Silicon Revisions

Device Flash Memory (KB)	Data Memory (KB)	Device Silicon Revision					
		A0	A1	A2	A3		
16/32	4/8	X	X	—	—		
64	16	X	X	—	X		
128	32	X	X	—	—		
256	16	X	—	—	—		
256	64	—	X	X	—		

26. Module: CTMU

The CTMU internal temperature sensing diode does not function for V_{DD}/AV_{DD} operating voltages that are less than 2.5V.

Work around

None.

Affected Silicon Revisions

Device Flash Memory (KB)	Data Memory (KB)	Device Silicon Revision					
		A0	A1	A2	A3		
16/32	4/8	X	X	—	—		
64	16	X	X	—			
128	32	X	X	—	—		
256	16		—	—	—		
256	64	—	X	X	—		

27. Module: I²C

When the I²C module is operating as a Slave, some reserved bus addresses may be Acknowledged (ACKed) when they should be not Acknowledged (NAKed).

As a result, there will be multiple data NAK interrupts until the Stop condition is asserted.

Work around

When the address interrupt arrives, check the address to determine if it is actually a reserved address. If the address is a reserved address, set a flag and use the flag to ignore subsequent data interrupts. When the Stop condition occurs, clear the flag.

Affected Silicon Revisions

Device Flash Memory (KB)	Data Memory (KB)	Device Silicon Revision					
		A0	A1	A2	A3		
16/32	4/8	X	X	—	—		
64	16	X	X	—			
128	32	X	X	—	—		
256	16		—	—	—		
256	64	—	X	X	—		

28. Module: Bus Matrix

The Flash Memory Size register (BMXPFMSZ) was not programmed with the correct value.

Work around

Use a fixed number based on the size of the part being used.

Affected Silicon Revisions

Device Flash Memory (KB)	Data Memory (KB)	Device Silicon Revision					
		A0	A1	A2	A3		
16/32	4/8	--					
64	16	Date code pre-1750					
128	32	--					
256	64	--					
256	16	Date code pre-1808					

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS60001168**K**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

No data sheet clarifications to be reported in this revision.

APPENDIX A: REVISION HISTORY

Rev A Document (10/2011)

Initial release of this document; issued for revision A0 silicon.

Includes silicon issues 1 (Voltage Regulator), 2 (Oscillator), 3 (I^2C), 4 (USB), 5 (ADC), 6 (ADC), 7 (ADC), 8 (Parallel Master Port (PMP)), and 9 (I/O Ports).

Rev B Document (2/2012)

Added silicon revision A1 for 16/32 KB Flash devices.

Added 64/128 KB Flash devices.

Added silicon issues 10 (CPU) and 11 (Oscillator).

Rev C Document (4/2012)

Updated silicon issue 10 (CPU).

Added silicon issue 12 (Input Capture).

Rev D Document (10/2012)

Updated silicon issue 6 (ADC).

Added silicon issue 13 (Watchdog Timer (WDT)).

Updated the note in the Silicon DEVREV Values tables (see Table 1 and Table 2).

Rev E Document (4/2013)

Updated the Device ID for the PIC32MX150F128B in Table 2.

Updated silicon issue 9 (I/O Ports).

Added silicon issues 14 (Non-5V Tolerant Pins) and 15 (5V Tolerant Pins).

Added data sheet clarification 1 (The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS60001168J):).

Rev F Document (6/2014)

Updated Device ID values in Table 1, Table 2, and Table 3.

Added Silicon DEVREV Values for Devices with 256 KB Flash (see Table 3).

Removed Data Sheet Clarification 1.

Updated silicon issue 9 (I/O Ports).

Added silicon issues 16 (I/O Ports), 17 (I/O Ports), 18 (I/O Ports), 19 (UART), 20 (Timer1), 21 (Flash Memory), 22 (Flash Memory), 23 (Flash Memory), and 24 (Flash Memory).

Rev G Document (4/2015)

Updated the Rev A3 Silicon DEVREV Values for Devices with 64/128 KB Flash in Table 2.

Updated the title of Table 3 to: Silicon DEVREV Values for Devices with 256 KB Flash and 64 KB RAM.

Added Silicon DEVREV Values for Devices with 256 KB Flash and 16 KB RAM (Table 4).

Updated the Affected Revisions for 256 KB Flash Memory devices in Table 5 and in silicon issues 22 (Flash Memory) and 23 (Flash Memory).

Updated issue 9 (I/O Ports).

Added Silicon Issues 25 (Power-Saving Modes) and 26 (CTMU).

Added Data Sheet Clarification 1 (Power-Down Current (I_{PD})).

Rev H Document (4/2016)

Removed Data Sheet Clarification 1.

Added the PIC32MX270FDB device to TABLE 3:.

Added silicon issue 27 (I^2C).

Rev J Document (5/2018)

Added silicon issue 28 (Bus Matrix).

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