



ADC User Guide for Nexus Platform

Technical Note

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
ADC	Analog to Digital Converter
CAL	Calibration
CDC	Clock Domain Crossing
COG	Conversion On-Going
DCS	Dynamic Clock Select
DTR	Digital Temperature Readout
EOC	End of Conversion
FIFO	First In, First Out
LRC	Lower Right Corner
MSPS	Mega Samples per Second
PTAT	Proportional to Absolute Temperature
PLL	Phase Locked Loop
SAR	Successive Approximation Register
SOC	Start of Conversion

1. Introduction

1.1. Overview

The Lattice Nexus™ product line includes the CrossLink™-NX, Certus™-NX, CertusPro™-NX, and MachXO5™-NX families of devices. All families feature an integrated analog block consisting of two Analog to Digital Converters (ADC) and three analog continuous-time comparators.

The ADC is implemented with Successive Approximation Register (SAR) architecture and provides 12-bit resolution with up to 1 MSPS (Mega Samples per Second) conversion speed. It supports both continuous and single-pass conversion modes. Each ADC has a differential analog MUX to select one of the following; eight external dual-mode pin pairs, four internal signals, or one dedicated external analog pin pair. The dual-mode pins can be either digital I/O or analog channel input.

The continuous-time comparator can be used to monitor either separate dual-mode pin-pairs or the ADC channel inputs in parallel. The output of the comparator is provided as continuous and latched outputs.

1.2. Features

The key features of the Analog IP include:

- Two ADCs
 - 12-bit resolution
 - 1 MSPS conversion rate
 - Selectable input signal
 - Eight Dual-mode external input pairs
 - Dedicated external input pair
 - Internal Voltage Rails
 - Internal Junction Temperature Sensing Diode (DTR)
 - External 1.0 V to 1.8 V Reference Voltage
 - Input signal range 0 V to VREF (1.0 V to 1.8 V based on external reference)
 - Unipolar or Bipolar input conversion
 - Three continuous-time comparators
 - Straight binary or 2's complement output

2. Functional Description

2.1. Overview

Each ADC is a 12-bit, 1 MSPS SAR architecture converter that requires an external voltage reference to meet the specifications listed in the data sheet. Each ADC can convert up to a maximum 1.8 V input signal with 1.8 V reference voltage and the input signal can be converted in unipolar mode or bipolar mode. The two ADCs can sample the input sequentially or simultaneously and the sampling periods are programmable by changing the *adc_soc_i* (start of conversion) signal period. Before either ADC can be used for accurate results, they need to be calibrated. Both ADCs are calibrated when the *adc_cal_i* signal is active and calibration is complete when the *adc_calrdy_o* signal is active. The ADC Core Module consists of the following three main blocks ADC0, ADC1, and Control/Status. These blocks are summarized below and shown in the following figures.

- Control/Status Block (see [Figure 2.1](#)):
 - Clock/Reset sub-block
 - ADC Conversion Control sub-block
 - ADC Calibration sub-block
- ADC0 Block (see [Figure 2.2](#)):
 - Three continuous-time comparators with synchronous and latched outputs
 - 12 Input Analog MUX
 - 12-bit SAR ADC
 - Internal Reference Voltage Generation Block
- ADC1 Block (see [Figure 2.3](#)):
 - 12 Input Analog MUX
 - 12-bit SAR ADC
 - DTR (on die temperature sensor)
 - Internal Reference Voltage Generation Block

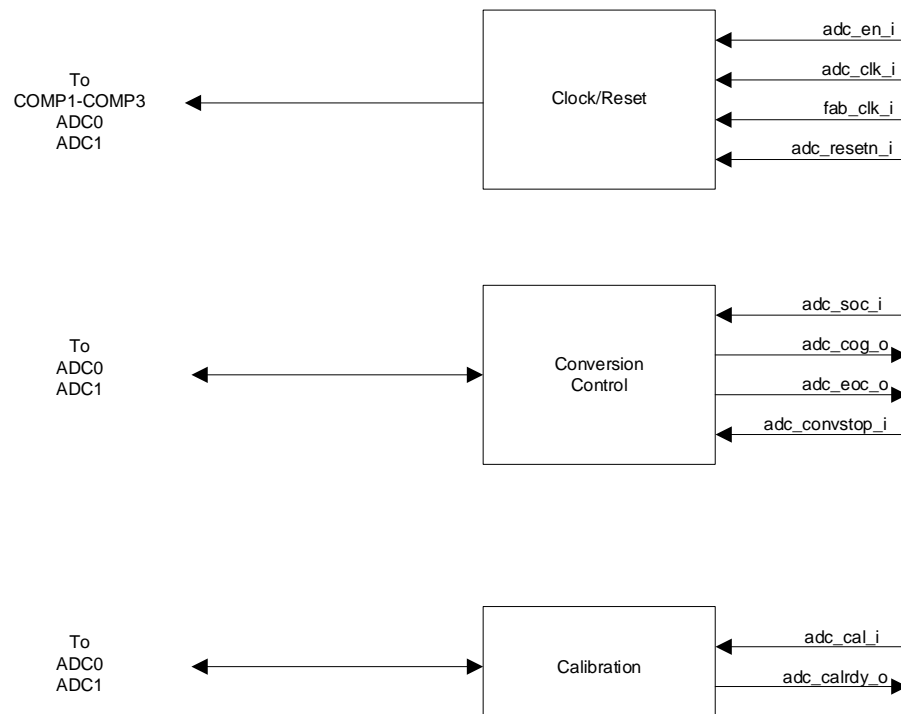


Figure 2.1. ADC Core Module Control and Status Block

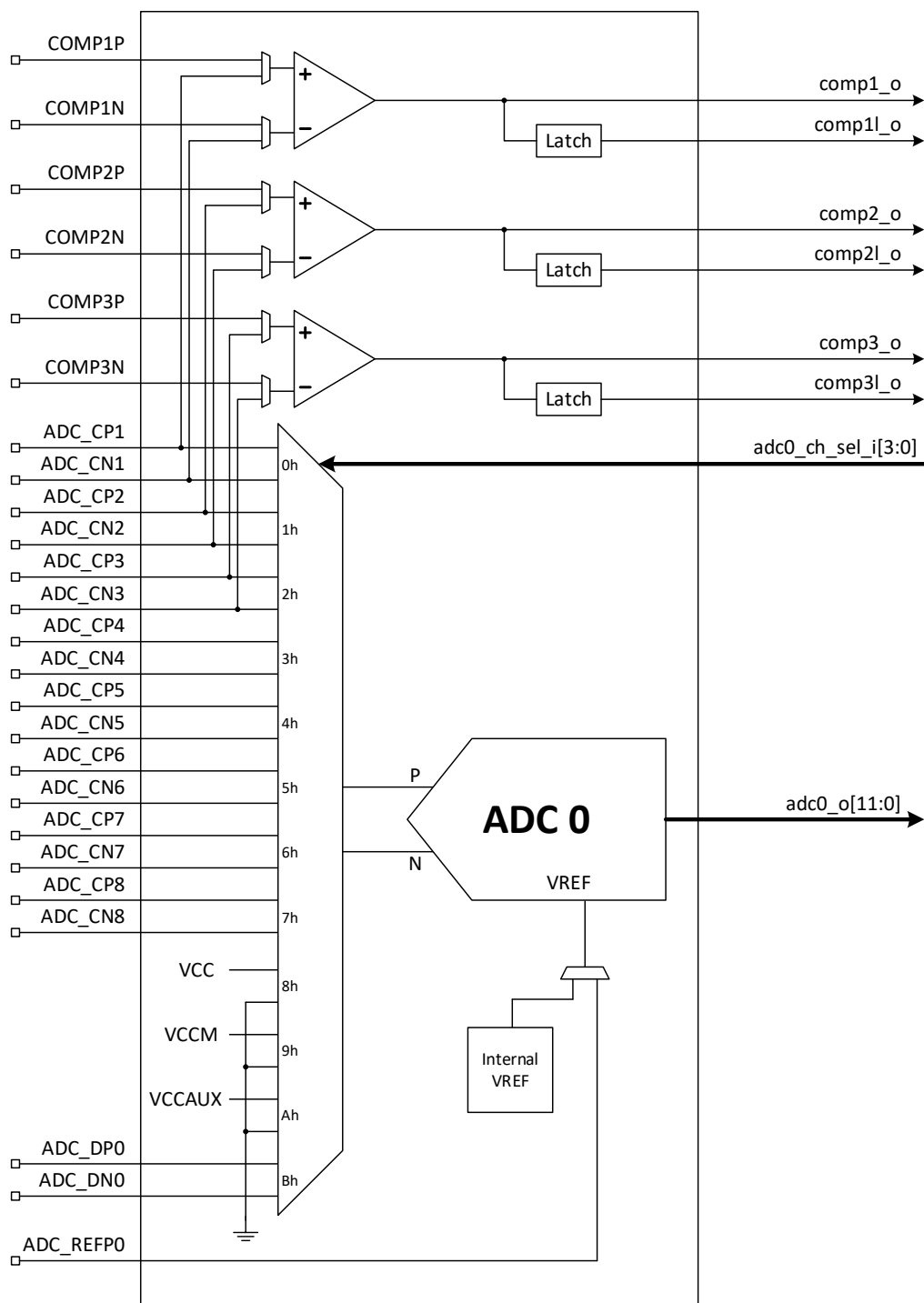


Figure 2.2. ADC Core Module ADC0 Block

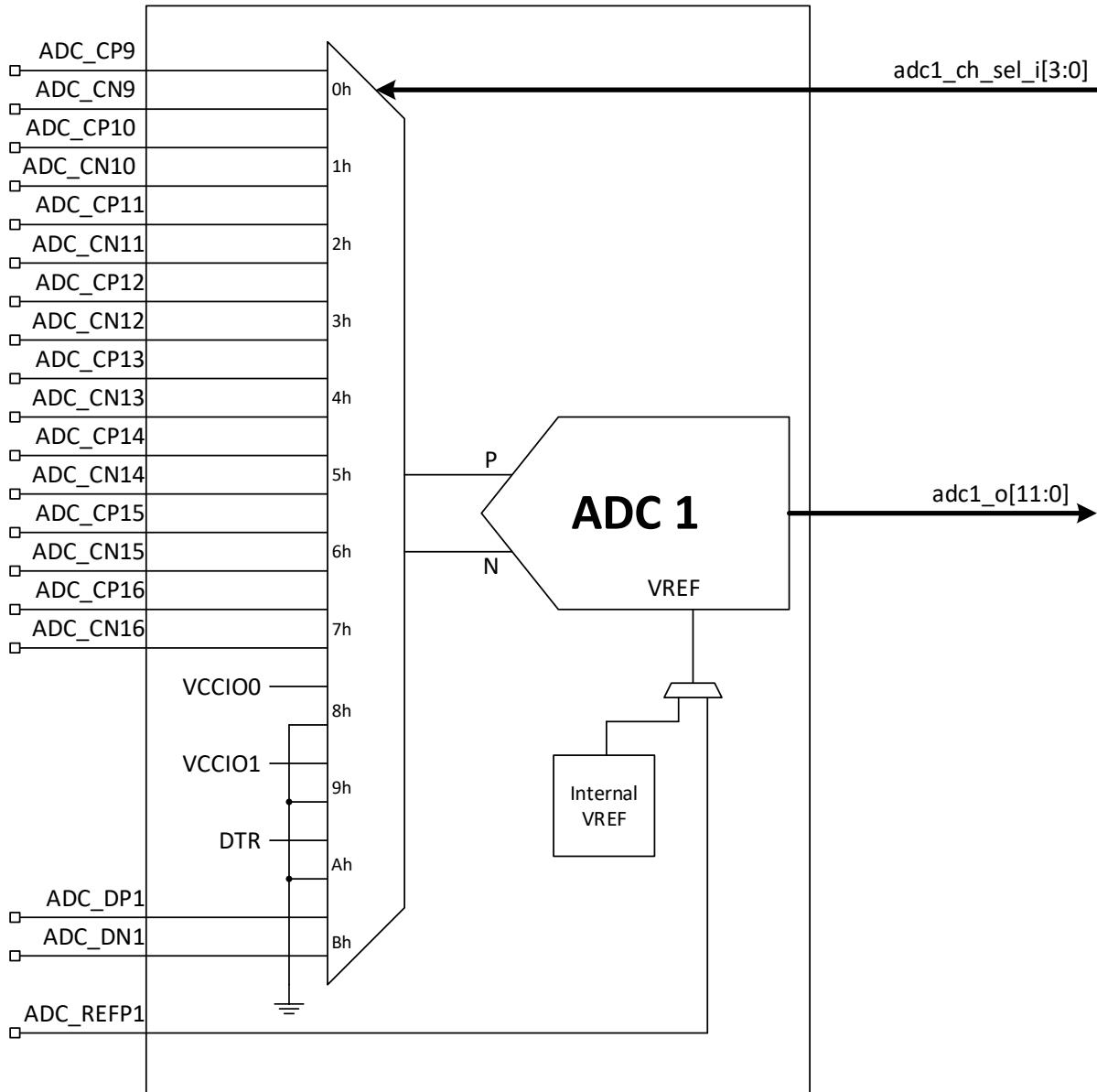


Figure 2.3. ADC Core Module ADC1 Block

2.2. Modules Description

2.2.1. ADC Cores

The ADC Cores are implemented with an SAR (Successive Approximation Register) architecture. The SAR architecture utilizes a binary search algorithm which results in a fast and consistent conversion time. Each of the ADC Cores convert unipolar or bipolar input signal into 12-bit resolution data with maximum 1 MSPS conversion speed sequentially or simultaneously.

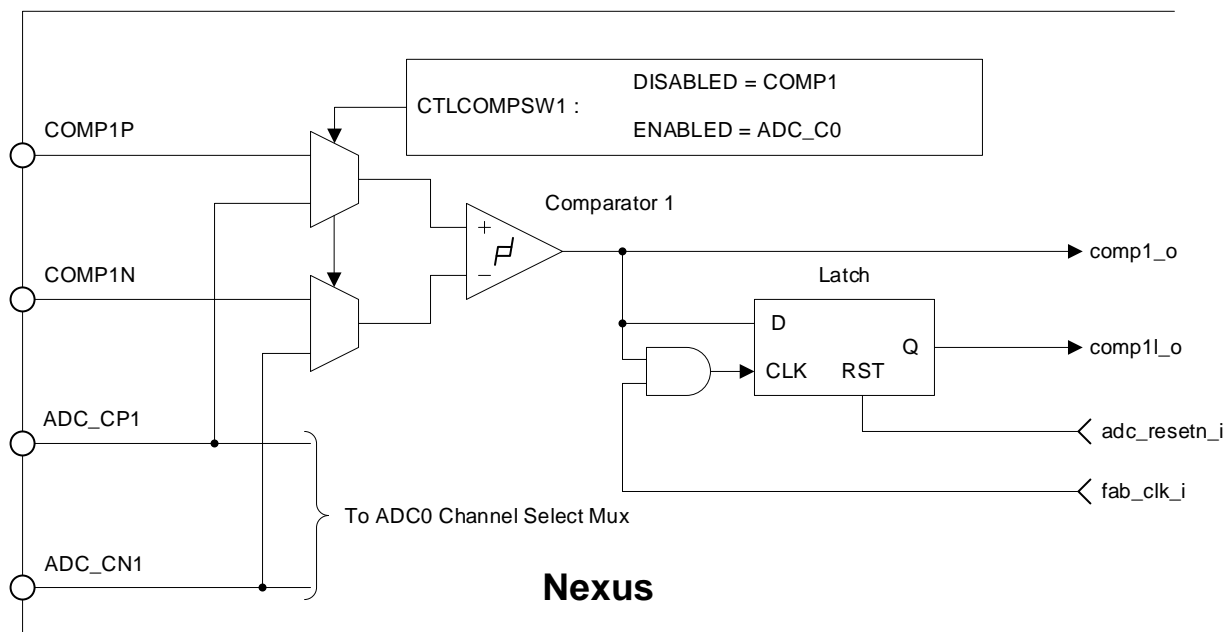


Figure 2.4. Comparator 1 Block Diagram

2.2.2. Comparators

Three analog comparators are available. Both the negative (-) and the positive (+) inputs must be connected to external signals. The output of each comparator is provided both as a continuous-time signal and a latched signal, as shown in Figure 2.4. The inputs can be provided from either dedicated pins (COMP1P and COMP1N) or shared with the ADC channel (ADC_CP1 and ADC_CN1). The selection is controlled by the CTLCOMPSW parameter in the synthesis design phase and therefore is static during operation.

2.2.3. Calibration Controller

A calibration must be run after the ADC block is enabled and before the first conversion is started. The ADC's auto-calibration function calibrates gain and offset errors. The ADC calibration also corrects for process variations and devices mismatches, optimizing its performance. Calibration should be initiated by setting the *adc_cal_i* signal active at least eight clock cycles after reset (*adc_resetr_i*) is deasserted. Calibration needs to be performed any time after the ADC block reset has been activated.

2.2.4. Voltage Reference

The ADC's reference voltage must be provided by an external reference in order to meet the data sheet specifications. The external reference voltage should have at least $\pm 0.2\%$ accuracy. The ADC can convert a maximum 1.8 V input signal with 1.8 V reference voltage.

2.3. Signal Description

Table 2.1 lists the top-level input and output signals for ADC Core Module. The port names in upper-case represent signals that should be connected to physical pins of the device and port names in lower-case represent internal signals.

Table 2.1. ADC Module Ports

Port Name	Direction	Level	Description
Clocks and Reset			
adc_clk_i	In	Digital	ADC clock drives the converter core (from lower right PLL secondary output number 4)
fab_clk_i	In	Digital	Fabric clock synchronizes the ADC control and status signals and Comparator latches
adc_resetrn_i	In	Digital	Active Low reset to ADC, Calibration, and Comparator latches
Control and Status			
adc_en_i	In	Digital	ADC enable.
adc0_o[11:0]	Out	Digital	12-bit ADC 0 output.
adc1_o[11:0]	Out	Digital	12-bit ADC 1 output.
adc0_ch_sel_i[3:0]	In	Digital	ADC 0 channel input selection.
adc1_ch_sel_i[3:0]	In	Digital	ADC 1 channel input selection.
adc_soc_i	In	Digital	Start of conversion.
adc_eoc_o	Out	Digital	End of conversion.
adc_cog_o	Out	Digital	Conversion on-going signal.
adc_convstop_i	In	Digital	Stop on-going conversion control.
adc_cal_i	In	Digital	Calibration start.
adc_calrdy_o	Out	Digital	End of calibration.
comp1_o	Out	Digital	Comparator 1 output
comp1l_o	Out	Digital	Comparator 1 Latched output
comp2_o	Out	Digital	Comparator 2 output
comp2l_o	Out	Digital	Comparator 2 Latched output
comp3_o	Out	Digital	Comparator 3 output
comp3l_o	Out	Digital	Comparator 3 Latched output
Analog Inputs			
ADC_DP0	In	Analog	ADC 0 Dedicated positive input
ADC_DN0	In	Analog	ADC 0 Dedicated negative input
ADC_DP1	In	Analog	ADC 1 Dedicated positive input
ADC_DN1	In	Analog	ADC 1 Dedicated negative input
COMP1IP	In	Analog	Comparator 1 positive external input
COMP1IN	In	Analog	Comparator 1 negative external input
COMP2IP	In	Analog	Comparator 2 positive external input
COMP2IN	In	Analog	Comparator 2 negative external input
COMP3IP	In	Analog	Comparator 3 positive external input
COMP3IN	In	Analog	Comparator 3 negative external input
ADC_CP1	In	Analog	ADC 0 Channel 1 positive input (shared with comparator 1)
ADC_CN1	In	Analog	ADC 0 Channel 1 negative input (shared with comparator 1)
ADC_CP2	In	Analog	ADC 0 Channel 2 positive input (shared with comparator 2)
ADC_CN2	In	Analog	ADC 0 Channel 2 negative input (shared with comparator 2)
ADC_CP3	In	Analog	ADC 0 Channel 3 positive input (shared with comparator 3)
ADC_CN3	In	Analog	ADC 0 Channel 3 negative input (shared with comparator 3)

Port Name	Direction	Level	Description
ADC_CP4	In	Analog	ADC 0 Channel 4 positive input
ADC_CN4	In	Analog	ADC 0 Channel 4 negative input
ADC_CP5	In	Analog	ADC 0 Channel 5 positive input
ADC_CN5	In	Analog	ADC 0 Channel 5 negative input
ADC_CP6	In	Analog	ADC 0 Channel 6 positive input
ADC_CN6	In	Analog	ADC 0 Channel 6 negative input
ADC_CP7	In	Analog	ADC 0 Channel 7 positive input
ADC_CN7	In	Analog	ADC 0 Channel 7 negative input
ADC_CP8	In	Analog	ADC 0 Channel 8 positive input
ADC_CN8	In	Analog	ADC 0 Channel 8 negative input
ADC_CP9	In	Analog	ADC 1 Channel 9 positive input
ADC_CN9	In	Analog	ADC 1 Channel 9 negative input
ADC_CP10	In	Analog	ADC 1 Channel 10 positive input
ADC_CN10	In	Analog	ADC 1 Channel 10 negative input
ADC_CP11	In	Analog	ADC 1 Channel 11 positive input
ADC_CN11	In	Analog	ADC 1 Channel 11 negative input
ADC_CP12	In	Analog	ADC 1 Channel 12 positive input
ADC_CN12	In	Analog	ADC 1 Channel 12 negative input
ADC_CP13	In	Analog	ADC 1 Channel 13 positive input
ADC_CN13	In	Analog	ADC 1 Channel 13 negative input
ADC_CP14	In	Analog	ADC 1 Channel 14 positive input
ADC_CN14	In	Analog	ADC 1 Channel 14 negative input
ADC_CP15	In	Analog	ADC 1 Channel 15 positive input
ADC_CN15	In	Analog	ADC 1 Channel 15 negative input
ADC_CP16	In	Analog	ADC 1 Channel 16 positive input
ADC_CN16	In	Analog	ADC 1 Channel 16 negative input

3. Functional Overview

3.1. ADC Enable

During operation, the *adc_en_i* input is used to enable the ADC or power down the ADC.

3.2. Calibration

The ADC calibration starts with *adc_cal_i* going high (at least eight clocks after *adc_resetsn_i* goes high). When the ADC calibration is complete, *adc_calrdy_o* goes high to indicate that the ADC is calibrated. The timing diagram shown in Figure 3.1 also includes a first conversion starting just after the calibration conclusion. Note the signals CYCLE and ADC STATE represent status within the ADC and CLK is the ADC sample clock (*adc_clk_i* divided by CLK_DIV parameter).

Note that if *adc_resetsn_i* is activated (for example, to reset the comparator latches) then the ADC returns to an uncalibrated state and needs a subsequent calibration cycle for accurate results.

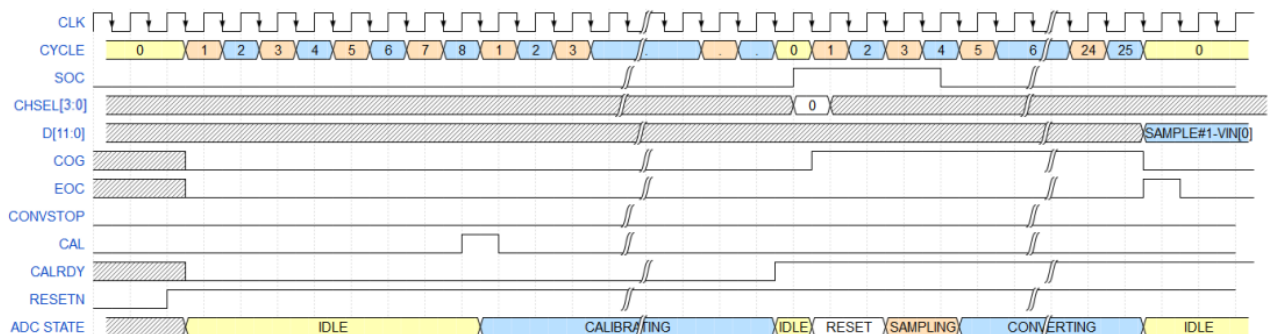


Figure 3.1. ADC Timing Diagram: Calibration

3.3. Reference Voltage

ADC reference voltages are provided on pin ADC_REFP0 for ADC0 and ADC_REFP1 for ADC1. The pins can be connected to a single reference or separate references. The reference sets both the maximum level the ADC can convert and the accuracy of the conversion.

3.4. ADC Input Selection

Inputs *adc0_ch_sel_i* and *adc1_ch_sel_i* are used to select the input channel to the ADC, refer to Figure 2.2 and Figure 2.3 for input selection.

3.4.1. Power Supply Sensor

There are five on-chip power supply sensors that can monitor the FPGA power supply voltages. The sensors can measure VCCIO0, VCCIO1, VCCAUX, and VCC on the package power supply balls. VCCM is an internal supply that is derived from VCCAUX and should measure around 1.25 V. All the power supply monitor signals are passed through a divider before being measured; the power supply voltage can be calculated from the ADC code using Equation 1.

$$\text{Power Supply Voltage} = \frac{\text{ADC output code}}{4096} \times 2.5 \times V_{ref} \quad \text{Eq. 1.}$$

When using the ADC to monitor, a supply that is greater than 3.0 V an external V_{REF} of 1.5 V or greater is needed.

3.4.2. DTR (Digital Temperature Readout)

On-die junction temperature can be monitored using internal PTAT (Proportional to Absolute Temperature) characteristic BJT diode voltage, see Figure 3.2. The DTR output code values are shown in Table 3.1 for various configurations and reference voltages. The temperature can also be computed using Equation 2; only results between -40 °C and +120 °C are valid.

Note: When using Equation 2 in Bi-Polar mode, VREF is the applied reference voltage divided by 2.

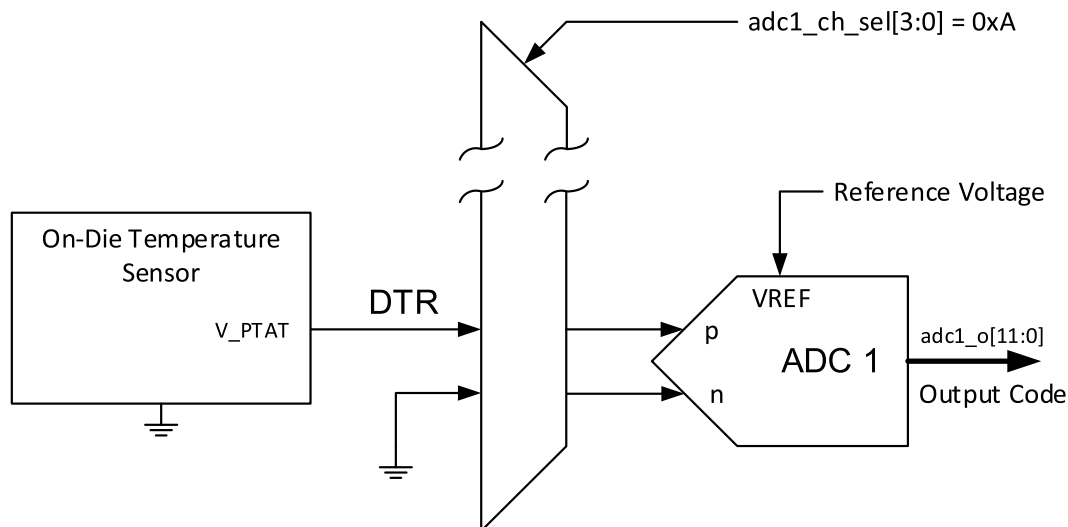


Figure 3.2. Digital Temperature Readout

Table 3.1. DTR Output Code Values as a Function of Temperature and Configuration

Temperature (°C)	V_PTAT (V)	ADC Output Code (Decimal) ¹					
		Uni-Polar VREF				Bi-Polar VREF	
		1.0 V	1.2 V	1.5 V	1.8 V	1.5 V	1.8 V
-40	0.8337	3414	2845	2276	1897	4096	3794
-30	0.8164	3343	2786	2229	1857	4096	3715
-20	0.7990	3272	2727	2181	1818	4096	3636
-10	0.7817	3201	2668	2134	1778	4096	3557
0	0.7643	3130	2608	2087	1739	4096	3478
10	0.7470	3059	2549	2039	1699	4079	3399
20	0.7296	2988	2490	1992	1660	3984	3320
30	0.7123	2917	2431	1945	1620	3890	3241
40	0.6949	2846	2372	1897	1581	3795	3162
50	0.6776	2775	2312	1850	1541	3700	3083
60	0.6602	2704	2253	1802	1502	3605	3004
70	0.6429	2633	2194	1755	1462	3511	2925
80	0.6256	2562	2135	1708	1423	3416	2846
90	0.6082	2491	2076	1660	1384	3321	2768
100	0.5909	2420	2016	1613	1344	3226	2689
110	0.5735	2349	1957	1566	1305	3132	2610
120	0.5562	2278	1898	1518	1265	3037	2531

Note:

- Values of 4096 do not correspond to a temperature, rather this indicates the ADC at full-scale.

$$\text{Temperature } (^{\circ}\text{C}) = 440.6 - (\text{ADC output code} \times V_{\text{REF}}) / 7.105 \quad \text{Eq. 2.}$$

3.5. Output Format

The output can be provided as either straight binary or 2's complement the Analog Input signal conversion to a digital code in bipolar mode is shown in Figure 3.3 and unipolar mode is shown in Figure 3.4.

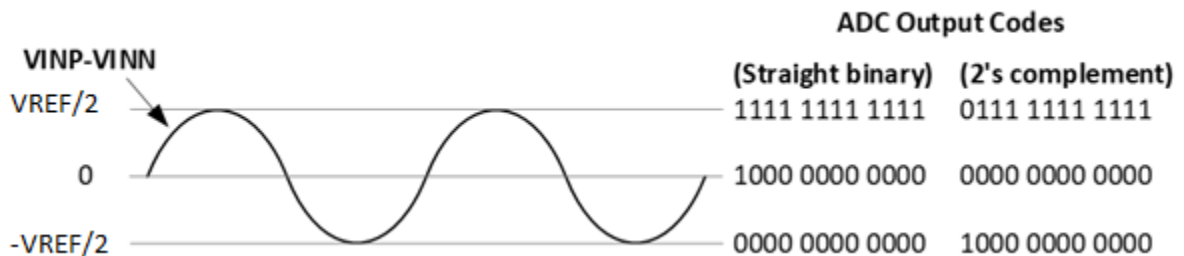


Figure 3.3. Bipolar Input Signal and Output Code Sample

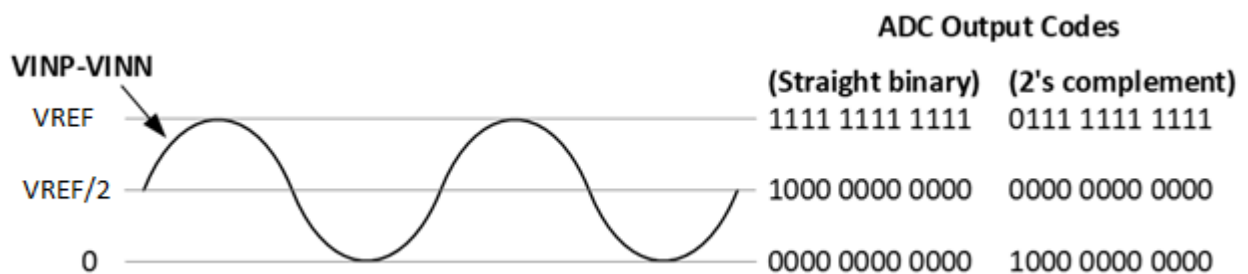


Figure 3.4. Unipolar Input Signal and Output Code Sample

3.6. ADC Conversion

The ADC supports two conversion modes: Continuous conversion mode and Single-Pass conversion mode. In both cases, the *adc_soc_i* (Start-of-Conversion) signal is acquired on the falling edge of the ADC sample clock. Then the analog signal tracking is started for minimum two ADC sample clock cycles after *adc_soc_i* rising edge. The analog input signal tracking time is controlled by the width of the *adc_soc_i* pulse, which can have from minimum four ADC sample clock cycles to unlimited number of sample clock cycles. The tracking of analog input signal stops on the falling edge of the ADC sample clock after *adc_soc_i* is de-asserted. One ADC conversion takes at least 25 ADC sample clock cycles corresponding to four sample clock cycles tracking time and the ADC output data becomes available on the falling edge of the sample clock as indicated by the *adc_eoc_o* (End of Conversion) signal going high. The *adc_eoc_o* signal is synchronized to *fab_clk_i* and is high for one *fab_clk_i* cycle. The *adc_cog_o* (Conversion-On-Going) is synchronized to *fab_clk_i* and asserted about five ADC sample clock cycles after the *adc_soc_i* assertion. The output data is available after *adc_eoc_o* is high and remains available until the end of the next conversion.

The two ADCs can sample the input as sequentially or simultaneously and its sampling period is programmable by changing *adc_soc_i* signal period.

3.6.1. ADC Sample Clock and Fabric Clock

The ADC sample clock, shown as CLK in the timing diagrams, is derived from the *adc_clk_i* which is divided by parameter CLK_DIV. The parameter CLK_DIV must be an even number to provide a 50 percent duty cycle and has a minimum value of 2. The maximum conversion rate is 1 MSPS, which corresponds to a maximum ADC sample clock rate of 25 MHz and *adc_clk_i* of 50 MHz with the minimum CLK_DIV value of 2. Each conversion takes at least 25 ADC sample clock cycles, 21 sample clock cycles plus the *adc_soc_i* pulse width (minimum of four sample clock cycles). The conversion rate for the ADC is varied by varying the ADC sample clock rate. The relation between the ADC sample clock rate and conversion rate is defined as:

$$\text{Conversion Rate} = \text{ADC Sample Clock Rate} / (\text{number of required clocks to finish conversion})$$

The fabric clock (*fab_clk_i*) is used to synchronize the input and output signals between the FPGA logic and the ADC hardware as shown in Figure 3.5. For applications that measure DC supply voltages (internal or external) or the DTR, the *fab_clk_i* can be much slower and asynchronous to the *adc_clk_i*. In these cases a simple averaging or smoothing filter can be applied to the ADC output as needed. However, to operate the ADC at its maximum performance and use the results for subsequent frequency content analysis, then the *fab_clk_i* and *adc_clk_i* need to be synchronized and timed correctly to provide accurate sample timing. For example: using a reference clock of 100 MHz, set the PLL CLKOS4 to bypass (to minimize the jitter content of the ADC sampling clock) for an output of 100 MHz and set another secondary PLL output to 25 MHz, then set the CLK_DIV value for the ADC to four. This results in an ADC sample clock and fabric clock of 25 MHz and the two are synchronized. A finite state machine can drive the *adc_soc_i* once every 25 *fab_clk_i* cycles to achieve 1 MSPS performance. Note the ADC hardware is synchronized to the falling edge of the ADC sample clock and the CDC Logic is rising edge synchronized to provide ample set-up and hold timings when the two clocks are the same frequency. Thus, the user logic within the FPGA should also be synchronized to the positive edge of the *fab_clk_i*.

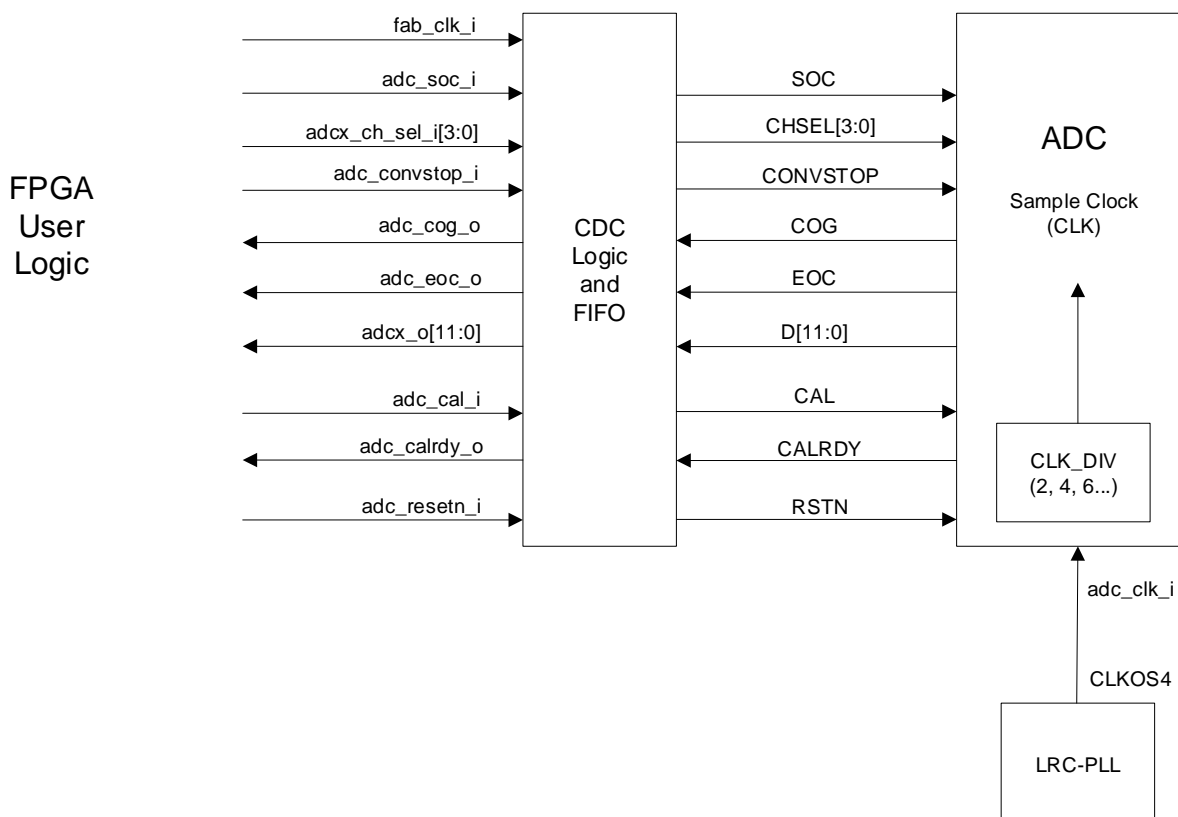


Figure 3.5. Nexus ADC Clock Domains

3.6.2. Programmable Input Signal Sampling Time

ADC's sampling duration can be controlled by changing *adc_soc_i* pulse width. In the timing diagram shown in Figure 3.6 the first conversion has a sampling period of *n* clock cycles and the second conversion has the minimum sample period of four clock cycles. Note the signals CYCLE and ADC STATE represent status within the ADC and CLK is the ADC sample clock (*adc_clk_i* divided by CLK_DIV parameter).

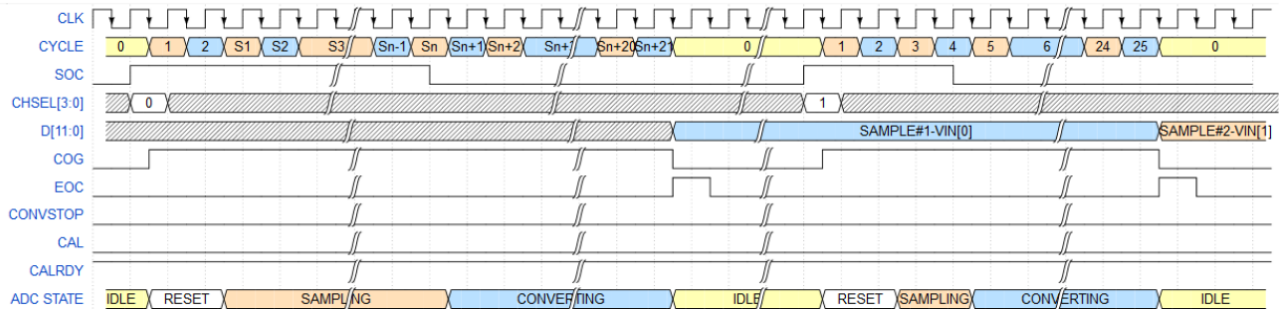


Figure 3.6. ADC Timing Diagram: Programmable Input Signal Sample

3.6.3. Single-Pass Conversion Mode

Single-Pass conversion mode can be used for individual samples conversion or to reduce the sample rate while keeping the same clock frequency and sampling time. When conversion ends and no *adc_soc_i* pulse is applied, the ADC is put into idle mode. In the timing diagram in Figure 3.7 Single-Pass conversions are shown with a minimum sample time (*adc_soc_i* is high for four clock cycles). Note the signals CYCLE and ADC STATE represent status within the ADC and CLK is the ADC sample clock (*adc_clk_i* divided by CLK_DIV parameter).

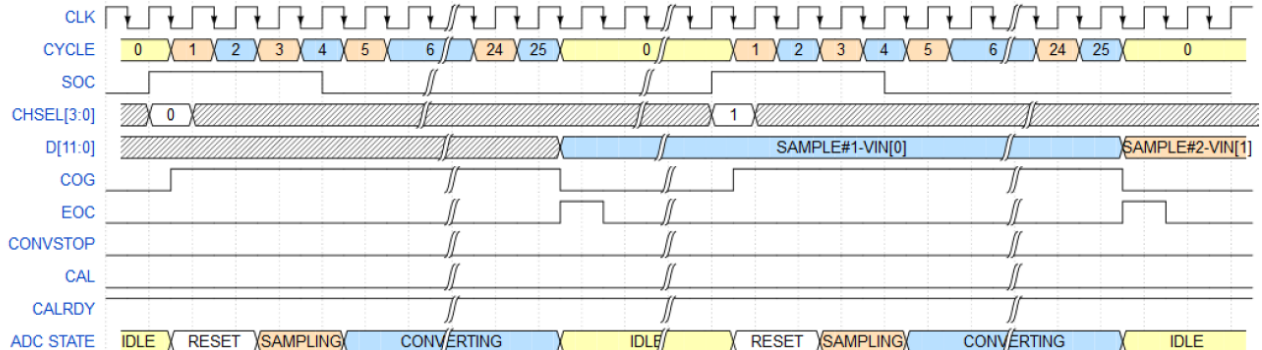


Figure 3.7. ADC Timing Diagram: Single-Pass Conversion Mode

3.6.4. Continuous Conversion Mode

Continuous conversion mode is supported by driving the *adc_soc_i* high at the end of the previous conversion (*adc_clk_i* cycle number 25). The timing diagram in Figure 3.8 shows three continuous conversions. Note the signals CYCLE and ADC STATE represent status within the ADC and CLK is the ADC sample clock (*adc_clk_i* divided by CLK_DIV parameter).

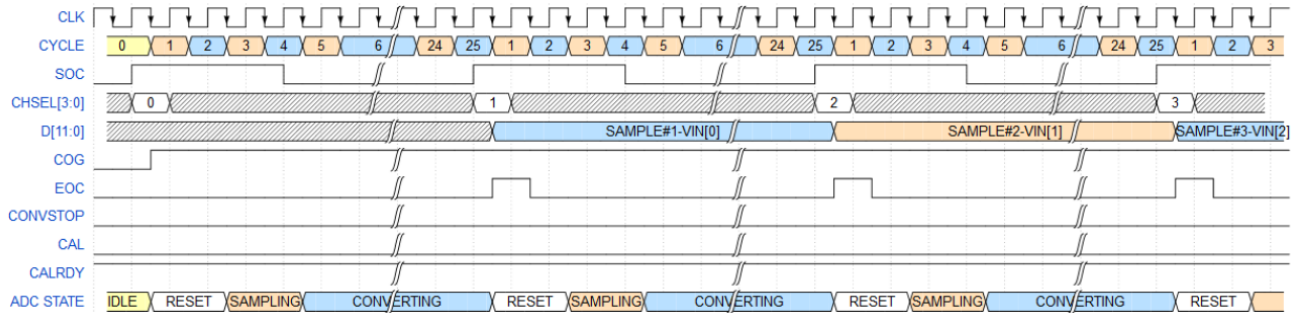


Figure 3.8. ADC Timing Diagram: Continuous Mode

3.6.5. Conversion Stop Signal

The *adc_convstop_i* (conversion stop) input can be used to abort an ongoing conversion. In the timing diagram shown in Figure 3.9, an ongoing ADC conversion aborted by the *adc_convstop_i* asserted high. Note the signals CYCLE and ADC STATE represent status within the ADC and CLK is the ADC sample clock (*adc_clk_i* divided by CLK_DIV parameter).

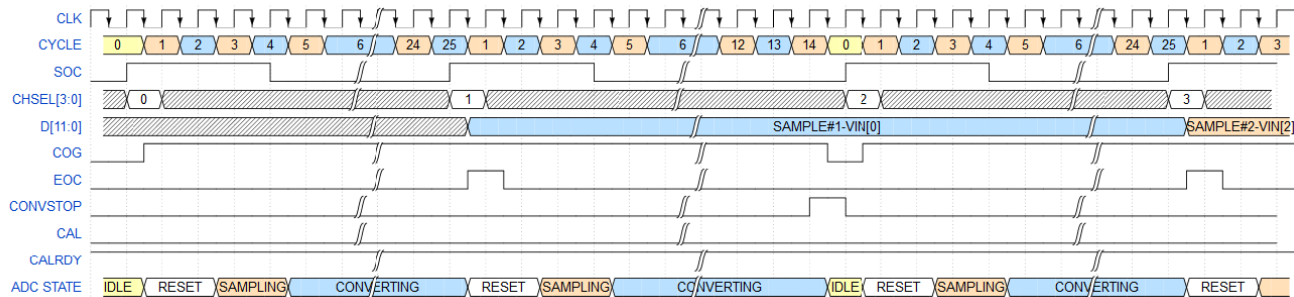


Figure 3.9. ADC Timing Diagram: Aborting an Ongoing Conversion

3.6.6. Comparators

There are three continuous-time comparators. The comparator inputs are selected in the design between ADC channel inputs (in parallel) or separate comparator inputs. Each comparator has two outputs, a continuous output and a latched output. The latched output is synchronized to the *fab_clk_i* and cleared by *adc_resetsn_i*. When the latched comparator outputs are cleared with *adc_resetsn_i*, the ADC calibration will also be reset.

4. Hardware Considerations

4.1. Supply Decoupling

The ADCs are powered by two supplies: one for the analog circuitry ($V_{CC_ADC_18}$) and one for the digital circuitry (V_{CC_ADC}). It is a good practice to decouple the digital noise from the analog circuits, when possible. Figure 4.1 shows an example of how to isolate the digital power and ground from the analog power and ground. The inductor L_1 should be a Ferrite bead with a minimum impedance of $250\ \Omega$ at 1 MHz. The bulk capacitor C_1 should be in the range of 2 to 3 μF . The decoupling capacitors (C_2 , C_3 , and C_4) should be typical 0.1 μF . A single zero- Ω resistor (R_G) is used to connect the digital ground plane to the analog ground plane. Not all Nexus packages have separate connections for the analog power and ground.

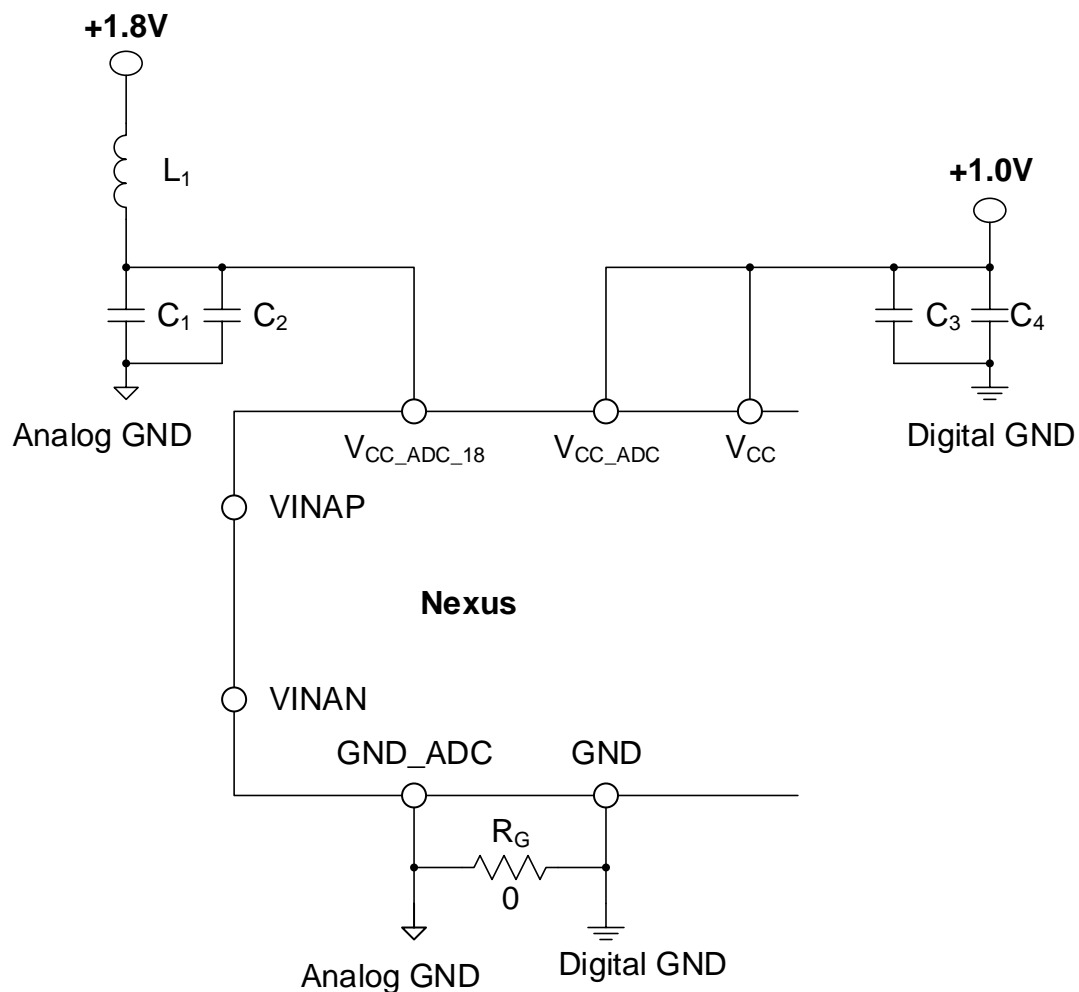


Figure 4.1. ADC Power Supply Decoupling

4.2. Anti-Aliasing Input Filtering

When an ADC is used to sample real time data, it is important to limit the frequency content of the input signal in order to maintain fidelity of the signal that is being processed. Typically, a low-pass filter is used with corner frequency (f_c) set to the Nyquist frequency which is half the sampling frequency (f_s). Signal processing applications often utilize a multiple order low-pass filter (such as a fifth order or more) to effectively block frequency content above f_c . The discussion of such filters is beyond the scope of this technical note. Instead, a single-order resistor-capacitor (RC) low-pass filter is discussed. RC low-pass filters attenuate frequency content above f_c at the rate of -20 dB/decade as shown in Figure 4.2. A differential RC filter is shown in Figure 4.3 for one of the ADCs supported by Nexus devices. The corner frequency for the RC filter is given by Equation 3.

$$f_c = \frac{1}{2\pi(R_{F1} + R_{F2})C_F} \quad \text{Eq. 3.}$$

Where the f_c is in Hertz, R_{F1} and R_{F2} are in Ω , and C_F is in Farads. At the corner frequency, the amplitude of the input signal is attenuated by -3 dB. Table 4.1 provides some example values for typical sampling frequencies.

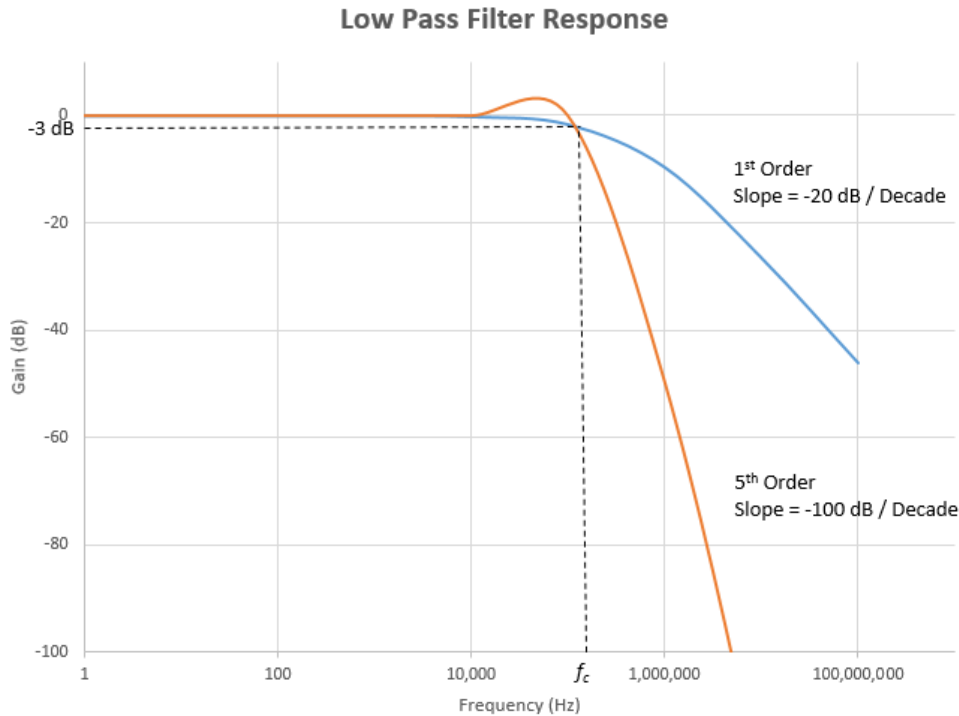


Figure 4.2. Low Pass Filter Response

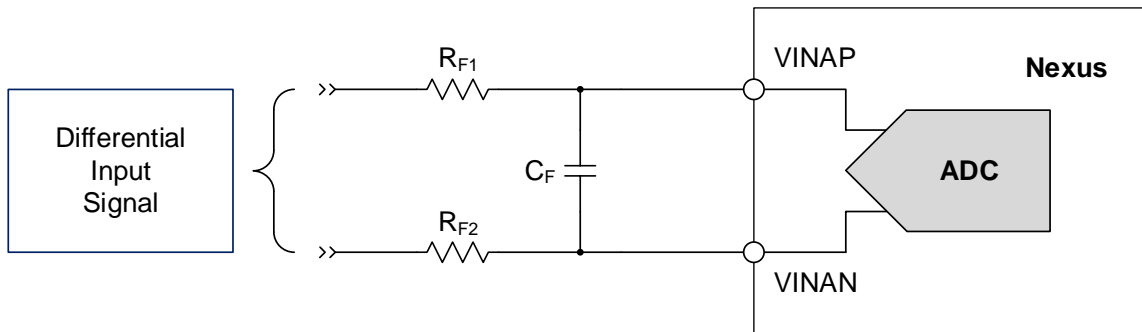


Figure 4.3. Differential ADC Input Filter

Table 4.1. RC Values for Differential Low Pass Filter

$R_{F1} + R_{F2}$ (Ω)	C_F (pF)	F_c (kHz)	f_s (MHz)
200	1,600	500	1.0
200	3,200	250	0.5
720	2,200	100	0.2

The ADCs in Nexus devices can also operate in single-ended input mode. Figure 4.4 shows an example of how a single-ended RC low-pass filter can be connected to the ADCs within Nexus devices. The values in Table 4.1 can also be used for the single-ended filter by setting the value of R_{F2} to zero.

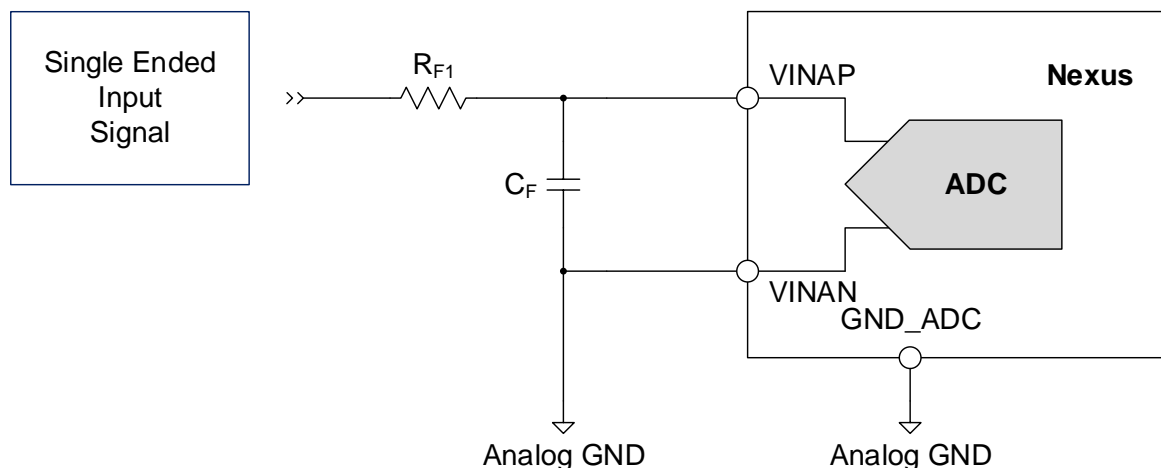


Figure 4.4. Single Ended ADC Input Filter

4.3. External Voltage Reference

An external voltage reference is needed for the ADCs to meet the data sheet specifications. Each ADC has a dedicated external voltage reference pin. These pins can be connected to a single reference or to separate references. The reference voltage source should be accurate to 0.2% over temperature and supply voltage. The external voltage reference should be connected to the analog ground. The supply for the external reference should be isolated from the digital supply using a Ferrite bead and bypass capacitors and/or a separate supply.

Appendix A. ADC Primitive

Primitive Parameters

Table A.1. ADC Parameters

Parameter	Setting	Options	Default
ADC_ENP	Enable ADC	ENABLED, DISABLED	DISABLED
CLK_DIV[7:0]	DCLK Divider Control	2–254 (even number only)	2
CTLCOMP1SW1	Comparator 1 Input Source Selection	ENABLED – GPIO0 DISABLED – Dedicated Input	DISABLED
CTLCOMP1SW2	Comparator 2 Input Source Selection	ENABLED – GPIO1 DISABLED – Dedicated Input	DISABLED
CTLCOMP1SW3	Comparator 3 Input Source Selection	ENABLED – GPIO2 DISABLED – Dedicated Input	DISABLED
DF	Output Data Format Control	STRAIGHT_BINARY, TWOS_COMPLIMENT	STRAIGHT_BINARY
EN_COMP1	Auxiliary Comparator 1 Enable	ENABLED/DISABLED	DISABLED
EN_COMP2	Auxiliary Comparator 2 Enable	ENABLED/DISABLED	DISABLED
EN_COMP3	Auxiliary Comparator 3 Enable	ENABLED /DISABLED	DISABLED
OMA	Channel A Analog Input Configuration	BIPOLAR, UNIPOLAR	BIPOLAR
OMB	Channel B Analog Input Configuration	BIPOLAR, UNIPOLAR	BIPOLAR
REFBUFFAEN	Channel A Internal Reference Buffer Enable	ENABLED, DISABLED	DISABLED
REFBUFFBEN	Channel B Internal Reference Buffer Enable	ENABLED, DISABLED	DISABLED
SLEEP	Enable Sleep Mode (Not supported)	DISABLED	DISABLED
VREFACFG[1:0]	Channel A External Reference Voltage Level Selection	1P0_TO_1P2 – 1.0 V ≤ VREF < 1.2 V, 1P2_TO_1P4 – 1.2 V ≤ VREF < 1.4 V, 1P4_TO_1P6 – 1.4 V ≤ VREF < 1.6 V, 1P6_TO_1P8 – 1.6 V ≤ VREF ≤ 1.8 V	1P0_TO_1P2
VREFASEL	Channel A Reference Voltage Input Configuration	EXTERNAL, INTERNAL ¹	EXTERNAL
VREFBCFG[1:0]	Channel B External Reference Voltage Level Selection	1P0_TO_1P2 – 1.0 V ≤ VREF < 1.2 V, 1P2_TO_1P4 – 1.2 V ≤ VREF < 1.4 V, 1P4_TO_1P6 – 1.4 V ≤ VREF < 1.6 V, 1P6_TO_1P8 – 1.6 V ≤ VREF ≤ 1.8 V	1P0_TO_1P2
VREFBSEL	Channel B Reference Voltage Input Configuration	EXTERNAL, INTERNAL ¹	EXTERNAL

Note:

1. INTERNAL reference is not precise and is mainly used for wafer level testing. An accurate EXTERNAL reference should be used for all customer ADC applications.

Primitive Instantiation

To properly instantiate the ADC block, the following code should be implemented. Use BB_ADC primitives to interface between the top-level I/O pins to the analog inputs of the ADC. Use wires to connect the BB_ADC primitive to the ADC analog inputs. Finally, connect the ADC clock (CLKDCLK) to the on chip PLL_LRC output CLKOS4. For additional information regarding the PLL, see [sysCLOCK PLL Design and User Guide for Nexus Platform \(FPGA-TN-02095\)](#).

Note that the dedicated analog inputs (DP0, DN0, DP1, and DN1) do not require the BB_ADC primitive and may be connected directly from top-level pin to the ADC input, as shown in Listing 3.

Listing 1. Wires to connect the ADC IP

Note that the Lattice Radiant™ 3.0 and earlier do not support the ADC Architectural Module in the IP Catalog, but the ADC can be instantiated by copying and editing the following listings into user code modules.

```

wire  clk_dclk_w;

wire  complip_w;
wire  complin_w;
wire  comp2ip_w;
wire  comp2in_w;
wire  comp3ip_w;
wire  comp3in_w;

wire  [15:0] gpion_w;
wire  [15:0] gpiop_w;

```

Listing 2. Primitives to interface with the analog inputs of the ADC IP

```

genvar i ;
generate
    for (i = 0;(i < 16);i = (i + 1))
        begin
            BB_ADC BB_ADC_GPION_0 (.IOPAD(gpion_i[i]), .INADC(gpion_w[i])) ;
            BB_ADC BB_ADC_GPIOP_0 (.IOPAD(gpiop_i[i]), .INADC(gpiop_w[i])) ;
        end
endgenerate
BB_ADC BB_ADC_COMPLIN (.IOPAD(complin_i), .INADC(complin_w)) ;
BB_ADC BB_ADC_COMPLIP (.IOPAD(complip_i), .INADC(complip_w)) ;
BB_ADC BB_ADC_COMP2IN (.IOPAD(comp2in_i), .INADC(comp2in_w)) ;
BB_ADC BB_ADC_COMP2IP (.IOPAD(comp2ip_i), .INADC(comp2ip_w)) ;
BB_ADC BB_ADC_COMP3IN (.IOPAD(comp3in_i), .INADC(comp3in_w)) ;
BB_ADC BB_ADC_COMP3IP (.IOPAD(comp3ip_i), .INADC(comp3ip_w)) ;

```

Listing 3. Instantiation of the ADC IP

```

ADC # (
    .ADC_ENP ("ENABLED"),
    .CLK_DIV (2),
    .CTLCOMPSW1 ("DISABLED"),
    .CTLCOMPSW2 ("DISABLED"),
    .CTLCOMPSW3 ("DISABLED"),
    .DF ("STRAIGHT_BINARY"),
    .EN_COMP1 ("DISABLED"),
    .EN_COMP2 ("DISABLED"),
    .EN_COMP3 ("DISABLED"),
    .OMA ("BIPOLAR"),

```

```
.OMB ("BIPOLAR"),
.REFBUFAEN ("DISABLED"),
.REFBUFBN ("DISABLED"),
.SLEEP ("DISABLED"),
.VREFACFG ("1P0_TO_1P2"),
.VREFASEL ("EXTERNAL"),
.VREFBCFG ("1P0_TO_1P2"),
.VREFBSEL ("EXTERNAL"))

ADC_inst (
.ADCEN (adc_en_i),
.CAL (cal_i),
.CALRDY (calrdy_o),
.CHASEL (chasel_i),
.CHBSEL (chbsel_i),
.CLKDCLK (clk_dclk_w),
.CLKFAB (clk_fabric),
.COG (cog_o),
.COMP1IN (complin_w),
.COMP1IP (complip_w),
.COMP1O (comp1_o),
.COMP1OL (comp1l_o),
.COMP2IN (comp2in_w),
.COMP2IP (comp2ip_w),
.COMP2O (comp2_o),
.COMP2OL (comp2l_o),
.COMP3IN (comp3in_w),
.COMP3IP (comp3ip_w),
.COMP3O (comp3_o),
.COMP3OL (comp3l_o),
.CONVSTOP (convstop_i),
.DA (da_o),
.DB (db_o),
.EOC (eoc_o),
.DN0 (dn_i[0]),
.DN1 (dn_i[1]),
.DP0 (dp_i[0]),
.DP1 (dp_i[1]),
.GPION (gpion_w),
.GPIOP (gpiop_w),
.RESETN (resetn_i),
.RSTN (resetn_i),
.SOC (soc_i)
);
```

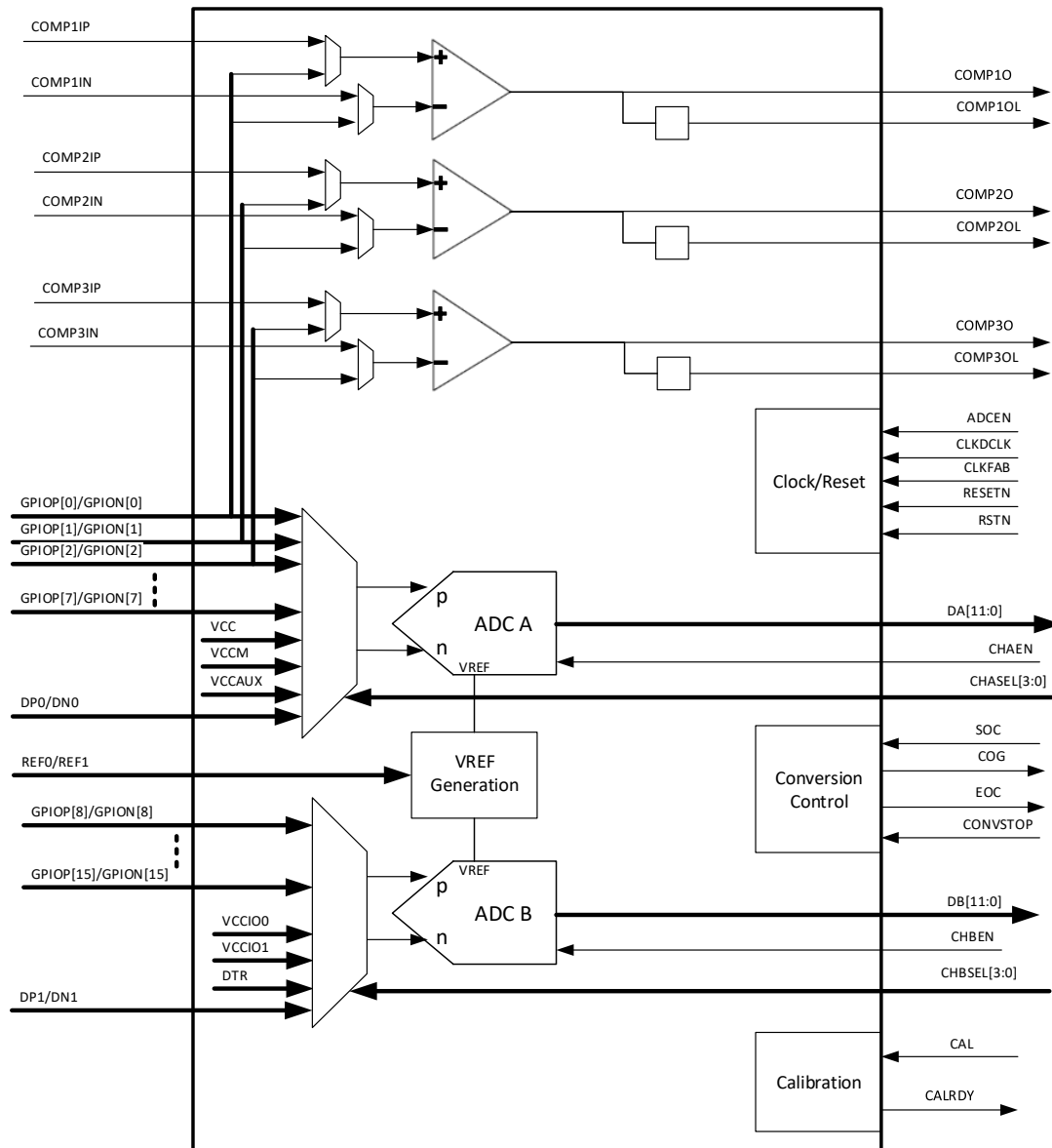


Figure A.1. ADC Primitive Block Diagram

Appendix B. Limitations

The ADC and features are limited based on device family, package, and speed grade as defined in [Table B.1](#).

Table B.1. ADC Core Module Features versus Device and Package

Device ¹	Package	COMP ²	ADC_D ³	ADC_C ⁴	Ext VREF	ADC Supply
LIFCL-40 CrossLink-NX	CABGA400	Y	Y	Y	Y	VCCADC18
	CSBGA289	Y	Y	Y	Y	VCCADC18
	CABGA256	Y	Y	Y	Y	VCCADC18
	CSFBGA121	N	N	List 1	N	VCCAUX
	QFN72	N	N	List 2	N	VCCADC18
LIFCL-17 CrossLink-NX	CABGA256	N	Y	List 1	Y	VCCADC18
	CSFBGA121	N	N	List 1	N	VCCAUX
	QFN72	N	N	List 2	N	VCCADC18
	WLCSP72	N	N	List 2	N	VCCAUX
LFD2NX-40 Certus-NX	CABGA256	Y	Y	Y	Y	VCCADC18
	CABGA196	Y	Y	Y	Y	VCCADC18
	CSFBGA121	Y	N	Y	N	VCCAUX
LFD2NX-17 Certus-NX	CSFBGA121	N	N	List 1	Y	VCCADC18
LFCPNX-100 CertusPro-NX	LFG672	Y	Y	Y	Y	VCCADC18
	BBG484	Y	Y	Y	Y	VCCADC18
	ASG256	Y	Y	Y	Y	VCCADC18
LFMX05-25 MachXO5-NX	BBG400	Y	Y	Y	Y	VCCADC18
	BBG256	Y	Y	Y	Y	VCCADC18

Notes:

1. The ADC is only supported in the Automotive devices (all speed grades) and the higher speed grades of the Commercial / Industrial devices (-8 and -9).
2. All three Comparator external inputs available (COMP1, COMP2, and COMP3).
3. Both dedicated external inputs available (ADC_D0 and ADC_D1).
4. All 16 dual-function external inputs available (ADC_C1 – ADC_C16).

List 1 : All except Channels 5, 11, 12, 13, and 16

List 2 : All except Channels 5, 8, 10, 11, 12, 13, and 16

References

For more info on this FPGA device, refer to the following:

- [CrossLink-NX Family Datasheet \(FPGA-DS-02049\)](#)
- [Certus-NX Family Datasheet \(FPGA-DS-02078\)](#)
- [CertusPro-NX Family Datasheet \(FPGA-DS-02086\)](#)
- [MachXO5-NX Family Datasheet \(FPGA-DS-02102\)](#)
- [sysCLOCK PLL Design and User Guide for Nexus Platform \(FPGA-TN-02095\)](#)
- [ADC Core Module – Lattice Radiant Software User Guide \(FPGA-IPUG-02168\)](#)

For complete information on Lattice Radiant Project-Based Environment, Design Flow, Implementation Flow and Tasks, as well as on the Simulation Flow, see the [Lattice Radiant Software 2.0 User Guide](#).

Technical Support Assistance

For technical support or for additional information regarding security, lock policy settings, and authentication commands, submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 1.4, March 2022

Section	Change Summary
All	Minor adjustments in formatting across the document, including changing reference document titles with Usage Guide to User Guide.
Acronyms in The Document	Added definitions for CAL, CDC, FIFO, and LRC
Introduction	Updated section content to include MachXO5-NX support.
Functional Description	<ul style="list-style-type: none"> Updated overall section content. Updated Figure 2.1. ADC Core Module Control and Status Block, Figure 2.2. ADC Core Module ADC0 Block, Figure 2.3. ADC Core Module ADC1 Block, and Figure 2.4. Comparator 1 Block Diagram. Updated overall content of Table 2.1. ADC Module Ports.
Functional Overview	<ul style="list-style-type: none"> Updated overall Calibration section content. Updated overall ADC Conversion section. Updated Figure 3.1. ADC Timing Diagram: Calibration, Figure 3.6. ADC Timing Diagram: Programmable Input Signal Sample, Figure 3.7. ADC Timing Diagram: Single-Pass Conversion Mode, Figure 3.8. ADC Timing Diagram: Continuous Mode, and Figure 3.9. ADC Timing Diagram: Aborting an Ongoing Conversion.
Appendix B. Limitations	Added this section that defines limitations of ADC and feature availability based on family, package, and speed grade.
References	Added reference to MachXO5-NX datasheet and ADC Core Module Radiant IP User Guide.

Revision 1.3, June 2021

Section	Change Summary
All	Minor adjustments in formatting.
Acronyms in This Document	Removed definition for GPIO.
Introduction	Updated section content to include CertusPro-NX support.
Functional Description	<ul style="list-style-type: none"> Updated overall section content. Updated Figure 2.1 and Figure 2.2. Updated Table 2.1.
Functional Overview	<ul style="list-style-type: none"> Updated overall section content. Updated Figure 3.2 and Figure 3.5.
Appendix A. ADC Primitive	<ul style="list-style-type: none"> Added this section to move Parameters and Instantiation. Moved ADC hardware primitive to this section and added documentation of the software generated ADC IP wrapper. Updated Table A.1 to add table note. Updated Listing 3 in Instantiation.
References	Added reference to CertusPro-NX datasheet.

Revision 1.2, June 2020

Section	Change Summary
All	<ul style="list-style-type: none"> Changed document title from CrossLink-NX ADC Usage Guide to <i>ADC Usage Guide for Nexus Platform</i>. Changed CrossLink-NX to Nexus across the document.
Introduction	Updated Features section.
Functional Description	<ul style="list-style-type: none"> Updated Overview and Voltage Reference section. Updated Table 2.1.
Functional Overview	<ul style="list-style-type: none"> Updated ADC Enable, Reference Voltage, and ADC Input Selection section. Updated Table 3.1.
Parameters	Updated Table 4.1 to add table note.
Instantiation	Updating Listing 3 instantiation.
Hardware Considerations	Added External Voltage Reference section.
References	Updated this section.

Revision 1.1, April 2020

Section	Change Summary
Acronyms in This Document	Updated this section.
Functional Description	<ul style="list-style-type: none"> Updated Overview section. Updated Figure 2.1. ADC Block Diagram. Updated ADC Cores section. Updated Comparators section. Added Figure 2.2. Comparator 1 Block Diagram. Updated Calibration Controller section. Updated Table 2.1. ADC Ports.
Functional Overview	<ul style="list-style-type: none"> Updated Calibration section and adjusted heading number. Updated Figure 3.2. Power Supply Voltage Conversion Graph ($V_{ref} = 1.2\text{ V}$). Updated Table 3.1. DTR Output Code Values as a Function of Temperature and Configuration. Added Equation 2. Moved the Power Supply Sensor and the DTR (Digital Temperature Readout) sub-sections under ADC Input Selection.
Hardware Considerations	Added this section.

Revision 1.0, December 2019

Section	Change Summary
All	Initial release



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